SE LABS

**SYSTRON DONNER**

A THORN EMI company

SYSTRON
DONNER
Member THORN EMI Group

# 6054B

INSTRUMENT DIVISION

## FREQUENCY COUNTER

DOCUMENT NO. 120040-01

# OPERATING AND SERVICE MANUAL

2727 Systron Drive • Concord, California 94518 • U.S.A.
Tel: (415)676-5000 • TWX: 910-481-9479 • Cable: SYSTRON DONNER
FSCM No. 52542

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SYSTRON DONNER CORPORATION

# ADDENDUM

MODEL 6054B

Changes resulting from TCO 976 dated 2/20/79

To eliminate miscounting in WIDE mode when manually reset, A11 Function PC Assembly has been modified.

On schematic 05338601 Figure 7-17 page 7-19:

Add CR1, 1N4151, from U3-12 to U13-8 with cathode connected to U13-8.
Delete connection from U13-8 to U16-1.
Change Q3 from 2N3906 to MPSA65.

On PC Assembly 05338601 Figure 7-16 page 7-18:

Add CR1 directly below the space between R3 and U14 in line with R14 and R25.

On the parts list page 6-37:

Change CR1 from Not Used to

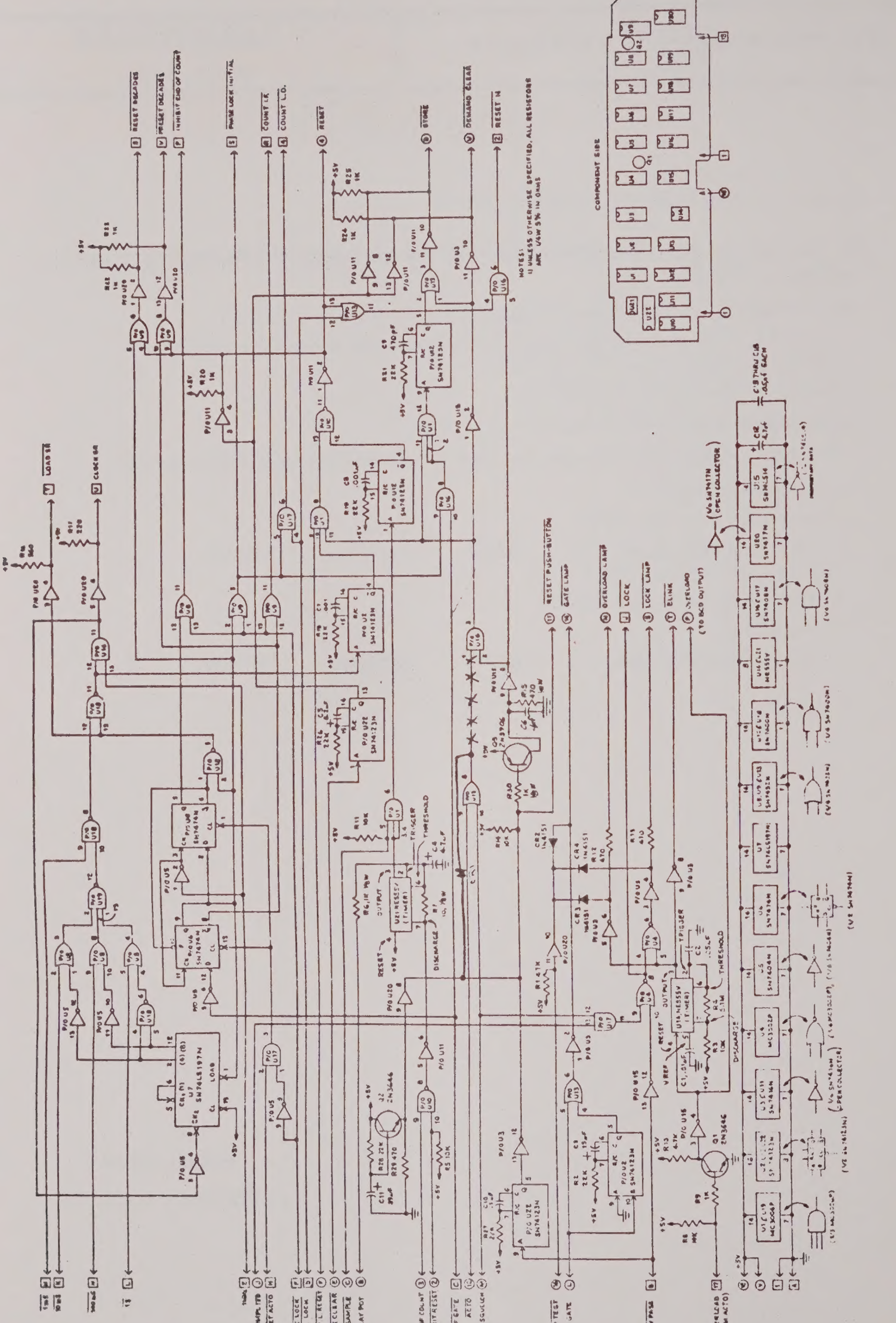
| | | | | | |
|---|---|---|---|---|---|
| CR1 | DIODE, Signal 50V | 03508 | 1N4151 | 100385 | 4 |

Change CR2 to Same as CR1
Change CR3,CR4 to Same as CR1
Change Q3 to:

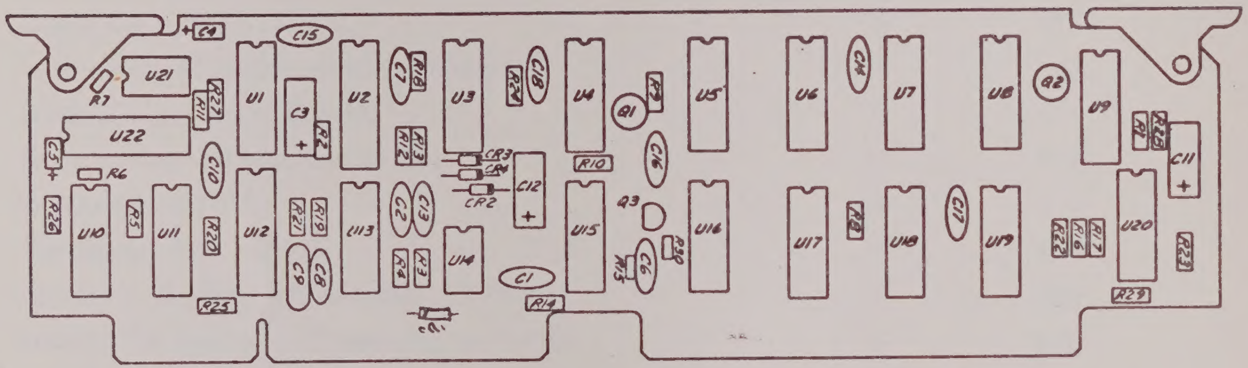
| | | | | | |
|---|---|---|---|---|---|
| Q3 | TRANSISTOR | 04713 | MPSA65 | 101404 | 1 |

**MODEL 6054B**

**FREQUENCY COUNTER**


TBE
10 TBE
100 TBE
1Ē
11 COMPLETED
RESET AUTO
PHASE LOCK
FREQ LOCK
P.L. RESET
CHANGE CLEAR
SAMPLE
DISPLAY POT
END OF COUNT
1st BIT RESET
END OF GATE
AUTO
MODIFIED SQUELCH
LAMP TEST
GATE
LOW PASS
OVERLOAD (FROM AUTO)
LOAD SR
CLOCK SR
RESET DECADES
PRESET DECADES
INHIBIT END OF COUNT
PHASE LOCK INITIAL
COUNT I.F.
COUNT L.O.
RESET
STORE
DEMAND CLEAR
RESET N
RESET PUSH-BUTTON
GATE LAMP
OVERLOAD LAMP
LOCK
LOCK LAMP
BLINK
OVERLOAD (TO BCD OUTPUT)
U7 SN74LS197N
SN74123N
U21 NE555V (TIMER)
U14 NE555V (TIMER)
Q1 2N3646
Q2 2N3646
Q3 2N3906
NOTES:
1) UNLESS OTHERWISE SPECIFIED, ALL RESISTORS ARE 1/4W 5% IN OHMS
COMPONENT SIDE
C13 THRU C18 .05µF EACH
(U6 SN7417N OPEN COLLECTOR)

# FUNCTION PC ASSEMBLY SCHEMATIC


C4
C15
U21
R7
R27
R11
U1
C3
R2
U2
C7
R18
U3
R24
C18
U4
Q1
R9
U5
U6
C14
U7
U8
Q2
U9
R1
R28
C11
U22
C5
R6
C10
R12
R13
CR3
CR4
CR2
C12
R10
C16
R26
U10
R5
U11
R20
U12
R21
R19
U13
C2
C13
C9
C8
R8
R3
U14
C1
U15
Q3
R15
C6
R30
U16
U17
U18
C17
U19
R22
R16
R17
U20
R23
R25
CR1
R14
R29

FUNCTION PC ASSEMBLY

# ADDENDUM

## MODEL 6054B

Due to Provisioning Parts List requirements and to match the Technical Manual to the Provisioning Parts List the following component reference designator changes must be made to the enclosed manual.

Reference designator additions and/or changes:

| Component | Was | Change To |
|---|---|---|
| Digital Extender Assembly 05502901 | – | A28 |
| ACTO Extender Assembly 05502801 | – | A29 |
| 500 MHz Pre Amp PC Assembly 06748401 | – | A22 |
| Attenuator 6 dB 05542806 | – | AT1 |
| Interconnect PC Board Assembly 05344001 | – | A27 |
| Diode PC Assembly 05389001 | – | A25 |
| Power Divider and Detector 055841 | U2 | U11 |
| Pin Leveler 103203 | U1 | U10 |
| Termination 50Ω 102969 | – | AT2 |
| ACTO P.S. Regulator PC Assembly 05393301 | – | A24 |
| Counter P.S. Regulator PC Assembly 05394101 | – | A23 |
| Sampler 057169 | U3,U4 | U12,U13 |
| Connector, PC 20 pin 101253 | – | XA14 - XA17 |
| Power Supply Schematic #7-055122 and Main Chassis PL | | |
| Capacitor, Tant 1 µF 40V 103275 | C1 | C9 |
| CAPACITOR, Tant 1 µF 35V 100082 | C3 | C8 |
| CAPACITOR, Tant 100 µF 100119 | C2, C4 | C6, C7 |
| RESISTOR, WW 2Ω 2W 5% 101772 | R1, R2 | R3, R2 |
| Line Filter, 250V 117643 | U5 | FL1 |
| Receptacle, RF BNC 101155 | J3,4,5 | J3,5,6 |
| Time Base Oscillator PC Assembly 06738201 | – | A26 |
| IEEE 488 Switch Plate Assembly Switches 117573 | S1 - S6 | S7 - S12 |
| Opt. 13 High Stability Oscillator 03342901 | U1 | A26 |
| 6054B-6068 High Stability Oscillator 117733 | U1 | A26 |

**MODEL 6054B**
**FREQUENCY COUNTER**
**Serial Number** ______________
**Issue Date 1 July 1978**

**Final Assembly #057087 Figure 7-1 and Parts List page 6-5.**

Add A28 and A29 REFerence designators to the Digital Extender and ACTO Extender respectively.

**Test Assembly #057164 Figure 7-41 and Parts List page 6-7.**

Change 500 MHz Pre Amplifier PC Assembly to read

| | | | | | | |
|---|---|---|---|---|---|---|
| 10 | A22 | ASSEMBLY, 500 MHz Pre Amp. PC | 52542 | 06748401 | 06748401 | 1 |

Change 6 dB Attenuator to read

| | | | | | | |
|---|---|---|---|---|---|---|
| 11 | AT1 | ATTENUATOR, 6 dB | 34078 | 444-6 | 05542806 | 1 |

**Universal Chassis Assembly #057496 Figure 7-42 and Parts List page 6-9.**

Change Interconnect PC Board Assembly to read

| | | | | | | |
|---|---|---|---|---|---|---|
| 2 | A27 | ASSEMBLY, Interconnect PC Board | 52542 | 05344001 | 05344001 | 1 |

Change Diode PC Assembly to read

| | | | | | | |
|---|---|---|---|---|---|---|
| 4 | A25 | ASSEMBLY, Diode PC | 52542 | 05389001 | 05389001 | 1 |

Change U2 Power Divider and Detector to read

| | | | | | | |
|---|---|---|---|---|---|---|
| 20 | U11 | Power Divider and Detector | 52542 | 055841 | 055841 | 1 |

Change U1 PIN Leveler to read

| | | | | | | |
|---|---|---|---|---|---|---|
| 21 | U10 | PIN LEVELER | 50436 | 33102A | 103203 | 1 |

Change Termination 50Ω to read

| | | | | | | |
|---|---|---|---|---|---|---|
| 32 | AT2 | TERMINATION, 50Ω | 16179 | 20020P | 102969 | 1 |

**Main Chassis Assembly #057163 Figure 7-43 and Parts List pages 6-11 and 6-12.**

Change Assembly, ACTO PS Regulator PC to read

| | | | | | | |
|---|---|---|---|---|---|---|
| 4 | A24 | ASSEMBLY, ACTO PS Regulator PC | 52542 | 05393301 | 05393301 | 1 |

Change Assembly, Counter PS Regulator PC to read

| | | | | | | |
|---|---|---|---|---|---|---|
| 5 | A23 | ASSEMBLY, Counter PS Regulator PC | 52542 | 05394101 | 05394101 | 1 |

Change U3,U4 Sampler to read

| | | | | | | |
|---|---|---|---|---|---|---|
| 7 | U12, U13 | SAMPLER | 52542 | 057169 | 057169 | 2 |

Add U3 between item 13 and 14 as follows:

| | | | | | | |
|---|---|---|---|---|---|---|
| | U3 | P/O Option 11, 12 and 13 | | | | |

Change Connector PC 20-pin item 23 to read as follows:

| | | | | | | |
|---|---|---|---|---|---|---|
| 23 | XA14-XA17 | CONNECTOR, PC 20-pin | 05574 | 2VK10D/1-2 | 101253 | 4 |

Change C1 Capacitor Tant 1 μF 40V item 44 to read

| | | | | | | |
|---|---|---|---|---|---|---|
| 44 | C9 | CAPACITOR, Tant 1 μF 40V | 56289 | 150D105X0050A2 | 103275 | 1 |

Change C3 Capacitor, Tant 1 μF 35V item 53 to read

| | | | | | | |
|---|---|---|---|---|---|---|
| 53 | C8 | CAPACITOR, Tant 1 μF 35V | 56289 | 150D105X9035A2 | 100082 | 1 |

Change C2,C4 Capacitor, Tant 100 μF 10V item 54 to read

| | | | | | | |
|---|---|---|---|---|---|---|
| 54 | C6,C7 | CAPACITOR, Tant 100 μF 10V | 56289 | 150D107X9010R2 | 100119 | 2 |

Change R1,R2 Resistor WW 2Ω 2W item 55 to read

| | | | | | | |
|---|---|---|---|---|---|---|
| 55 | R3,R2 | RESISTOR, WW 2Ω 2W 5% | 56289 | 240E2R05 | 101772 | 2 |

**Rear Panel Assembly #055115 Figure 7-46 and Parts List page 6-15.**

Change J3,4,5 Recept RF BNC 101155 to read

| | | | | | | |
|---|---|---|---|---|---|---|
| | J3,5,6 | RECEPT, RF BNC | 81349 | UG-1094 U | 101155 | 3 |

Change U5 Line Filter to read

| | | | | | | |
|---|---|---|---|---|---|---|
| 16 | FL1 | LINE FILTER, 250V | 02777 | F85417 | 117643 | 1 |

**Transformer Chassis Assembly #055116 Figure 7-36 and Parts List page 6-16.**

Change Time Base Oscillator Assembly 06738201 to read

| | | | | | | |
|---|---|---|---|---|---|---|
| 2 | A26 | ASSEMBLY, Time Base Oscillator PC | 52542 | 06738201 | 06738201 | 1 |

**A4, 500 MHz Decade and Gate PC Assembly #05331301 Figure 7-6 & 7-7 and Parts List page 6-24.**

Change L4 Inductor 24 GHz to read

| | | | | | | |
|---|---|---|---|---|---|---|
| | L4 | INDUCTOR, 24 GA wire loop | 52542 | 067637 | 067637 | 2 |

Change Q3 thru Q7 to read

| | |
|---|---|
| Q3,Q5<br>thru<br>Q7 | Same as Q1 |
| Q4 | Same as Q2 |

**A14, N IF PC Assembly #05324601 Figure 7-23 & 7-24 and Parts List page 6-47.**

Change J1 Lug Terminal to read

| | | | | | | |
|---|---|---|---|---|---|---|
| 144 | | LUG, Terminal | 88245 | 2000B-1 | 100482 | 1 |

**A16, Local Osc. & Shifter Assy. #05710401 Figure 7-29 & 7-30 and Parts List page 6-59.**

Change L1 Inductor 14 Ga Wire loop to read

| | | | | | | |
|---|---|---|---|---|---|---|
| | L1 | INDUCTOR, 14 GA Wire Loop | 52542 | 067636 | 067636 | 1 |

**Option 05 IEEE 488 Cable Harness #057363 Parts List page 6-76.**

Change Connector 24-pin P/O Rear Panel item 1 to read

| | | | | | | |
|---|---|---|---|---|---|---|
| 1 | J4 | CONNECTOR, 24-pin P/O Rear Panel | 02660 | 57-20240-2(383) | 117054 | 1 |

**Option 05 IEEE 488 Switch Plate Assembly #057358 Parts List page 6-76 and Block Diagram Figure 7-53.**

Change S1-S6 Switch, Slide to read

| | | | | | | |
|---|---|---|---|---|---|---|
| 2 | S7-S12 | SWITCH, Slide SPDT | 79727 | GS111SPDTG10 | 117573 | 6 |

**Option 11 #05545201, Option 12 #05545202, Option 13 #05545203 Figure 7-66 and Parts List page 6-84.**

Change item 20 Oscillators to read

| | | | | | | |
|---|---|---|---|---|---|---|
| 20 | A26 | OSCILLATOR, High Stability Opt. 11 | 52542 | 03342801 | 03342801 | 1 |
| 20 | A26 | OSCILLATOR, High Stability Opt. 12 | 52542 | 03342701 | 03342701 | 1 |
| 20 | A26 | OSCILLATOR, High Stability Opt. 13 | 52542 | 03342901 | 03342901 | 1 |

# INSTRUCTION

# MANUAL

MODEL 6054B

FREQUENCY COUNTER

Serial Number ___________

Issue Data 1 July 1978

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FSCM No. 52542

# TEST & MEASUREMENT GROUP
# OF
# SYSTRON DONNER
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F – All freight charges will be paid for by the Purchaser.

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WM Division – Sacramento, CA
ACD Division – Sunnyvale, CA
SD GmbH – Munich, West Germany

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# CHAPTER 1

# DESCRIPTION

## 1.1 INTRODUCTION

This manual contains operating and maintenance instructions for the Systron-Donner Model 6054B Frequency Counter. Instrument specifications, replaceable parts lists, and standard options are included.

The Model 6054B measures frequencies from 20 Hz to 24 GHz in three modes. The low range mode makes direct measurements from 20 Hz to 20 MHz. Radio frequency (RF) measurements, 20 MHz to 24 GHz, may utilize a wide band mode, or the normal mode. In addition, frequencies from 20 MHz to 500 MHz are automatically selected for direct measurement. Frequencies from 500 MHz to 24 GHz are measured precisely, and automatically by the use of the Frequency Locked Automatic Computing Transfer Oscillator (FLACTO)*

The wide band mode may be utilized for input signals having low modulation rates at high deviation limits. Communications channels with broad deviation limits, signals which are drifting rapidly, and frequencies from sweepers are examples of frequencies where utilization of the wide band mode is most useful. The normal band mode is utilized to provide high resolution of stable frequency sources, such as signals from microwave synthesizers, multiplied signal sources, and frequency sources which are phase locked to high stability references.

The eleven-digit display features leading zero suppression and automatic decimal placement. A single pushbutton switch tests all display indicators. High stability oscillators, BCD output, and remote control are available as options.

## 1.2 SPECIFICATIONS

Table 1-1 lists the specifications applicable to the Model 6054B.

### TABLE 1-1 SPECIFICATIONS

| FREQUENCY MEASUREMENTS | |
|---|---|
| Low Frequency Input: | |
| Range: | 20 Hz to 20 MHz. |
| Sensitivity: | 10 mV rms. |
| Input Impedance | 1 Megohm/20 pF. |
| Coupling: | ac. |
| Connector: | BNC type. |
| Maximum Input Without Damage: | 20 to 100 Hz: 200 Vrms<br>100 Hz to 100 kHz: 20 Vrms<br>100 kHz to 20 MHz: 2 Vrms |
| RF Frequency Input: | |
| Range: | 20 MHz to 24 GHz. |
| Sensitivity: | 20 MHz to 10 GHz -30 dBm<br>10 GHz to 18 GHz -25 dBm<br>18 GHz to 24 GHz -20 dBm |
| Input Impedance: | 50 ohms nominal. |
| VSWR (input signal ≃ -10 dBm): | 2:1 to 12.4 GHz<br>3:1 12.4 GHz to 18 GHz |
| Coupling: | ac. |
| Connector: | Type SMA |
| Operating Dynamic Range: | |
| Prior to Acquisition | After Acquisition |
| 50 dB to 10 GHz | 60 dB to 10 GHz |
| 45 dB to 18 GHz | 55 dB to 18 GHz |
| 40 dB to 24 GHz | 50 dB to 24 GHz |
| Maximum Input Without Damage: | +20 dBm prior to acquisition; +30 dBm after. |
| Jitter: | In Normal mode ±1.5 counts per GHz of input frequency. |
| ACQUISITION TIME | |
| Wide Mode: | First Reading; 400 μs + 56 ms + 1/R x N seconds.<br>Subsequent Readings; 400 μs + 1/R x N seconds. |

---

*FLACTO is a trademark of Systron-Donner Corporation.

## TABLE 1-1 SPECIFICATIONS (Contd)

| | |
|---|---|
| Normal Mode: | First Reading; 157 ms + N x 1 ms + 1/R seconds.<br>Subsequent Readings; 1/R seconds |

*NOTE*

*R = Resolution selected (time base)*

*N = A number which represents the harmonic relationship between the local oscillator and the unknown input frequency.*

| | |
|---|---|
| AMPLITUDE DISCRIMINATION | |
| Of Two Frequencies: | 20 dB (10 dB typical). |
| AM Modulation: | Any modulation index as long as the minimum voltage of the signal is not less than the specified sensitivity. |
| FM Modulation: | |
| Wide Mode: | See figure 1-1. |
| Normal Mode: | See Figure 1-2. |
| Kickback Noise: | -65 dBm typical. |
| TIME BASE | |
| Crystal Frequency: | 10 MHz |
| Aging Rate After Warm-Up: | ±1 part in $10^6$ per year. |
| Frequency Retrack for Off Periods up to Approximately 24 Hrs: | ±5 parts in $10^7$ within 10 seconds. |
| Short Term Aging Rate: | ±5 parts in $10^8$ per day average for 3 days. |
| Temperature Variation: | TCXO with variation of 1 part in $10^6$ over the temperature range of 0 to +50°C. |
| 10% Line Voltage Variation: | ±5 parts in $10^8$. |
| Long-Term Aging Rate: | ±3 parts in $10^7$ for 30 days. |
| INT/EXT TIME BASE | |
| External Input: | A 1 MHz or 10 MHz, 1.5V p-p signal into 1 kΩ provides access to the time base. |
| Connector: | BNC type. |

## TABLE 1-1 SPECIFICATIONS (Contd)

| | |
|---|---|
| 1 MHz OUT | |
| Output: | Provides 1 MHz $\leqslant$2.4V square wave TTL compatible. |
| Connector: | BNC type. |
| GENERAL | |
| Resoltuion: | Selectable from 1 Hz to 1 MHz. |
| Display: | 11 digits, 0.4 in. LED, with autopositioned decimal point; leading zero suppression; measurement units in GHz, MHz, kHz; lock, gate, and remote control indicators; flashing overload indicator. |
| Reset: | Manual and automatic. |
| Recycle Rate: | Adjustable 0.5 ms to 10 seconds and manual. |
| Indicator Test: | Digital readout displays all 8's and all other indicators light. |
| Test: | Measures 1 MHz for resolution selected. |
| Discriminator Output: | Provides a voltage proportional to the modulation superimposed on the RF carrier. The voltage output range is approximately ±2 volts and the frequency deviation band is ±5 MHz. Scale factor is approximately 0.4 volts per MHz. |
| Dimensions: | 3½" H x 16 3/4" W x 17½" D (8.9 x 42.5 x 44.4 cm) |
| Weight: | Approximately 30 lbs (13.6 kg) net; 37 lbs (16.8 kg) shipping. |
| Power: | 115/230 Vac, 50-60 and 400 Hz 106 watts. Switch selectable. |
| Fuse: | Main power, 1.5A, 115V, 0.75A, 230V.<br>Oscillator power, 0.25A, 115V, 0.125A, 230V. |
| Operating Temp: | 0°C to 50°C. |
| Storage Temp: | -40°C to +85°C. |

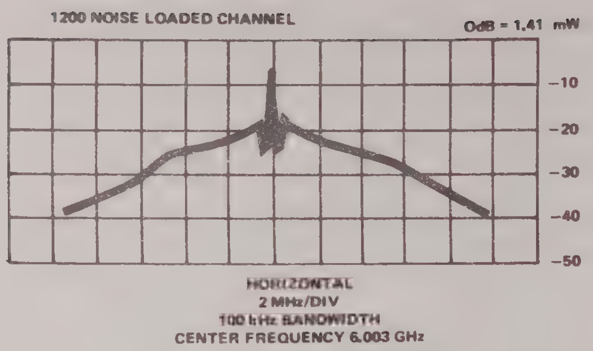


FIGURE 1-1 WIDE MODE FREQUENCY MODULATION

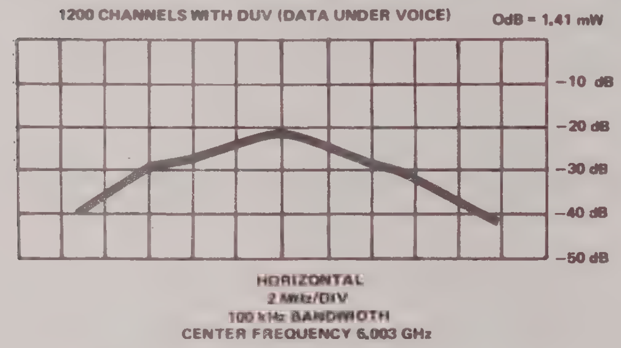


FIGURE 1-2 NORMAL MODE FREQ. MODULATION

## 1.3 STANDARD OPTIONS

Table 1-2 lists the standard options available for the Model 6054B Frequency Counter. A full description, drawings, and parts lists are included in appropriate chapters of this manual.

### TABLE 1-2 STANDARD OPTIONS

| Option | Description |
|---|---|
| 04 | Systems Interface: For computer or semi-computer applications. Complete programmability of all switchable front panel control, with the exception of the power switch, is provided in single line format. All information displayed on the front panel is outputted in parallel 8-4-2-1 BCD format. This digital output included all 11 display digits, annunciator, decimal point, and lock lamp. Logic levels are +5 volts (nominal), positive true, TTL compatible. A print command is provided for indication of end measurement (+5 volt nominal). Grounding inhibit line prevents the counter from making a new measurement. |

### TABLE 1-2 STANDARD OPTIONS (Contd)

| Option | Description | |
|---|---|---|
| 05 | Data Interchange: This system interface option provides data interchange per IEEE STD 488-1975 | |
| 11 | Time Base Oscillator: Increases time base stability to <±3 parts in $10^9$ per 24 hours. | |
| | Aging Rate After Warm-Up: | <±3 parts in $10^9$/24 hours. |
| | Max. Warm-Up for Off Periods to 1 Week: | 72 hours. |
| | Freq. Retrace for Off Periods to Approx. 24 hours: | 1 hour typical to reach ±6 parts in $10^8$ maximum. |
| | Short-Term Aging Rate: | ±1 part in $10^{10}$ rms for 1 second average. |
| | Temperature Variation: | <±2 parts in $10^{10}$/°C typical. Maximum; ±4 parts in $10^9$ over a 20°C change within the range of -20°C to +55°C. |
| | 10% Line Voltage Change from Spec: | ±5 parts in $10^{10}$. |
| | Long-Term Aging Rate: | ±3 parts in $10^8$ for 30 days. |
| 12 | Time Base Oscillator: Increases time base stability to <±1 part in $10^9$ per 24 hours. | |
| | Aging Rate After Warm-Up: | <±1 part in $10^9$/24 hours. |
| | Max. Warm-Up for Off Periods to 1 Week: | 72 hours. |
| | Freq. Retrace for Off Periods to Approx. 24 hours: | 1 hour typical to reach ±6 parts in $10^8$ maximum. |
| | Short-Term Aging Rate: | ±1 part in $10^{10}$ rms for 1 second average. |
| | Temperature Variation: | <±2 parts in $10^{10}$/°C typical. Maximum; ±4 parts in $10^9$ over a 20°C change within the range of -20°C to +55°C. |
| | 10% Line Voltage Change from Spec: | ±5 parts in $10^{10}$. |
| | Long-Term Aging Rate: | ±3 parts in $10^8$ for 30 days. |

### TABLE 1-2 STANDARD OPTIONS (CONT)

| Option | Description |
|---|---|
| 13 | Time Base Oscillator: Increases time base stability to <±5 parts in $10^{10}$ per 24 hours. |
| | Aging Rate After Warm-Up: +5 parts in $10^{10}$/24 hours. |
| | Max. Warm-Up for Off Periods to 1 Week: 72 hours. |
| | Frequency Retrace for Off Periods to Approx. 24 hours: 1 hour typical to reach <±5 parts in $10^9$. |
| | Short-Term Aging Rate: ±5 parts in $10^{11}$ rms for 1 second average. |
| | Temperature Variation: <±2 parts in $10^{10}$/°C typical Maximum: ±4 parts in $10^9$ over a 20°C change within the range of -20°C to +55°C |
| | 10% Line Voltage Change from Spec: ±5 parts in $10^{10}$. |
| | Long-Term Aging Rate: ±1.5 parts in $10^8$ for 30 days. |
| 18 | 18 GHz Operating Range. |
| 20 | Rear Inputs: For system applications the counter can be supplied with rear signal input connectors. The low frequency front panel input connector is paralleled with a second BNC type connector located at the rear panel. This connector is terminated by 50 ohms. The high frequency input connector is removed from the front panel and relocated at the rear. |
| 27 | 50-60/400 Hz Operation: For applications where line frequency is other than 60 Hz, this option allows operation at 50 to 60 Hz and 400 Hz (±10%) without effecting counter specifications. |
| 28X | IF Offsets: In many receiver applications the user may desire to have a direct display of the received frequency. With Option 28X, up to fifteen customer specified offset frequencies may be selected to add to or subtract from the display. |

## 1.4 AGING RATE

Aging Rate defines the average slope of the fractional frequency change of an oscillator plotted against time (figure 1-3). Long-term aging rate is expressed as the fractional change per day, week, or month. Short-term stability is expressed as the average fractional change in frequency per second in a 120-second period.

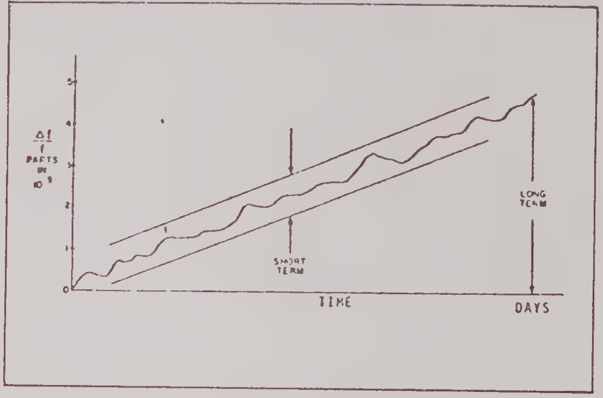


FIGURE 1-3 AGING RATE OF OSCILLATOR

## 1.5 ACCESSORIES

Table 1-3 lists the accessories available for the 6054B Frequency Counter.

### TABLE 1-3 LIST OF ACCESSORIES

| Description | Part Number |
|---|---|
| Coaxial cable, 6' male, BNC each end. | A10338 |
| Line Cord adapter, 3-prong to 2-prong. | E0183 |
| BNC "T" connector. | J0622 |
| BNC 50 ohm terminator. | RF0014 |
| X10 Probe (Tektronix) | P6008 |
| X100 Probe (Tektronix) | P6009 |
| Rack mount brackets (pair) | |
| Equipment carrying case, heavy-duty. This case is lightweight and impack resistant. The interior is foam padded with room for counter, line cord, accessory cable and manual. | D39950 |

## 1.6 TOOLS AND TEST EQUIPMENT

Two extender assemblies are furnished with the Model 6054B to provide extension of the plug-in PCB assemblies when performing corrective maintenance, test or calibration procedures. These extenders are listed as follows as to functional name and Systron-Donner assembly/part number:

| | |
|---|---|
| ACTO Extender Assembly | #05502801 |
| Digital Extender Assembly | #05502901 |

No special tools are required for the maintenance of this counter. A special test fixure is required to perform performance tests on those units equipped with Option 04, Systems Interface or Option 05 Data Interchange (IEEE-488).

Table 5-1 located in Chapter 5 of this manual provides a listing of the recommended test equipment required for the testing and alignment procedures of the Model 6054B Frequency Counter.

# CHAPTER 2

# INSTALLATION

## 2.1 INTRODUCTION

The Model 6054B Frequency Counter is shipped in an operational condition, and is, essentially, ready for use as received. This section contains unpacking, inspection, and installation information to aid in setting up the instrument for immediate use.

## 2.2 RECEIVING INSPECTION

As soon as the instrument is received, check the carton for evidence of damage or rough handling. If damage is found, or is suspected, notify the carrier and your Systron-Donner representative. Open the shipping container only in their presence.

Use care in removing the instrument from the container. Check immediately for loose or broken control knobs, bent or broken connectors, and dents or scratches on the panel surfaces. If damage of any nature is found, refer to the warranty instructions in the front of this instruction manual.

All Systron-Donner instruments must pass rigid inspection tests before leaving the plant. However, upon receipt, a receiving inspection test should be performed immediately after unpacking to ensure that the instrument is still operational. (Refer to Chapter 3).

## 2.3 INSTALLATION

### 2.3.1 Power

The instrument is provided with a 3-conductor power cord which grounds the case when connected through a compatible grounding outlet. If a standard ground outlet is not available, a 3-conductor adapter must be used which provides the necessary grounding connection. Make sure the rear panel 115/230V switch is in the correct position before connecting the instrument to a power source. Also be certain that the proper fuse, F1, is installed (1.5 ampere, 115 Vac; 0.75 ampere, 230 Vac).

### 2.3.2 System Interface Option 04

Remote programming and digital output connections are made to the rear panel mounted Remote and BCD microribbon connectors. Tables 2-1 and 2-2 define the input/output pin descriptions for these connectors.

### 2.3.3 Data Interchange Option 05

This option allows the Model 6054B to be connected to any system using the IEEE488-1975 Interface. Data interchange connections are made to the rear panel connectors and address switches. Table 2-3 defines the input/output pin configuration, Table 2-4 provides program format data and Table 2-5 output sequence data.

## TABLE 2-1 BCD CONNECTOR J1 INTERFACE

| PIN | FUNCTION | PIN | FUNCTION |
|---|---|---|---|
| 1 | $10^0$ 1 bit | 26 | $10^0$ 4 bit |
| 2 | $10^0$ 2 bit | 27 | $10^0$ 8 bit |
| 3 | $10^1$ 1 bit | 28 | $10^1$ 4 bit |
| 4 | $10^1$ 2 bit | 29 | $10^1$ 8 bit |
| 5 | $10^2$ 1 bit | 30 | $10^2$ 4 bit |
| 6 | $10^2$ 2 bit | 31 | $10^2$ 8 bit |
| 7 | $10^3$ 1 bit | 32 | $10^3$ 4 bit |
| 8 | $10^3$ 2 bit | 33 | $10^3$ 8 bit |
| 9 | $10^4$ 1 bit | 34 | $10^4$ 4 bit |
| 10 | $10^4$ 2 bit | 35 | $10^4$ 8 bit |
| 11 | $10^5$ 1 bit | 36 | $10^5$ 4 bit |
| 12 | $10^5$ 2 bit | 37 | $10^5$ 8 bit |
| 13 | $10^6$ 1 bit | 38 | $10^6$ 4 bit |
| 14 | $10^6$ 2 bit | 39 | $10^6$ 8 bit |
| 15 | $10^7$ 1 bit | 40 | $10^7$ 4 bit |
| 16 | $10^7$ 2 bit | 41 | $10^7$ 8 bit |
| 17 | MU 1 bit | 42 | MU 4 bit |
| 18 | MU 2 bit | 43 | MU 8 bit |
| 19 | Decimal 1 bit | 44 | Decimal 4 bit |
| 20 | Decimal 2 bit | 45 | Decimal 8 bit |
| 21 | N.C. | 46 | N.C. |
| 22 | N.C. | 47 | Reset Inhibit |
| 23 | N.C. | 48 | + Print Command |
| 24 | Lo Ref +1.2 or 2.9V | 49 | N.C. |
| 25 | Hi Ref +3.7 or 9V | 50 | Ground |

Notes:
MU = Measurement Units.
N.C. = No Connection.
Lo and Hi Ref = output level from voltage divider across +5 or +15 volts.

## TABLE 2-2 REMOTE CONNECTOR J2 INTERFACE

| PIN | FUNCTION | PIN | FUNCTION |
|---|---|---|---|
| 1 | $10^8$ 1 bit | 19 | $10^8$ 4 bit |
| 2 | $10^8$ 2 bit | 20 | $10^8$ 8 bit |
| 3 | $10^9$ 1 bit | 21 | $10^9$ 4 bit |
| 4 | $10^9$ 2 bit | 22 | $10^9$ 8 bit |
| 5 | $10^{10}$ 1 bit | 23 | $10^{10}$ 4 bit |
| 6 | $10^{10}$ 2 bit | 24 | $10^{10}$ 8 bit |
| 7 | N.C. | 25 | N.C. |
| 8 | N.C. | 26 | N.C. |
| 9 | $\overline{1\ \mu s}$ | 27 | N.C. |
| 10 | $\overline{10\ \mu s}$ | 28 | N.C. |
| 11 | $\overline{100\ \mu s}$ | 29 | $\overline{\text{NORMAL}}$ |
| 12 | $\overline{\text{1 ms}}$ | 30 | $\overline{\text{WIDE}}$ |
| 13 | $\overline{\text{10 ms}}$ | 31 | $\overline{\text{LOW}}$ |
| 14 | $\overline{\text{100 ms}}$ | 32 | $\overline{\text{TEST}}$ |
| 15 | $\overline{\text{1s}}$ | 33 | $\overline{\text{SAMPLE}}$ |
| 16 | LOCK | 34 | $\overline{\text{RESET}}$ |
| 17 | N.C. | 35 | $\overline{\text{REMOTE}}$ |
| 18 | OVERLOAD | 36 | Ground |

## TABLE 2-3 IEEE DATA INTERCHANGE CONNECTOR

| PIN | FUNCTION | PIN | FUNCTION |
|---|---|---|---|
| 1 | DI01 | 13 | DI05 |
| 2 | DI02 | 14 | DI06 |
| 3 | DI03 | 15 | DI07 |
| 4 | DI04 | 16 | DI08 |
| 5 | EOI | 17 | REN |
| 6 | DAV | 18 | Gnd DI06 return |
| 7 | NRFD | 19 | Gnd DI07 return |
| 8 | NDAC | 20 | Gnd DI08 return |
| 9 | IFC | 21 | Gnd IFC |
| 10 | SRQ | 22 | Gnd SRQ return |
| 11 | ATN | 23 | Gnd ATN return |
| 12 | SHIELD (gnd) | 24 | Gnd |

Notes:

1. DIO = data input/output
2. EOI = end or identify
3. DAV = data valid
4. NRFD = not ready for data

## TABLE 2-3
## IEEE DATA INTERCHANGE CONNECTOR (Cont)

5. NDAC = not data accepted
6. IFC = interface clear
7. SRQ = Service request
8. ATN = Attention (wake up)
9. REN = remote enable
10. Ground refers to the signal ground return of the referenced contact.

## TABLE 2-4
## PROGRAM FORMAT IEEE DATA INTERCHANGE

| CODE DI07 | DI06 | DI05 | DI04 | DI03 | DI02 | DI01 | ASCII CHAR. | FUNCTION | GROUP |
|---|---|---|---|---|---|---|---|---|---|
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | @ | 1 MHz | RESOLUTION |
| 1 | 0 | 0 | 0 | 0 | 0 | 1 | A | 1 MHz | |
| 1 | 0 | 0 | 0 | 0 | 1 | 0 | B | 100 kHz | |
| 1 | 0 | 0 | 0 | 0 | 1 | 1 | C | 10 kHz | |
| 1 | 0 | 0 | 0 | 1 | 0 | 0 | D | 1 kHz | |
| 1 | 0 | 0 | 0 | 1 | 0 | 1 | E | 100 Hz | |
| 1 | 0 | 0 | 0 | 1 | 1 | 0 | F | 10 Hz | |
| 1 | 0 | 0 | 0 | 1 | 1 | 1 | G | 1 Hz | |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 | H | WIDE | MODE |
| 1 | 0 | 0 | 1 | 0 | 0 | 1 | I | NORMAL | |
| 1 | 0 | 0 | 1 | 0 | 1 | 0 | J | LOW | |
| 1 | 0 | 0 | 1 | 0 | 1 | 1 | K | TEST | |
| 1 | 0 | 0 | 1 | 1 | 0 | 0 | L | HOLD | CONTROL |
| 1 | 0 | 0 | 1 | 1 | 0 | 1 | M | RECYCLE | |
| 1 | 0 | 0 | 1 | 1 | 1 | 0 | N | SAMPLE | |
| 1 | 0 | 0 | 1 | 1 | 1 | 1 | O | RESET | |
| 1 | 0 | 1 | 0 | 0 | 0 | 0 | P | No Offset | POSITIVE OFFSETS |
| 1 | 0 | 1 | 0 | 0 | 0 | 1 | Q | Cust. Offset | |
| 1 | 0 | 1 | 0 | 0 | 1 | 0 | R | Cust. Offset | |
| 1 | 0 | 1 | 0 | 0 | 1 | 1 | S | Cust. Offset | |
| 1 | 0 | 1 | 0 | 1 | 0 | 0 | T | Cust. Offset | |
| 1 | 0 | 1 | 0 | 1 | 0 | 1 | U | Cust. Offset | |
| 1 | 0 | 1 | 0 | 1 | 1 | 0 | V | Cust. Offset | |
| 1 | 0 | 1 | 0 | 1 | 1 | 1 | W | Cust. Offset | |
| 1 | 0 | 1 | 1 | 0 | 0 | 0 | X | Cust. Offset | NEGATIVE OFFSETS |
| 1 | 0 | 1 | 1 | 0 | 0 | 1 | Y | Cust. Offset | |
| 1 | 0 | 1 | 1 | 0 | 1 | 0 | Z | Cust. Offset | |
| 1 | 0 | 1 | 1 | 0 | 1 | 1 | [ | Cust. Offset | |
| 1 | 0 | 1 | 1 | 1 | 0 | 0 | / | Cust. Offset | |
| 1 | 0 | 1 | 1 | 1 | 0 | 1 | ] | Cust. Offset | |
| 1 | 0 | 1 | 1 | 1 | 1 | 0 | ˆ | Cust. Offset | |
| 1 | 0 | 1 | 1 | 1 | 1 | 1 | — | Cust. Offset | |

Program Subsets:

| | | | |
|---|---|---|---|
| SH1 | TE0 | SR0 | DC0 |
| AH1 | L4 | RL2 | DT0 |
| T7 | LE0 | PP0 | C0 |

TABLE 2-5
OUTPUT SEQUENCE IEEE DATA INTERCHANGE

| BYTE | FUNCTION | ASCII CHAR. | CODE | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | | DIO7 | DIO6 | DIO5 | DIO4 | DIO3 | DIO2 | DIO1 |
| 1 | MSD | 0 → 9 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| 2 | NMSD | 0 → 9 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| 3 | | 0 → 9 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| 4 | | 0 → 9 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| 5 | | 0 → 9 | 0 | 1 | 1 | X | X | X | X |
| 6 | | 0 → 9 | 0 | 1 | 1 | X | X | X | X |
| 7 | | 0 → 9 | 0 | 1 | 1 | X | X | X | X |
| 8 | | 0 → 9 | 0 | 1 | 1 | X | X | X | X |
| 9 | | 0 → 9 | 0 | 1 | 1 | X | X | X | X |
| 10 | NLSD | 0 → 9 | 0 | 1 | 1 | X | X | X | X |
| 11 | LSD | 0 → 9 | 0 | 1 | 1 | X | X | X | X |
| 12 | Delimiter | E | 1 | 0 | 0 | 0 | 1 | 0 | 1 |
| 13 | Exp. Pointer | + | 0 | 1 | 0 | 1 | 0 | 1 | 1 |
| 14 | Exponent | 0 → 6 | 0 | 1 | 1 | 0 | X | X | X |
| 15 | Delimiter | CR | 0 | 0 | 0 | 1 | 1 | 0 | 1 |
| 16 | Delimiter | LF | 0 | 0 | 0 | 1 | 0 | 1 | 0 |

### 2.3.4 Cooling

The instrument design incorporates a cooling fan. Cooling air enters the case through the fan on the rear panel of the instrument, passing through the internal assemblies; then, exhausts through vent cutouts on the rear panel. Care must be exercised not to obstruct the flow of air into or out of the instrument case.

*NOTE*

*If the instrument is to be rack or console mounted determine if the stand/bumper feet will interfere; then, remove these items as required.*

## 2.4 STORAGE AND RESHIPMENT

Environmental conditions during storage and shipment should be limited to a maximum temperature of 85°C and a minimum temperature of -20°C.

To protect the instrument during shipment or storage, use the best packaging methods available. Contact the nearest Systron-Donner field office for materials similar to those used in the original factory package. Contract packing companies are also avaliable to provide dependable custom-packaging service on short notice.

1. If possible, use the original shipping container designed for the instrument. Otherwise, a strong carton (350 lb f/in$^2$ bursting strength) or wooden box should provide adequate protection.

2. Wrap the instrument in heavy paper or plastic before placing it in the shipping container.

3. Completely fill the area around the instrument with packing material; protect the front panel with several sheets of cardboard.

4. Seal the package with strong tape or metal bands. Mark FRAGILE – DELICATE INSTRUMENT on the outside of the package.

5. Refer to the warranty in this manual and check with the nearest Systron–Donner field office for shipping instructions. In all correspondence, refer to the instrument by full model number and serial number.

# CHAPTER 3

# OPERATION

## 3.1 INTRODUCTION

This chapter contains a description of the front and rear panel operating controls, connectors, and indicators along with a step-by-step operating procedure for the instrument. Information about factors which affect the accuracy of measurements are also included.

## 3.2 ACCURACY OF MEASUREMENTS

### 3.2.1 Gating Ambiguity

Digital measuring instruments are subject to a ±1 count ambiguity in the least significant digit of the display. This error is possible because the signal counted is not coherent (synchronized) with the time base pulses that control the signal gate. As Illustrated in figure 3-1, the first or last cycle of the input signal may, or may not, pass through the signal gate during the selected measurement interval.

As the measured frequency is increased, the percent of error due to the ±1 count ambiguity is reduced since it becomes less significant compared to the total count. In any case, the maximum percentage of error is a function of the frequency measured and the number of pulses counted; i.e., the time base selected, and may be expressed by:

$$\text{Max \% error} = \frac{100}{fT} \leqslant 100\%$$

Where: f is the frequency measured in Hz and T is the selected time base in seconds. Thus to measure 1 MHz with a ±0.001% maximum gating error, the RESOLUTION switch must be set to the 10 Hz position.

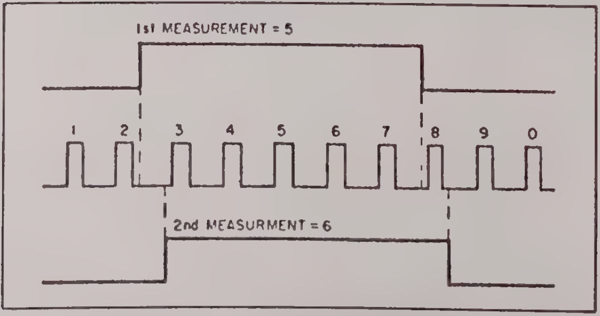


FIGURE 3-1 GATING AMBIGUITY

## 3.3 INTERNAL OSCILLATOR STABILITY

The gating precision, and therefore the accuracy of the count, is dependent upon the stability of the internal oscillator.

In the standard instrument, the oscillator is initially set to within ±1 part in $10^7$ of a 1 MHz frequency standard having at least an order of magnitude higher stability.

Deviation of the Model 6054B oscillator from this frequency then becomes a function of several factors; the most significant being time. Due to certain processes in the frequency determining elements of the oscillator, the "aging" rate is established that can be measured and specified for the oscillator. This aging rate is specified to be less than ±3 parts in $10^7$ per month. Generally, this aging rate decreases with time (providing the instrument remains continuously energized). The error due to oscillator instability may be estimated from:

$$\text{Max \% error} = (\pm 3/10^7 \times M) \times 100$$

Where: M is the number of months since last calibrated.

Oscillator stability is also a function of line voltage and temperature; except for the time immediately after calibration, their effect will be several orders of magnitude less than the effect of aging and may be neglected. To achieve the highest accuracy of measurement, the following considerations apply:

1. Maintain the instrument plugged in and continuously energized.

2. Maintain constant environmental conditions.

3. Monitor or regulate line voltage.

4. Calibrate instrument at intervals consistent with maximum allowable error.

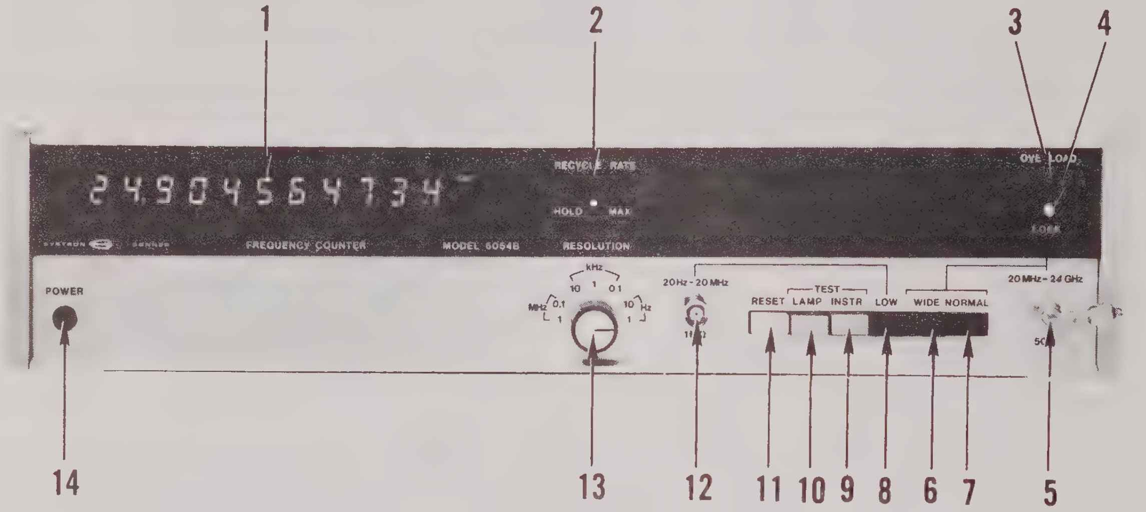
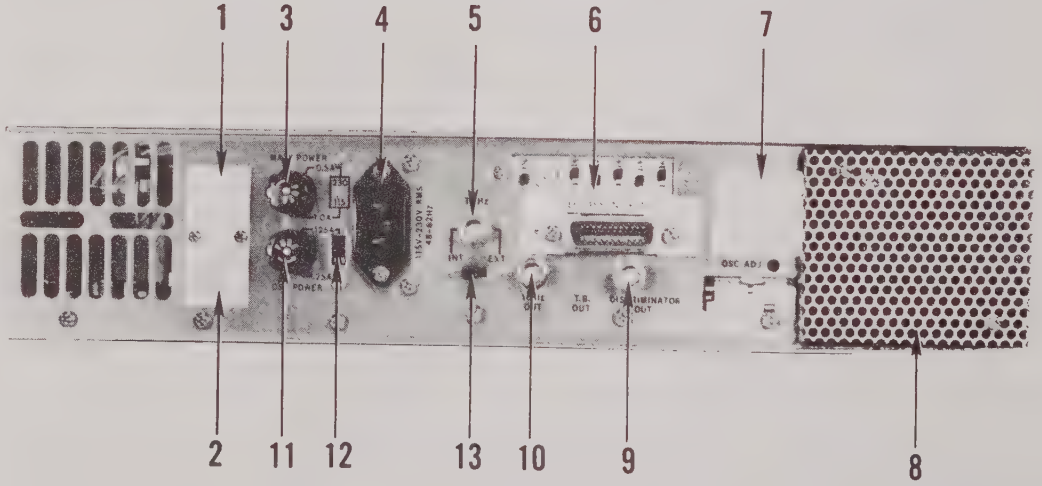

1
2
3
4
24.904564734
RECYCLE RATE
HOLD
MAX
OVE LOAD
LOCK
FREQUENCY COUNTER
MODEL 6054B
RESOLUTION
kHz
10
1
0.1
MHz
0.1
1
10
Hz
1
20 Hz - 20 MHz
TEST
RESET
LAMP
INSTR
LOW
WIDE
NORMAL
20 MHz - 24 GHz
POWER
14
13
12
11
10
9
8
6
7
5

FIGURE 3-2 FRONT PANEL FUNCTIONS


1
3
4
5
6
7
MAIN POWER
DC POWER
115V-230V RMS 48-62Hz
INT
EXT
T.B. OUT
DISCRIMINATOR OUT
OSC ADJ
2
11
12
13
10
9
8

Rear Panel With Option 05 Installed.

FIGURE 3-3 REAR PANEL FUNCTIONS

## 3.4 FRONT PANEL FUNCTIONS

The following table describes the controls, connectors, and indicators on the front panel of the instrument. Index number location is shown in figure 3-2.

TABLE 3-1 FRONT PANEL FUNCTIONS

| Index | Name | Description |
|---|---|---|
| 1 | READOUT and ANNUNCIATOR | Indicates units of measurement, GHz, MHz, kHz, Remote, and Gate. |
| 2 | RECYCLE RATE | Potentiometer and switch, varies display rate from 0.5 ms to 10 seconds and selects the HOLD function. |
| 3 | OVERLOAD | LED indicator; when an overload is connected to the instrument the OVERLOAD indicator and the LOCK indicator flash alternately and the least significant digit also flashes. |
| 4 | LOCK | LED indicator lights when the local oscillator is frequency locked to the RF signal in wide band mode, or phase locked to a suitable multiple of the 10 kHz reference frequency in normal band mode, or sufficient amplitude is present for correct direct count operation at frequencies between 20 MHz and 500 MHz. |
| 5 | 20 MHz - 24 GHz | SMA type connector provides input connection for 20 MHz - 24 GHz frequency range. |
| 6 | WIDE | Interlocked pushbutton switch, when depressed selects the 20 MHz - 24 GHz frequency range and type SMA input connector. Selects the wide band mode for signal measurement. |
| 7 | NORMAL | Interlocked pushbutton switch, when depressed selects the 20 MHz - 24 GHz frequency range and type SMA input connector. Selects the narrow band mode for signal measurement. (Normal mode is over ridden if resolution of less than 1 kHz is selected. |
| 8 | LOW | Interlocked pushbutton switch, when depressed selects the 20 Hz - 20 MHz frequency range and input BNC connector for signal measurement. |
| 9 | TEST/ INSTR | Interlocked pushbutton switch, when depressed, instrument counts 1 MHz internal time base signal. |
| 10 | TEST/ LAMP | Momentary pushbutton switch, when depressed readout will show all eights and all other indicators will light. When released the least significant digit may show zero, dependent on the selected resolution. |
| 11 | RESET | Momentary pushbutton switch, when depressed will set all indicators and control functions to the zero state. When switch is released a new sample will commence. |
| 12 | 20 Hz - 20 MHz | BNC connector provides input connection for low range signals. |
| 13 | RESOLUTION | Rotary switch selects desired resolution in Hz, kHz, or MHz. |
| 14 | POWER | Toggle switch, applies power to the counter, the least significant digit may indicate zero when the power is on and no signal is applied, dependent on the resolution selected. |

## 3.5 REAR PANEL FUNCTIONS

The following table describes the controls and connectors on the rear panel of the instrument. Index number location is shown in figure 3-3.

### TABLE 3-2 REAR PANEL FUNCTIONS

| Index | Name | Description |
|---|---|---|
| 1 | 20 Hz - 20 MHz connector (Option 20) | BNC connector that provides rear panel input, which is parallel to front panel input connector when option 20 is installed. |
| 2 | 20 MHz - 24 GHz connector (Option 20) | The 20 MHz - 24 GHz connector provides rear panel input on high frequencies. This input is supplied when option 20 is installed and only at the rear panel. |
| 3 | MAIN POWER fuse | Provides 1.5A fuse for 115 Vac operation and 0.75A fuse for 230 Vac operation. |
| 4 | Line Power Receptacle | Connects ac power to instrument. |
| 5 | 1 MHz/10 MHz | Connector provides input for an external time base. INT/EXT slide switch selects either internal or external time base. |
| 6 | BCD and REMOTE connectors, Option 04 or IEEE-488 Interface Option 05. | BCD connector provides parallel BCD outputs for 11-digit frequency information, annunciator, decimal point and LOCK lamp information. The REMOTE connector provides input function commands for all front panel controls except POWER switch. |
| | IEEE-488 Interface Option 05 | GPIB I/O Connector and address switches.<br>Option 04 and 05 are mutually exclusive. |
| 6 (Cont) | Connector | 24 pin metric dimensioned connector per IEEE 488 GPIB. |
| | Address | 5-Slide switches to allow selection of the TALK/LISTEN address assigned to the instrument. |
| | PROG-TALK ONLY | Slide switch. Allows the selection of full GPIB handshake function when in its PROG position. When placed in the TALK ONLY position the counter provides output data only and inhibits the other IEEE-488 interface functions. |
| 7 | FREQ ADJ/ COARSE/ FINE control | Adjusts time base oscillator. Depending on which oscillator is installed, access plate varies slightly in physical position. |
| 8 | Blower | Provides cooling air for circulation within instrument. |
| 9 | DISCRIMINATOR connector | BNC output connector that supplies discriminator waveform from lock IF assembly. |
| 10 | 1 MHz OUT connector | BNC connector provides a means of monitoring the internal oscillator when the INT/EXT Switch is placed in the INT position. |
| 11 | OSC POWER fuse | Oscillator power fuse. For 115 Vac operation, fuse is 0.25A, and for 230 Vac operation, fuse is 0.125A. |
| 12 | 115/230 line voltage selector switch | Line voltage selector switch selects 115 Vac or 230 Vac for instrument operation. |
| 13 | INT/EXT selector switch. | A slide switch which selects internal or external reference oscillator operation. |

## 3.6 OPERATING CHARACTERISTICS

The following paragraphs describe the operating ranges and modes, resolution and blanking, FM characteristics, dynamic range and overload.

### 3.6.1 Operating Ranges

There are two basic operating ranges available; 20 Hz to 20 MHz and 20 MHz to 24 GHz. Frequencies in the low range to 20 MHz are measured directly. For those inputs from 20 MHz to 24 GHz measurements are made using the FLACTO technique. FLACTO, Frequency Locked Automatic Computing Transfer Oscillator, operates in two modes Normal and Wide.

### 3.6.2 Resolution and Blanking

Resolution is defined as the value represented by the LSD (least significant digit). Resolution from 1 MHz to 1 Hz in decade steps are available. Blanking removes leading zero's on the digital display providing an unambiguous readout of the most significant digits to the left of decimal only and suppression leading zeros.

### 3.6.3 FM Characteristics

The 6054B will measure carrier frequencies in the presence of frequency modulation, phase modulation or residual noise. The FM characteristics are function of the modulation rate and carrier frequency as shown in Figure 3-4.

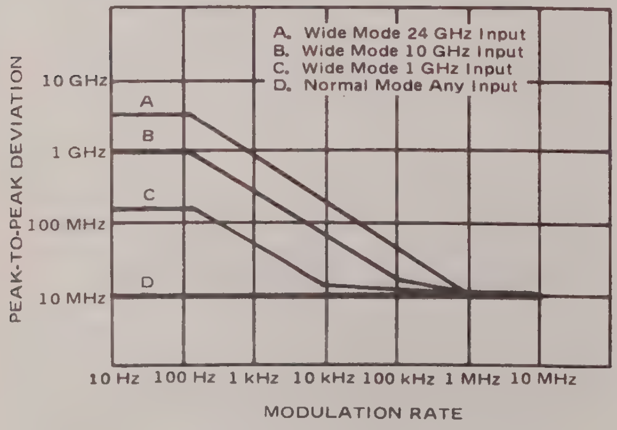


Figure 3-4 Frequency Modulation Characteristics

### 3.6.4 Dynamic Range and Overload Protection

Superior sensitivity for low power readings along with high power protection. Figure 3-5 depicts the wide dynamic operating range from -30 dBm to +30 dBm over the Model 6054's entire frequency band.

Two front panel LED indicators provide a constant display of signal strength. When the input level is equal to or above the counter sensitivity a green lock indicator illuminates. When the input signal is below the lock level the entire readout display is blanked and will remain so until an adequate input signal is provided.

At approximately +20 dBm (100 mW) a red OVERLOAD indicator will illuminate and will alternately flash with the lock indicator and least significant digit to provide a warning of potential signal overload.

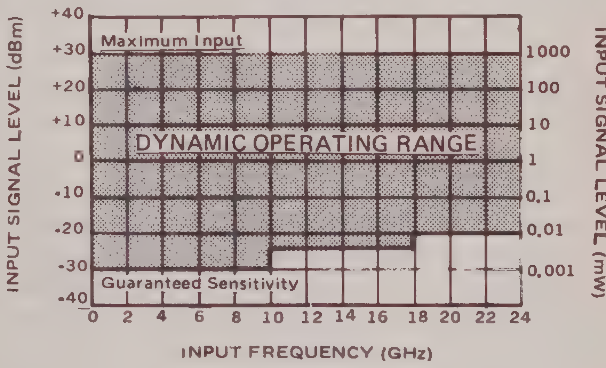


Figure 3-5 Sensitivity and Maximum Signal Level

## 3.7 OPERATING PROCEDURES

Prior to operations, insure the line switch is set to the available line voltage. If high stability oscillator, option 11, 12 or 13 is installed, allow 1 hour for warm up. Check 1 MHz output on rear panel to ensure oscillator is properly calibrated.

### 3.7.1 Low Range, 20 Hz to 20 MHz

1. Turn power on, depress the LOW RANGE switch, set RECYCLE RATE counter-clockwise but not into HOLD.

2. Select desired resolution.

3. Connect a suitable signal source, 20 Hz to 20 20 MHz, to the 20 Hz - 20 MHz BNC connector tor. Minimum signal strength 10 mV rms, maximum 2 Vrms.

4. Adjust RECYCLE RATE as desired.

5. Read the input frequency on the display.

### 3.7.2 RF Range, 20 MHz to 24 GHz

1. Turn power on, select either WIDE or NORMAL RF bandwidth and press selected switch. Set RECYCLE RATE counterclockwise and adjust as required.

2. Connect a suitable signal source, 20 MHz to 10 GHz, minimum signal, -30 dBm; from 10 GHz to 18 GHz, minimum signal, -25 dBm; 18 GHz to 24 GHz, minimum signal, -20 dBm. Maximum input less than +20 dBm.

3. Read the input frequency on the display.

### 3.7.3 Data Interface Option 05

The Model 6054B Frequency Counter may be operated via the General Purpose Interface Bus (GPIB). The Counter can be controlled by, listened to and talked to by, any device or devices that are IEEE STD 488 compatible.

The IEEE STD 488 GPIB system consists of a set of sixteen signal lines that are used to carry data invormation, interface messages and device dependent messages between different devices connected to the bus.

The GPIB is organized into three sets of signal lines:

1. Data bus, 8 signal lines (7 are actively used by the 6054B).
2. Data byte transfer control bus, 3 signal lines.
3. Interface management control bus, 5 signal lines (3 are actively used by the 6054B).

Figure 3-6 illustrates the GPIB structure and its interface capabilities.

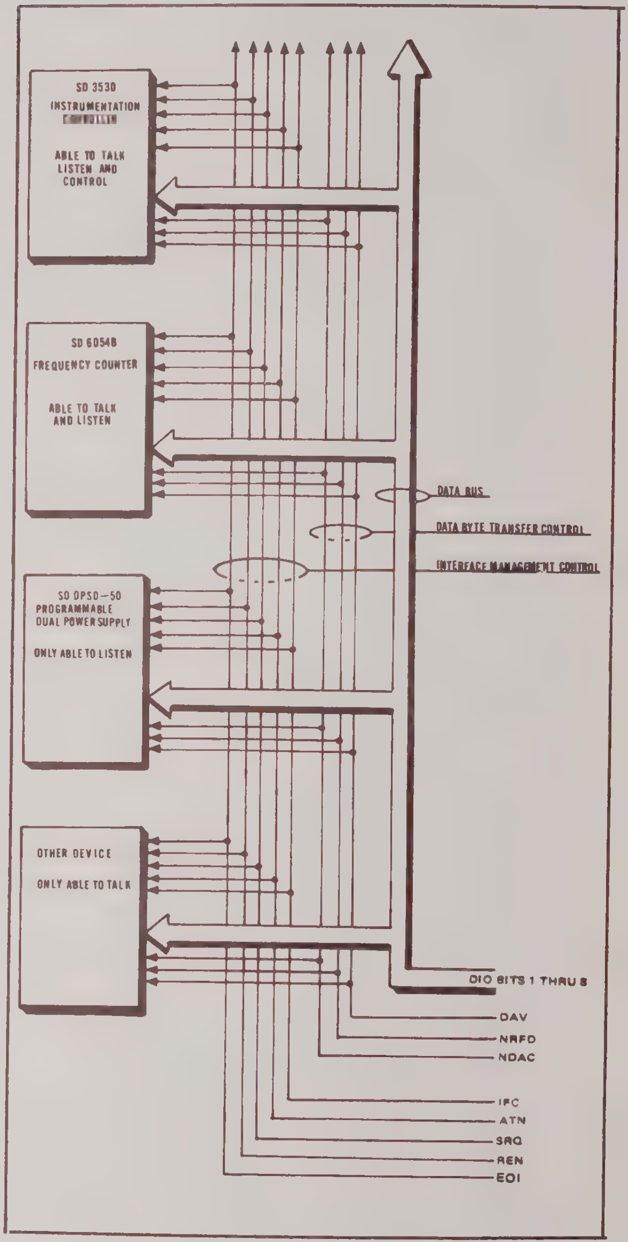

SD 3530
INSTRUMENTATION
ABLE TO TALK
LISTEN AND
CONTROL
SD 6054B
FREQUENCY COUNTER
ABLE TO TALK
AND LISTEN
SD DPSD—50
PROGRAMMABLE
DUAL POWER SUPPLY
ONLY ABLE TO LISTEN
OTHER DEVICE
ONLY ABLE TO TALK
DATA BUS
DATA BYTE TRANSFER CONTROL
INTERFACE MANAGEMENT CONTROL
DIO BITS 1 THRU 8
DAV
NRFD
NDAC
IFC
ATN
SRQ
REN
EOI

FIGURE 3-6 GPIB INTERFACE CAPABILITIES AND BUS STRUCTURE

*NOTE*

*For complete details on the electrical, mechanical and timing requirements, refer to IEEE STD 488 1975.*

The bus interface lines are assigned IEEE STD-488 mnemonics which are defined as follows:

DIO1 through DIO8: Data Input/Output lines 1 through 8, transmitted message bytes in bit parallel, byte-serial format, asynchronously and in a bi-directional manner.

DAV: Data Valid, indicates the availability of data on the DIO lines.

NRFD: Not Ready For Data, indicates when the device is ready to accept data.

ATN: Attention, indicates how the data on the DIO lines is to be interpreted, and which devices will respond to the data.

IFC: Interface Clear, is used to set the interface system, and the devices connected to it into a known quiescent state.

NDAC: **Not Data Accepted,** indicates when the data received was accepted.

SRQ*: Service Request, is used to request service from a controller.

REN: Remote Enable, is used by a controller device (in conjunction with other messages generated in the local logic) to place the Frequency Counter in the Remote Mode of operation.

EOI*: End Or Identify, is used to indicate the end of a data transfer or, with the ATN line to execute a polling sequence.

*These lines are not used by the Model 6054B Frequency Counter, and are supplied with terminations only.

Table 3-3 provides the pin designation for the Rear Panel GPIB 24-pin connector.

**TABLE 3-3 GPIB INTERFACE CONNECTOR**

| PIN NO. | IEEE STD-488 MNEMONIC |
|---|---|
| 1 | DIO1 |
| 2 | DIO2 |
| 3 | DIO3 |
| 4 | DIO4 |
| 5 | EIO (not used) |
| 6 | DAV |
| 7 | NRFD |
| 8 | NDAC |
| 9 | IFC |
| 10 | SRQ (not used) |
| 11 | ATN |
| 12 | GND (Shield) |
| 13 | DIO5 |
| 14 | DIO6 |
| 15 | DIO7 |
| 16 | DIO8 (not used) |
| 17 | REN |
| 18 | GND (DIO6 Return) |
| 19 | GND (DIO7 Return) |
| 20 | GND (DIO8 Return) |
| 21 | GND (IFC Return) |
| 22 | GND (SRQ Return) |
| 23 | GND (ATN Return) |
| 24 | GND (Logic) |

The Frequency Counter may be used On Line or Off Line as selected by the rear panel PROG-TALK ONLY slide switch.

When placed into it's On Line configuration (counter connected to the GPIB via it's rear panel connector and the PROG-TALK ONLY switch set in the PROG position) the Counter may be controlled by an instrumentation controller, a calculator or any other devices that are IEEE STD-488 compatible controllers. When power is applied to the Counter it"wakes up" to the following conditions:

1. Counter is placed in the Monitor mode and the DIO1 through DIO7 lines are set in their tri-state mode.
2. The Resolution is 1 Hz (ASCII G).
3. The Mode selection is set to NORMAL (ASCII I).
4. The HOLD Control function is selected (ASCII L).
5. The Offset function is programmed to No Offset (ASCII P).

The "handshake" process functions as follows:

1. The IFC command is issued by the controller

device and will cause the Counter to monitor the GPIB for further instructions; all data transmission is terminated. If the Counter was addressed as a listener, or talker, it will be unaddressed. The DIO1 through DIO7 lines will go to the tri-state mode.

2. The REN command is issued by the controller device. If the Counter receives it's listen address while the REN line is active, the Counter will enter it's Remote mode and listen for programming data. All front panel controls will become inoperative.
3. When the REN line goes inactive, the Counter will enter it's Local Mode and the Counter's front panel controls will become operative.

The addressing process is controlled by the GPIB ATN line and functions as follows:

1. The Counter is addressed to Talk or Listen by the controller issuing it's assigned Talk or Listen address while the ATN line is set active.
2. If the Counter was addressed to Talk, and the controller issues a Talk address other than the Counter's assigned to Talk address the Counter will automatically deselect itself as a Talker.
3. If the Counter was addressed to Talk, and the controller issues the Counter's Listen address, the Counter will automatically deselect itself as a Talker and assign itself to Listen.
4. If the Counter was addressed to Listen, and the Unlisten (UNL) ASCII ? command is issued by the controller, the Counter will deselect as a Listener.
5. If the Counter was addressed to Listen and the controller issues it's Talk address, the Counter will automatically deselect itself as a Listener, and be reassigned as a Talker.
6. If the controller issues an untalk (UNT) ASCII—command, the Counter will automatically deselect as a Talker.

The Talk and Listen addresses are selected by the Rear Panel 5-digit address switch. The setting of the 5-digit switch determines which talk address and the corresponding Listen address will be assigned to the Frequency Counter. Thirty-one Talk/Listen addresses may be assigned, refer to Table 3-4 for the address to ASCII Code format.

*NOTE*

*A 1-1-1-1-1 address must not be assigned to any device interfacing the bus; these addresses are reserved for the unlisten ASCII (?) and the untalk ASCII (—) commands.*

### TABLE 3-4
### TALK/LISTEN ADDRESS ASSIGNMENTS VS, ASCII CHARACTER

| ADDRESS SWITCH SETTING BITS | | | | | ASCII CHARACTER | |
|---|---|---|---|---|---|---|
| 5 | 4 | 3 | 2 | 1 | LISTEN | TALK |
| 0 | 0 | 0 | 0 | 0 | SP | @ |
| 0 | 0 | 0 | 0 | 1 | ! | A |
| 0 | 0 | 0 | 1 | 0 | " | B |
| 0 | 0 | 0 | 1 | 1 | # | C |
| 0 | 0 | 1 | 0 | 0 | $ | D |
| 0 | 0 | 1 | 0 | 1 | % | E |
| 0 | 0 | 1 | 1 | 0 | & | F |
| 0 | 0 | 1 | 1 | 1 | ' | G |
| 0 | 1 | 0 | 0 | 0 | ( | H |
| 0 | 1 | 0 | 0 | 1 | ) | I |
| 0 | 1 | 0 | 1 | 0 | * | J |
| 0 | 1 | 0 | 1 | 1 | + | K |
| 0 | 1 | 1 | 0 | 0 | , | L |
| 0 | 1 | 1 | 0 | 1 | - | M |
| 0 | 1 | 1 | 1 | 0 | . | N |
| 0 | 1 | 1 | 1 | 1 | / | O |
| 1 | 0 | 0 | 0 | 0 | 0 | P |
| 1 | 0 | 0 | 0 | 1 | 1 | Q |
| 1 | 0 | 0 | 1 | 0 | 2 | R |
| 1 | 0 | 0 | 1 | 1 | 3 | S |
| 1 | 0 | 1 | 0 | 0 | 4 | T |
| 1 | 0 | 1 | 0 | 1 | 5 | U |
| 1 | 0 | 1 | 1 | 0 | 6 | V |
| 1 | 0 | 1 | 1 | 1 | 7 | W |
| 1 | 1 | 0 | 0 | 0 | 8 | X |
| 1 | 1 | 0 | 0 | 1 | 9 | Y |
| 1 | 1 | 0 | 1 | 0 | : | Z |
| 1 | 1 | 0 | 1 | 1 | ; | [ |
| 1 | 1 | 1 | 0 | 0 | < | / |
| 1 | 1 | 1 | 0 | 1 | = | ] |
| 1 | 1 | 1 | 1 | 0 | > | ∧ |
| ⊕ 1 | 1 | 1 | 1 | 1 | ? | — |

⊕Not to be device assigned. Refer to note.

The IEEE STD-488 Multiline Interface Messages relate to an ASCII code. Table 3-5 provides the IEEE STD-488 DIO bit to ASCII code relationships.

**TABLE 3-5 IEEE STD-488 DIO CODE TO ASCII CHARACTER**

| IEEE STD-488 DIO BIT | | | | | | | ASCII CHARACTER | |
|---|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | LISTEN | TALK |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | SP | |
| 0 | 1 | 0 | 0 | 0 | 0 | 1 | ! | |
| 0 | 1 | 0 | 0 | 0 | 1 | 0 | ” | |
| 0 | 1 | 0 | 0 | 0 | 1 | 1 | # | |
| 0 | 1 | 0 | 0 | 1 | 0 | 0 | $ | |
| 0 | 1 | 0 | 0 | 1 | 0 | 1 | % | |
| 0 | 1 | 0 | 0 | 1 | 1 | 0 | & | |
| 0 | 1 | 0 | 0 | 1 | 1 | 1 | ’ | |
| 0 | 1 | 0 | 1 | 0 | 0 | 0 | ( | |
| 0 | 1 | 0 | 1 | 0 | 0 | 1 | ) | |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | * | |
| 0 | 1 | 0 | 1 | 0 | 1 | 1 | + | |
| 0 | 1 | 0 | 1 | 1 | 0 | 0 | , | |
| 0 | 1 | 0 | 1 | 1 | 0 | 1 | - | |
| 0 | 1 | 0 | 1 | 1 | 1 | 0 | • | |
| 0 | 1 | 0 | 1 | 1 | 1 | 1 | / | |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | |
| 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | |
| 0 | 1 | 1 | 0 | 0 | 1 | 0 | 2 | |
| 0 | 1 | 1 | 0 | 0 | 1 | 1 | 3 | |
| 0 | 1 | 1 | 0 | 1 | 0 | 0 | 4 | |
| 0 | 1 | 1 | 0 | 1 | 0 | 1 | 5 | |
| 0 | 1 | 1 | 0 | 1 | 1 | 0 | 6 | |
| 0 | 1 | 1 | 0 | 1 | 1 | 1 | 7 | |
| 0 | 1 | 1 | 1 | 0 | 0 | 0 | 8 | |
| 0 | 1 | 1 | 1 | 0 | 0 | 1 | 9 | |
| 0 | 1 | 1 | 1 | 0 | 1 | 0 | : | |
| 0 | 1 | 1 | 1 | 0 | 1 | 1 | ; | |
| 0 | 1 | 1 | 1 | 1 | 0 | 0 | < | |
| 0 | 1 | 1 | 1 | 1 | 0 | 1 | = | |
| 0 | 1 | 1 | 1 | 1 | 1 | 0 | > | |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | ? | |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | | @ |
| 1 | 0 | 0 | 0 | 0 | 0 | 1 | | A |
| 1 | 0 | 0 | 0 | 0 | 1 | 0 | | B |
| 1 | 0 | 0 | 0 | 0 | 1 | 1 | | C |
| 1 | 0 | 0 | 0 | 1 | 0 | 0 | | D |
| 1 | 0 | 0 | 0 | 1 | 0 | 1 | | E |
| 1 | 0 | 0 | 0 | 1 | 1 | 0 | | F |
| 1 | 0 | 0 | 0 | 1 | 1 | 1 | | G |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 | | H |
| 1 | 0 | 0 | 1 | 0 | 0 | 1 | | I |
| 1 | 0 | 0 | 1 | 0 | 1 | 0 | | J |
| 1 | 0 | 0 | 1 | 0 | 1 | 1 | | K |
| 1 | 0 | 0 | 1 | 1 | 0 | 0 | | L |
| 1 | 0 | 0 | 1 | 1 | 0 | 1 | | M |
| 1 | 0 | 0 | 1 | 1 | 1 | 0 | | N |
| 1 | 0 | 0 | 1 | 1 | 1 | 1 | | O |
| 1 | 0 | 1 | 0 | 0 | 0 | 0 | | P |
| 1 | 0 | 1 | 0 | 0 | 0 | 1 | | Q |
| 1 | 0 | 1 | 0 | 0 | 1 | 0 | | R |
| 1 | 0 | 1 | 0 | 0 | 1 | 1 | | S |
| 1 | 0 | 1 | 0 | 1 | 0 | 0 | | T |
| 1 | 0 | 1 | 0 | 1 | 0 | 1 | | U |
| 1 | 0 | 1 | 0 | 1 | 1 | 0 | | V |
| 1 | 0 | 1 | 0 | 1 | 1 | 1 | | W |
| 1 | 0 | 1 | 1 | 0 | 0 | 0 | | X |
| 1 | 0 | 1 | 1 | 0 | 0 | 1 | | Y |
| 1 | 0 | 1 | 1 | 0 | 1 | 0 | | Z |
| 1 | 0 | 1 | 1 | 0 | 1 | 1 | | [ |
| 1 | 0 | 1 | 1 | 1 | 0 | 0 | | \ |
| 1 | 0 | 1 | 1 | 1 | 0 | 1 | | ] |
| 1 | 0 | 1 | 1 | 1 | 1 | 0 | | ⌢ |
| 1 | 0 | 1 | 1 | 1 | 1 | 1 | | _ |

The Counter can be programmed by sending device dependent messages during the Counters Listen mode of operation. Device independent commands are received by the Frequency Counter at any time during it's operation. The Counter will ignore any device dependent or independent command for which it has not been desiged or programmed to respond to.

The device dependent data is progrmmed into the Counter in serial bytes consisting of 7-parallel bits. Table 3-6 provides the Program Format of the 6054B Counter.

*NOTE*
*All MODE selections must be followed by a RESET to ensure entry.*

The Model 6054B Counter outputs the measurement data when in it's talk mode in a 16-byte, 7-bit format in a byte serial, bit parallel sequence. TAble 3-7 provides the data output sequence as it relates to the data output format and equivalent ASCII Characters.

TABLE 3-6 IEEE STD-488 PROGRAM FORMAT

| BYTE | PROGRAM BITS 7 6 5 4 3 2 1 | ASCII CHARACTER | FUNCTION | GROUP |
|---|---|---|---|---|
| 1 | 1 0 0 0 0 0 0 | @ | 1 MHz | Resolution Selections |
| | 1 0 0 0 0 0 1 | A | 1 MHz | |
| | 1 0 0 0 0 1 0 | B | 100 kHz | |
| | 1 0 0 0 0 1 1 | C | 10 kHz | |
| | 1 0 0 0 1 0 0 | D | 1 kHz | |
| | 1 0 0 0 1 0 1 | E | 100 Hz | |
| | 1 0 0 0 1 1 0 | F | 10 Hz | |
| | *1 0 0 0 1 1 1 | G | 1 Hz | |
| 2 | 1 0 0 1 0 0 0 | H | Wide | Mode Selection |
| | 1 0 0 1 1 1 1 | O | Reset | |
| | *1 0 0 1 0 0 1 | I | Normal | |
| | 1 0 0 1 1 1 1 | O | Reset | |
| | 1 0 0 1 0 1 0 | J | Low | |
| | 1 0 0 1 1 1 1 | O | Reset | |
| | 1 0 0 1 0 1 1 | K | Test | |
| | 1 0 0 1 1 1 1 | O | Reset | |
| 3 | *1 0 0 1 1 0 0 | L | Hold | Control |
| | 1 0 0 1 1 0 1 | M | Recycle | |
| | 1 0 0 1 1 1 0 | N | Sample | |
| | 1 0 0 1 1 1 1 | O | Reset | |
| 4 | *1 0 1 0 0 0 0 | P | No Offset | Positive Offsets |
| | 1 0 1 0 0 0 1 | Q | Offset | |
| | 1 0 1 0 0 1 0 | R | Offset | |
| | 1 0 1 0 0 1 1 | S | Offset | |
| | 1 0 1 0 1 0 0 | T | Offset | |
| | 1 0 1 0 1 0 1 | U | Offset | |
| | 1 0 1 0 1 1 0 | V | Offset | |
| | 1 0 1 0 1 1 1 | W | Offset | |
| | 1 0 1 1 0 0 0 | X | Offset | Negative Offsets |
| | 1 0 1 1 0 0 1 | Y | Offset | |
| | 1 0 1 1 0 1 0 | Z | Offset | |
| | 1 0 1 1 0 1 1 | [ | Offset | |
| | 1 0 1 1 1 0 0 | / | Offset | |
| | 1 0 1 1 1 0 1 | ] | Offset | |
| | 1 0 1 1 1 1 0 | — | Offset | |
| | 1 0 1 1 1 1 1 | – | Offset | |

*Wake up states

TABLE 3-7 GPIB OUTPUT DATA FORMAT

| BYTE | BIT 7 | 6 | 5 | 4 | 3 | 2 | 1 | ASCII CHARACTER | DATA FUNCTION |
|---|---|---|---|---|---|---|---|---|---|
| 1 | 0 | 1 | 1 | X | X | X | X | 0 → 9 | $10^{10}$ Digit MSD |
| 2 | 0 | 1 | 1 | X | X | X | X | 0 → 9 | $10^9$ Digit |
| 3 | 0 | 1 | 1 | X | X | X | X | 0 → 9 | $10^8$ Digit |
| 4 | 0 | 1 | 1 | X | X | X | X | 0 → 9 | $10^7$ Digit |
| 5 | 0 | 1 | 1 | X | X | X | X | 0 → 9 | $10^6$ Digit |
| 6 | 0 | 1 | 1 | X | X | X | X | 0 → 9 | $10^5$ Digit |
| 7 | 0 | 1 | 1 | X | X | X | X | 0 → 9 | $10^4$ Digit |
| 8 | 0 | 1 | 1 | X | X | X | X | 0 → 9 | $10^3$ Digit |
| 9 | 0 | 1 | 1 | X | X | X | X | 0 → 9 | $10^2$ Digit |
| 10 | 0 | 1 | 1 | X | X | X | X | 0 → 9 | $10^1$ Digit |
| 11 | 0 | 1 | 1 | X | X | X | X | 0 → 9 | $10^0$ Digit LSD |
| 12 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | E | Delimiter |
| 13 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | + | Exponent Point |
| 14 | 0 | 1 | 1 | 0 | X | X | X | 0 → 6 | Exponent Value |
| 15 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | CR | Delimiter |
| 16 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | LF | Delimiter |

A typical system is shown in Figure 3-7 to illustrate the capability of the GPIB system to provide a variety of instrumentation system needs.

Two examples of possible event sequences, to accomplish specific measurement tasks using the GPIB system are provided as follows:

Event Sequence 1 (Basic Data Returned to the Controller).

1. Controller initializes the interface system by issuing the IFC command.
2. Controller causes all devices to set their internal conditions to a predefined state by issuing a DCL (device clear) message as an ASCII DC4, (0010100).
3. Controller sends the listen address of the programmable power supply, followed by program data for that device.
4. Controller sends the unlisten command(UNL) as an ASCII?, then the listen address for the next device, followed by the program data for it.
5. Event 4 is repeated until each device of interest for the test has been addressed and programmed, then the controller issues an unlisten command (UNL)
6. Controller sends the listen address of the selected measurement device (for example the

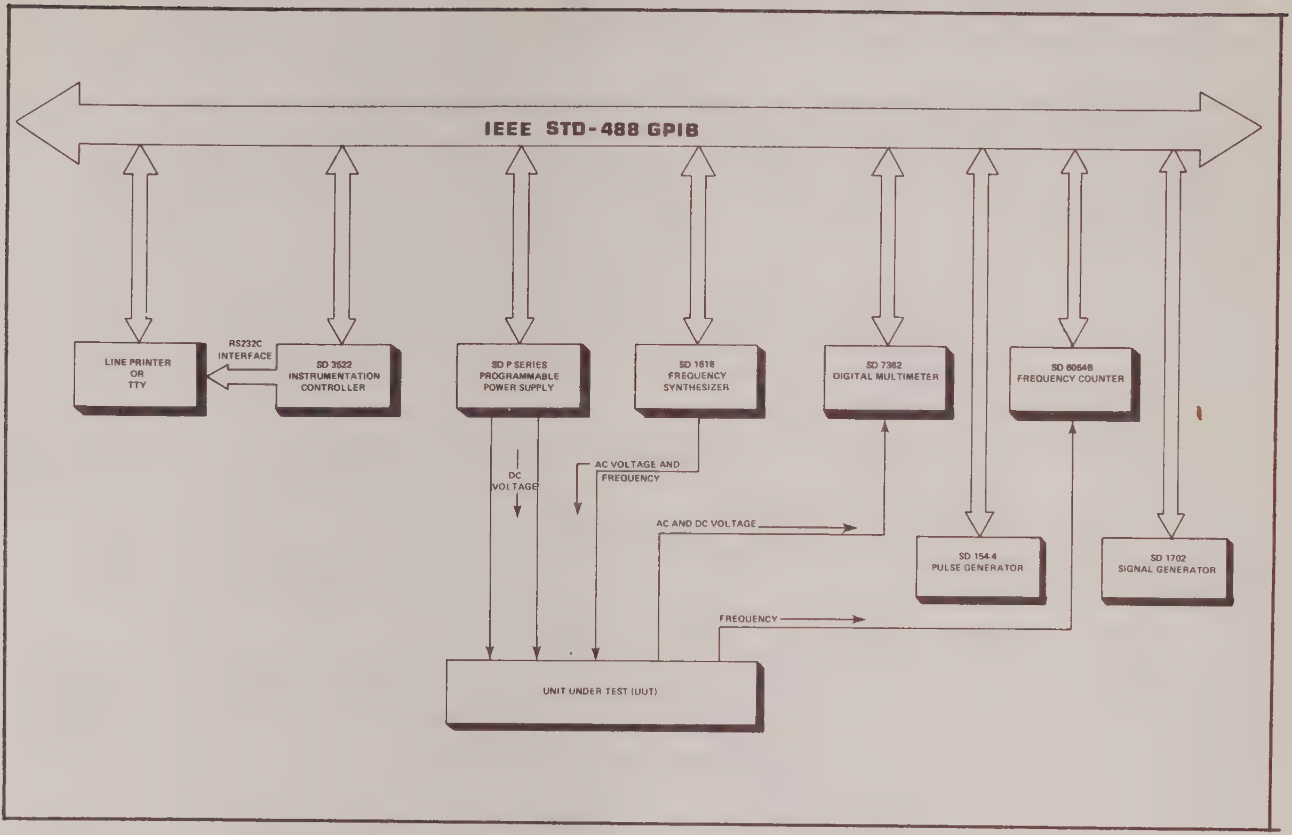

IEEE STD-488 GPIB
LINE PRINTER OR TTY
RS232C INTERFACE
SD 3522 INSTRUMENTATION CONTROLLER
SD P SERIES PROGRAMMABLE POWER SUPPLY
SD 1618 FREQUENCY SYNTHESIZER
SD 7362 DIGITAL MULTIMETER
SD 6054B FREQUENCY COUNTER
DC VOLTAGE
AC VOLTAGE AND FREQUENCY
AC AND DC VOLTAGE
SD 154-4 PULSE GENERATOR
SD 1702 SIGNAL GENERATOR
FREQUENCY
UNIT UNDER TEST (UUT)

FIGURE 3-7 TYPICAL TEST SYSTEM

Model 6054B Frequency Counter), then the program data to initiate a measurement.

7. Controller issues another UNL command, addresses itself to listen, then sends the talk address of the measurement device.
8. Upon completion of its measurement cycle the Frequency Counter enters its talk mode and sends the measurement result (basic data) to the controller that is the addressed listener.
9. The controller displays the measurement data on its CRT or transmits it via the RS232C Interface to the line printer or teletype to generate a "hard copy" of the test results.

Event Sequence 2 (Basic Data Directed to the Line Printer or TTY).

1. Controller initializes the interface system by issuing the IFC command.
2. Controller causes all devices to set their internal conditions to a predefined state by issuing a DCL (device clear) message as an ASCII DC4.
3. Controller sends the listen address of the programmable power supply, followed by program data for that device.
4. Controller sends the unlisten command (UNL) as an ASCII ?. then the listen address for the next device, followed by the program data for it.
5. Event 4 is repeated until each device of interest for the test has been addressed and programmed, then the controller issues an unlisten command (UNL).
6. Controller sends the listen address of the selected measurement device (for example the Model 6054B Frequency Counter), then the program data to initiate a measurement.
7. Controller sends another UNL command,

then the listen address of the line printer or teletype, followed by the talk address of the frequency counter.

8. Upon completion of it's measurement cycle the Frequency Counter enters it's talk mode and sends the measurement result (basic data) to the line printer or teletype.

*NOTE*

*If the controller were to address both the line printer or teletype and itself, the resulting basic data would be accepted by both devices, even though the two may have different transfer rates at which the data can be accepted.*

The Model 6054B Counter may be controlled by a calculator that is IEEE STD-488 compatible. Following are typical examples using the Hewlett Packard HP 9825 calculator as a controller and readout device.

The HP 9825 calculator is connected to the 6054B Frequency Counter via the GPIB cable and the Calculator and Counter are programmed as to their addresses by the rear panel address switches (710 address is used in the following typical examples, 7 being the calculator bus address and 10 being the counter's address in decimal).

Example 1 Configure the counter to the following mode and control functions;

| | |
|---|---|
| Resolution | 1 Hz |
| Mode | NORMAL |
| Control Function | RECYCLE |
| Offset | NO OFFSET |

and generate a display and printout on the calculator of the measurement data in a X.XXXXXXXXXE09 format.

Enter the following sequences via the HP 9825 keyboard and verify the entries on it's printer.

| STEP | ENTRY | FUNCTION |
|---|---|---|
| 0: | 0 → I | Initializes the GPIB and Counter. |
| 1: | rem 710; | Places the Counter into it's MONITOR mode. |
| | wrt 710, "GIMP" | Places the Counter into it's LISTEN mode, and writes ASCII's GIMP into the Counter to program it's mode and control functions as follows;<br>**ASCII** **FUNCTION**<br>G 1 Hz resolution<br>I NORMAL mode<br>M RECYCLE<br>P NO OFFSET |
| 2: | red 710, A; | Places the Counter into it's TALK mode to allow the calculator to read the measurement data. |
| | fxd 8; | Configures the calculator to fix a decimal point in it's eight position. |
| | dsp, A; | Enables the calculator's display. |
| | prt, A; | Enables the calculator's printer. |
| | wait 500 | Delays the readout 500 ms. |

If the readout was 1.260000000E 09, a frequency measurement of 1.260 GHz is indicated with a resolution to 1 Hz.

Example 2 Configure the counter to the following mode and control functions;

| | |
|---|---|
| Resolution | 1 kHz |
| Mode | TEST |
| Control Function | RECYCLE |
| Offset | NO OFFSET |

and generate a printout (no display) on the calculator of the measurement data in a XXXXXXXXXXXE+3 format.

| STEP | ENTRY | FUNCTION |
|---|---|---|
| 0: | 0 → I | Initializes the GPIB and Counter. |
| 1: | rem 710; | Places the Counter into it's MONITOR mode. |
| | wrt 710, "DKOMP" | Places the Counter into it's LISTEN mode, and writes ASCII's DKOMP into the Counter to program it's mode and control functions as follows:<br>**ASCII** **FUNCTION**<br>D 1 kHz resolution<br>K TEST mode<br>O RESET<br>M RECYCLE<br>P NO OFFSET |

| STEP | ENTRY | FUNCTION |
|---|---|---|
| 2: | red 710, A; | Places the Counter into it's TALK mode to allow the calculator to read the measurement data. |
| | prt, A; | Enables the calculator's printer. |
| | wait 500 | Delays the readout 500 ms. |

A readout of 00000001000E+3 will be printed by the calculator indicating a 1 MHz Test mode measurement of the Counter's time base reference oscillator.

The calculator printout shown in Figure 3-8 depicts the commands entered and the frequency measurement readout of a typical program.

Table 3-8 provides the step-by-step sequence of the typical program illustrated in Figure 3-8.

TABLE 3-8 TYPICAL PROGRAM

| PROGRAM STEP | COMMAND | COMMENTS |
|---|---|---|
| 0 | Dimension Calculator | Calculator Bus address 7, Counter address 10. |
| 1 | Write ASCII's DIOMP | 1 kHz,NORMAL,RESET, RECYCLE,NO OFFSET |
| 2 | Read, Display and Print. | Read, Display and Print. |
| 3 | Wait 500; lcl; wait 1000 | Wait 500 ms, go to Local, wait 1000ms. |
| 4 | Write ASCII's GIOMP | 1 Hz,NORMAL,RESET, RECYCLE,NO OFFSET |
| 5 | Read, Display and Print; wait 1500. | Read, Display, Print and wait 1500 ms. |
| 6 | Write DKOMP | 1 kHz,TEST,RESET, RECYCLE,NO OFFSET |
| 7 | Read, Display and Print. | Read, Display and Print. |
| 8 | Write ASCII's FJOMP | 10 Hz,LOW,RESET, RECYCLE,NO OFFSET |
| 9 | Read, Display and Print; wait 500 | Read, Display, Print, and wait 500 ms. |
| 10 | lcl, wait 1000 | Go to Local, wait 1000 ms. |
| 11 | Space, go to Step 1 | Space, go to Step 1, #6185 locations left. |

```
 0:  dim A$[150]
 1:  wrt 710,"DIOMP"
 2:  red 710,A$;dsp A$;prt A$
 3:  wait 500; lcl 710;wait 1000
 4:  wrt 710,"GIOMP"
 5.  red 710,A$;dsp A$;prt A$;wait 500
 6:  wrt 710,"DKOMP",wait 500
 7:  red 710,A$;dsp A$;prt A$;wait 1500
 8:  wrt 710, "FJOMP"
 9:  red 710,A$;dsp A$;prt A$;wait 500
10:  lcl 710;wait 1000
11:  spc ;gto 1
*6185

00003894921E+3
03894917479E+0
00000001000E+3
00000097463E+1
00003894917E+3
```

FIGURE 3-8
TYPICAL CALCULATOR PRINTOUT

The printout (last five lines on Figure 3-8) indicates the following frequency measurements assuming that 974.63 kHz is applied to J2 (20 Hz -20 MHz input) and 3894.917479 MHz is applied to J1 (20 MHz - 24 GHz input).

389421 x $10^3$ Hz
3894917479 x 0 Hz
1000 x $10^3$ Hz
97463 x $10^1$ Hz
38942 x $10^3$ Hz

## 3.8 RECEIVING INSPECTION TEST

1. Ensure the MAIN POWER selection switch is set to the correct available line voltage and the proper fuse is installed.

2. Set the INT/EXT switch on the rear panel to INT.

3. Turn power on, least significant digit should indicate a zero, depending on resolution.

4. Momentarily depress TEST/LAMP switch. Readout should show all eights, and all other indicators should light.

5. Depress TEST/INSTR switch. Counter will count internal 1 MHz frequency to resolution selected.

| RESOLUTION SWITCH POSITION | DISPLAY READING | ANNUNCIATOR READING |
|---|---|---|
| 1 MHz | 1. ±1 | MHz |
| 0.1 MHz | 1.0 ±1 | MHz |
| 10 kHz | 1.00 ±1 | MHz |
| 1 kHz | 1000. ±1 | kHz |
| 0.1 kHz | 1000.0 ±1 | kHz |
| 10 Hz | 1000.00 ±1 | kHz |
| 1 Hz | 1000.000 ±1 | kHz |

6. The instrument should automatically reset each time the RESOLUTION switch is stepped.

7. Momentarily depress the RESET switch, observe the gate light goes out.

## 3.9 EMERGENCY OPERATION

No emergency operational functions are provided in the design of the counter to allow operation under emergency operation procedures relating to the Model 6054B Counter would be at the system level.

### 3.9.1 Operation Under Adverse Conditions

Two functional modes are provided in the 20 MHz to 24 GHz frequency range.

WIDE (ACTO)
NORMAL (FLACTO)

The WIDE Mode should be utilized for measuring signals having low modulation rates and high deviation limits. Communications channels with broad deviation limits, signals which are drifting rapidly, and signals from a sweeping source are examples of WIDE mode utilization.

The NORMAL Mode is utilized to provide high resolution (up to 1 Hz) of stable frequency sources, ($\leqslant$10 MHz deviation) such as signals from microwave synthesizers, multiplexed signal sources and frequency sources which are phase locked to high stability references.

# CHAPTER 4

# PRINCIPLES OF OPERATION

## 4.1 INTRODUCTION

This chapter contains a general description of the Model 6054B Frequency Counter, followed by descriptions of the assemblies within the counter. References are made to schematic diagrams contained in chapter 6.

## 4.2 FUNCTIONAL DESCRIPTION

The Model 6054B Frequency Counter is designed in three functional groups: the Conversion Group, Indication Group and Control Group. (See figure 4-1) Input frequencies in the 20 Hz to 20 MHz range are measured in the conventional manner. The unknown frequency is applied to the low frequency input port (20 Hz - 20 MHz) and the number of zero crossings are accumulated for a known time period. The output indication is displayed as frequency in the correct units dependent upon the selected resolution. When input frequencies in the 20 MHz to 24 GHz range are applied to the microwave input port, the counter automatically decides whether to make direct measurement or to go into a conversion mode. If the signal frequency is less than 500 MHz, a direct measurement is made of the zero crossings, similar to that in low frequency measurement. For signals over 500 MHz, the instrument automatically converts the input to a lower frequency signal which is harmonically related to the unknown input signal.

Two functional modes of operation are available for the 500 MHz to 24 GHz range. The first mode, wideband operation, measures signals with low modulation rates at high deviation limits. The second mode provides high resolutions (1 Hz/1s) from relatively stable frequency sources.

## 4.3 CONVERSION GROUP

The Conversion Group includes four measurement techniques:

a. Low Frequency Direct.

b. Direct to 500 MHz.

c. Wide ACTO.

d. Normal FLACTO.

## 4.4 LOW FREQUENCY DIRECT

In the low frequency mode, the counter has a high impedance input amplifier/shaper. (see figure 4-2) When supplied with an input signal from .02 to 20 MHz at an amplitude of at least 10 mV, the signal is amplified and shaped into a TTL-compatible signal. The amplifier limits cleanly at all input levels. In addition, clamping diodes protect the input when the input voltage level exceeds 10V peak-to-peak. The result is an extremely large

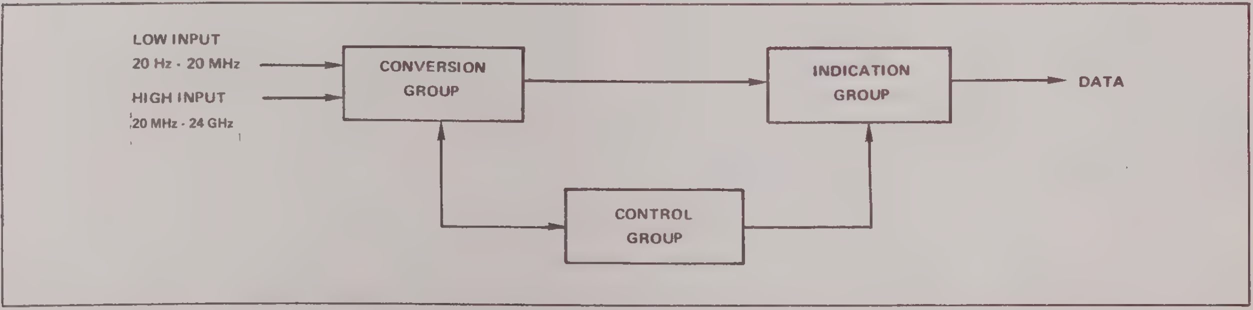


FIGURE 4-1 MODEL 6054B FREQUENCY COUNTER, FUNCTIONAL BLOCK DIAGRAM

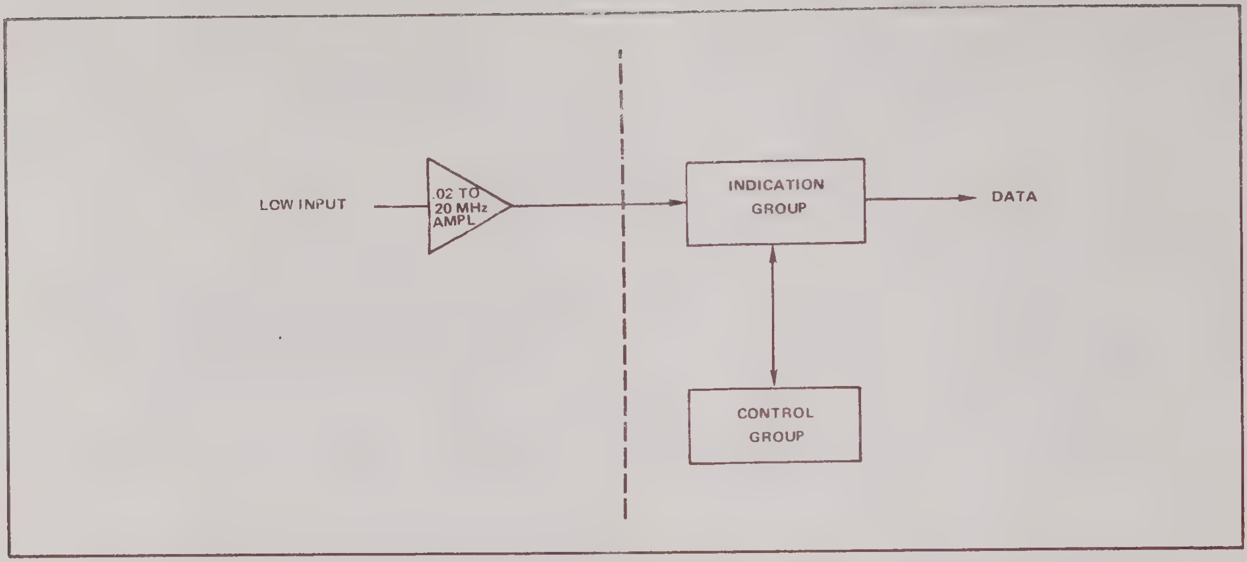


FIGURE 4-2 LOW FREQUENCY DIRECT CONVERSION TECHNIQUE

dynamic range amplifier/shaper without the use of attenuators. The measurement time period and frequency (resolution) are selected in decade steps from 1 μsec (1 MHz) to 1s (1 Hz).

## 4.5 DIRECT TO 500 MHz

When the 20 MHz to 24 GHz wide- or narrow-band operation is selected and a frequency at 500 MHz or lower is applied to the high frequency input connector, the counter measures the input directly using conventional digital techniques. (See figure 4-3). The input frequency is measured and displayed directly, requiring no frequency conversions. When an unknown signal, 500 MHz or below, is applied to the input, the frequency is detected in the 500 MHz amplifier and decade assembly. The detected dc level enables the 500 MHz decade to count the input frequency directly rather than counting the FLACTO local oscillator. Also, the detected level turns off the local oscillator drive to the FLACTO mixers, and disables the N computer and permits the time-base to be normal. (Normal is 1 μsec to 1 second divided in decade steps). The instrument now operates as a direct reading counter up to 500 MHz.

## 4.6 WIDE ACTO

In the wideband mode of operation, the counter is a frequency-locked ACTO which consists of two basic signal channels, the Lock channel and the N channel. (See figure 4-4). A resistive wideband power splitter divides and applies the RF input signal equally to the two channels. An RF leveling system prevents high power RF signals from damaging the sensitive mixers. One output of the power splitter provides an input to the Lock mixer. A local oscillator drives a second input of the mixer where harmonics higher than 24 GHz are generated The output of the Lock mixer is amplified in a 30 MHz IF amplifier, which has a bandwidth of 10 MHz. The output of the 30 MHz IF amplifier drives a frequency discriminator. When the IF signal present is large enough to develop a squelch-enabling voltage, the output of the discriminator is connected to the search oscillator where it is amplified and used as a tuning voltage for the Local Oscillator. The loop gain is very high and, therefore, maintains the IF signal at a frequency very near 30 MHz.

The second output from the power splitter provides

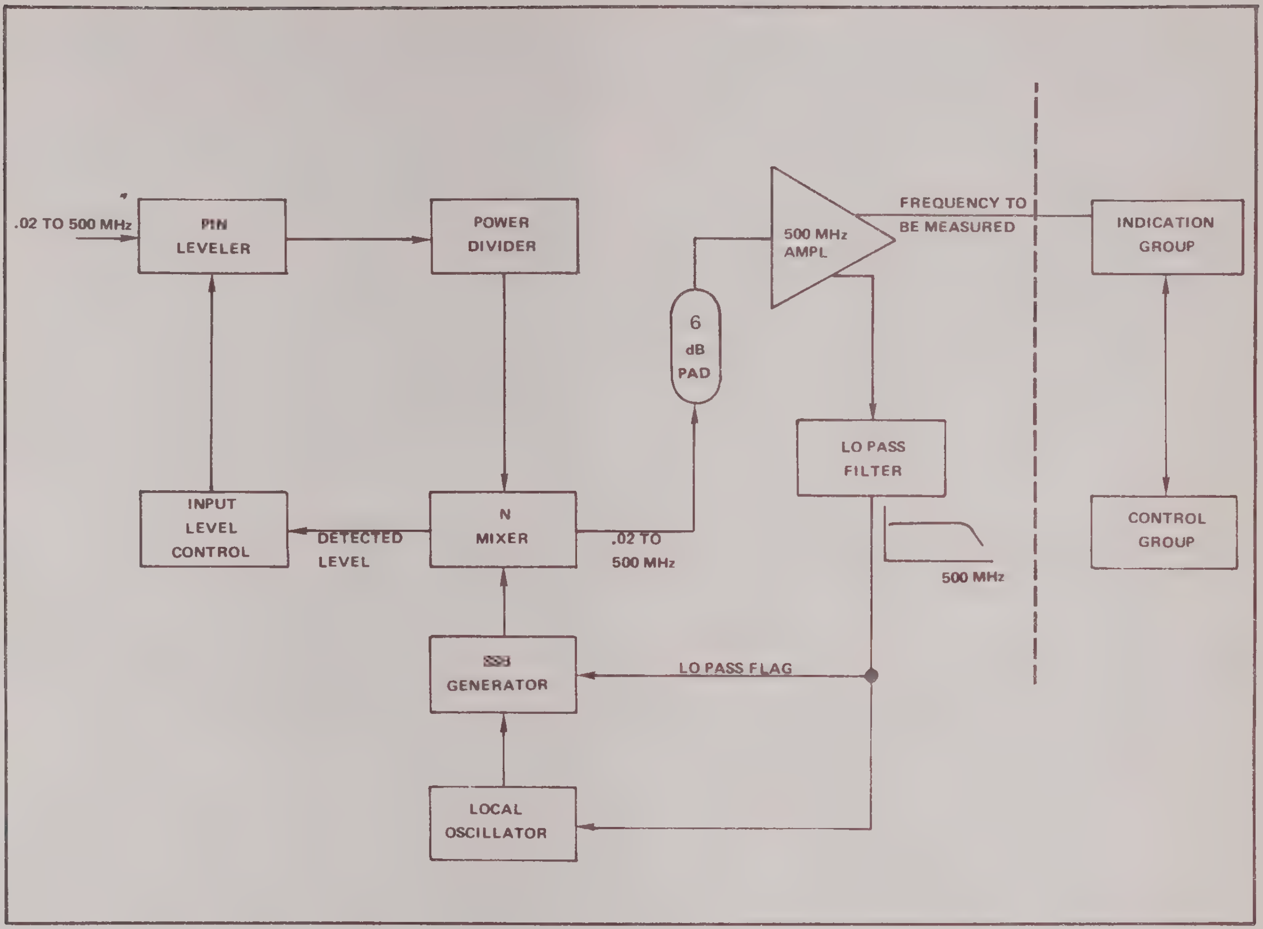

.02 TO 500 MHz
PIN LEVELER
POWER DIVIDER
500 MHz AMPL
FREQUENCY TO BE MEASURED
INDICATION GROUP
6 dB PAD
LO PASS FILTER
500 MHz
INPUT LEVEL CONTROL
DETECTED LEVEL
N MIXER
.02 TO 500 MHz
CONTROL GROUP
SSB GENERATOR
LO PASS FLAG
LOCAL OSCILLATOR

FIGURE 4-3 DIRECT TO 500 MHz CONVERSION METHOD

an input to the N mixer. A second input to the N Mixer is one kHz higher than the local oscillator (LO) frequency from the LO. This frequency is obtained by using a second output from the local oscillator and modulating it with 1 kHz in a single sideband (SSB) generator (shifter). The carrier and one sideband are nulled in the SSB generator, leaving only the upper sideband which results in a 1 kHz shift. The output of the N mixer is amplified by a 30 MHz IF amplifier which has a bandwidth of 10 MHz. Since the same RF signal is applied to both mixers, the mixers use the same harmonic number N.

To obtain the frequency N X 1 kHz, an output signal of the lock IF is mixer with the N IF. This frequency is compared digitally with the original 1 kHz in the control section and the harmonic number N is extracted. The local oscillator is now counted in the 500 MHz counter. Then, this frequency is multiplied by the harmonic number N. At the same time the lock IF is also measured. The N X LO and the Lock IF are added and displayed in the front panel LED Display as a direct indication of the input RF signal.

An assumption was made that a frequency lock had been obtained, which is not always true when an RF signal is applied. In the absence of an input signal the search oscillator is sweeping the local oscillator over a frequency range wide enough that one or more harmonics are capable of mixing with the input frequency to produce a 30 MHz IF signal. When a harmonic of the LO mixer with an input frequency of sufficient amplitude and produces the 30 MHz IF signal, a squench is developed. The presence of a squelch signal permits the discriminator output to override the search oscillator, which now becomes an amplifier and controls the frequency of the LO. The AFC action takes control and the system becomes frequency locked. Since the input to the counter is sideband, image frequencies are not rejected. These frequencies will mix with the LO signal and be amplified by the IF amplifier to produce a squelch signal. When this condition arises, the slope of the discriminator will be wrong. Instead of locking at the center of the S curve, the discriminator will attempt to lock at the extreme end of the curve, and be out of range of the squelch detector. Squelch will then be lost and the discriminator will immediately try again to lock to the same signal. The result is an oscillation. A detector in the control circuitry detects presence of this oscillation and forces the FLACTO to ignore this unallowable frequency lock and search for a new frequency.

## 4.7 NORMAL FLACTO

The normal-band mode of operation begins similar to that of the wideband mode of operation. (see figure 4-5). The FLACTO will search and lock on

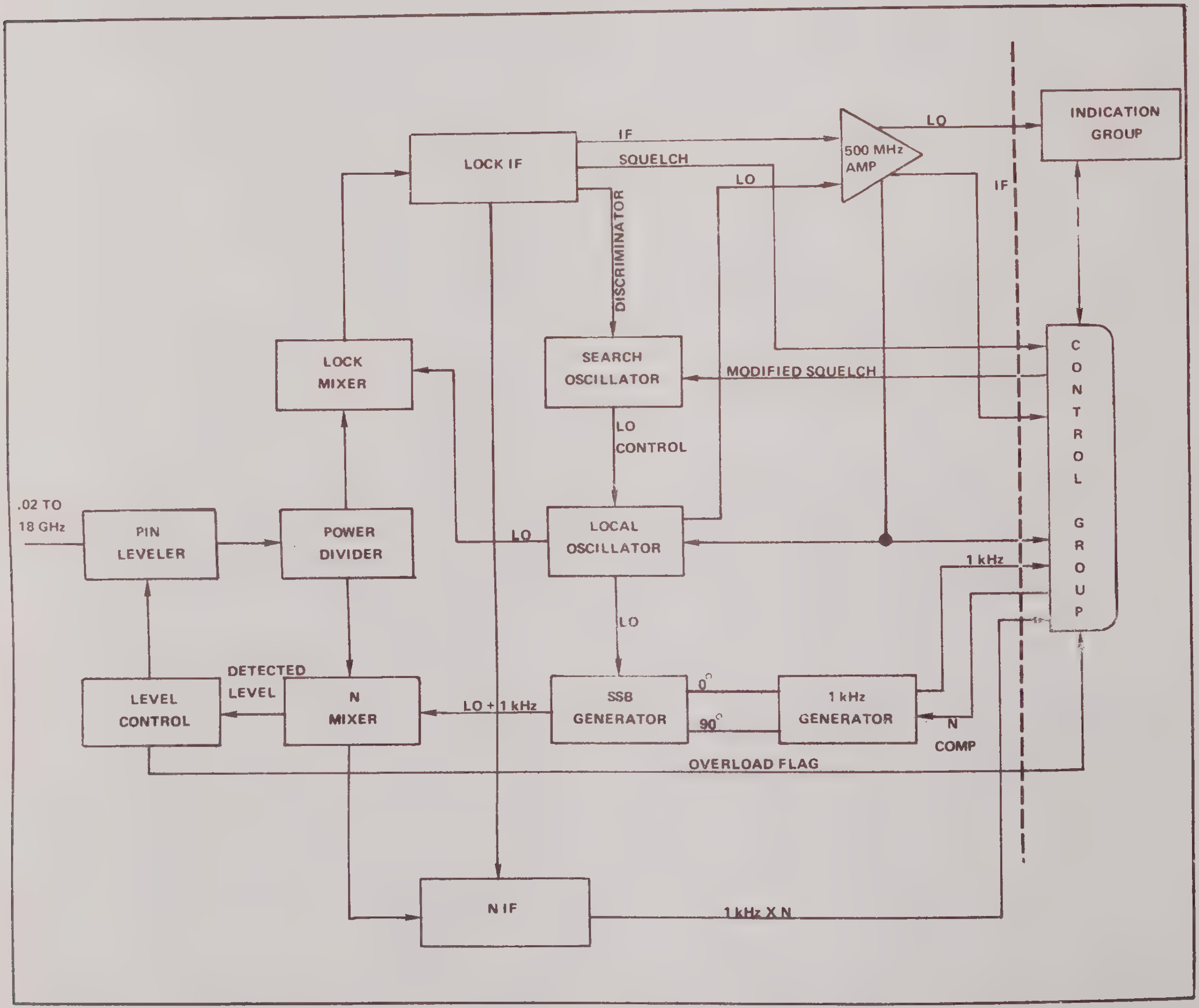

INDICATION GROUP
LO
IF
SQUELCH
LOCK IF
500 MHz AMP
LO
IF
DISCRIMINATOR
LOCK MIXER
SEARCH OSCILLATOR
MODIFIED SQUELCH
C O N T R O L G R O U P
LO CONTROL
.02 TO 18 GHz
PIN LEVELER
POWER DIVIDER
LO
LOCAL OSCILLATOR
1 kHz
LO
DETECTED LEVEL
LEVEL CONTROL
N MIXER
LO + 1 kHz
SSB GENERATOR
0°
90°
1 kHz GENERATOR
N COMP
OVERLOAD FLAG
N IF
1 kHz X N

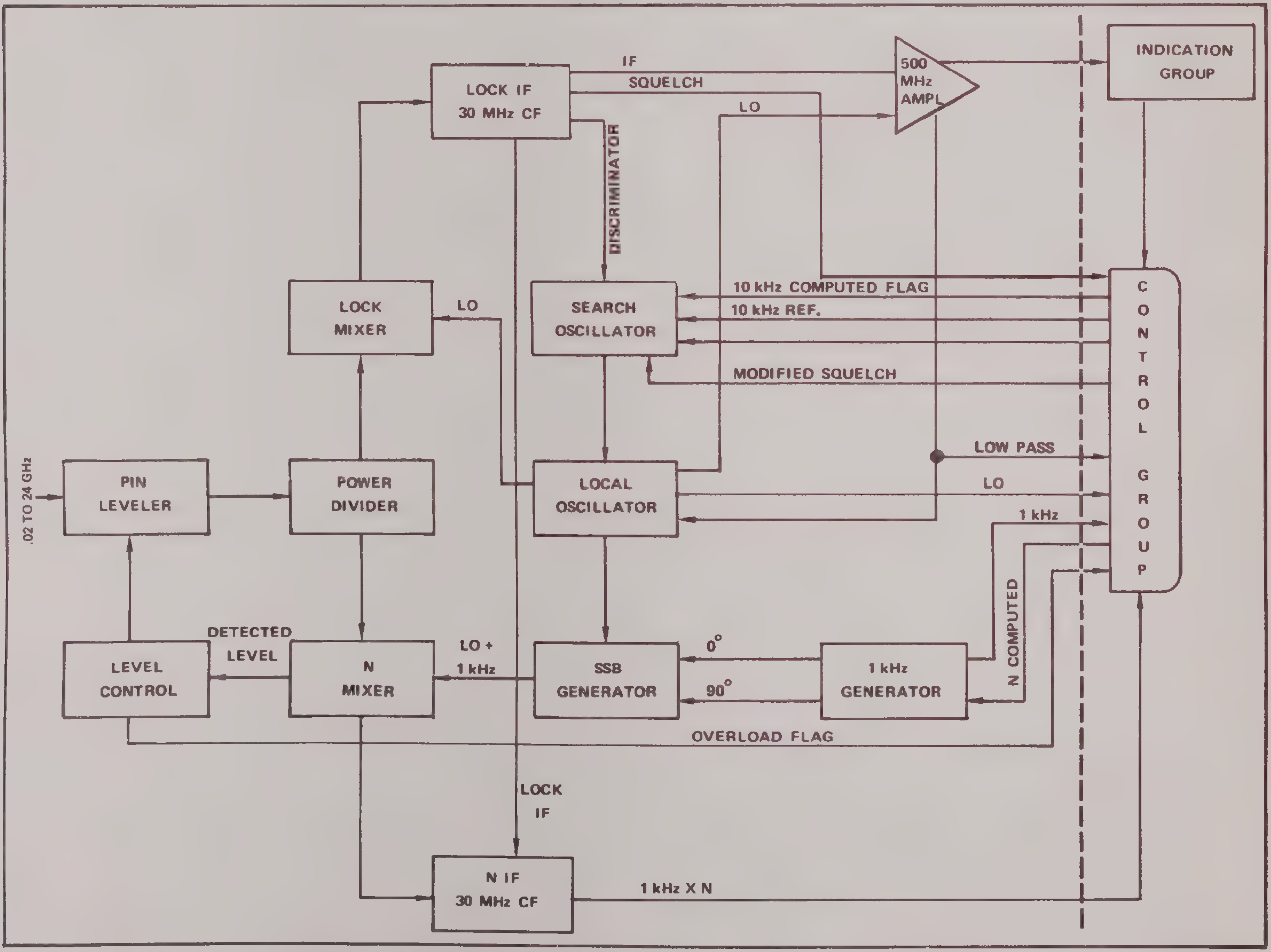
FIGURE 4-4 WIDE ACTO CONVERSION METHOD

to the RF input frequency and the harmonic number N will be computed. In the narrowband mode, the LO will no longer remain frequency locked to the RF input signal, but will be phase locked to a particular 10 kHz X harmonic number N. Since the LO is now controlled by a reference within the instrument, it will be as precise as the crystal reference oscillator in the counter and the LO frequency is no longer measured each time a frequency is counted. Only the IF signal is measured. The LO output will be digitally multiplied by N to which the IF signal is digitally added. Using this technique, it is possible to measure a frequency with a resolution of 1 Hz within a one second measuring period.

When phase-locked, the LO must be locked to a particular 10 kHz frequency increment. To ensure that the correct 10 kHz increment is selected, the LO frequency is first measured then stored in the binary counter in the Control Group. A binary-coded representation of the LO frequency programs a divide-by-M counter to a number which when activated by the LO frequency will produce a frequency near 10 kHz. Next, this divide-by-M frequency will be phase compared to 10 kHz. A dc voltage resulting from this phase comparison will now control the LO frequency, locking it to 10 kHz times the number programmed into the divide-by-M counter.

## 4.8 INDICATION GROUP

The Indication Group consists of an 11-digit storage/accumulation chain, and 11-digit accumulator, and a 40-bit shift register. Also, this group includes signal gates which route the information



INDICATION GROUP
IF
SQUELCH
LO
500 MHz AMPL
LOCK IF 30 MHz CF
DISCRIMINATOR
LOCK MIXER
LO
SEARCH OSCILLATOR
10 kHz COMPUTED FLAG
10 kHz REF.
MODIFIED SQUELCH
C O N T R O L G R O U P
LOW PASS
LO
1 kHz
.02 TO 24 GHz
PIN LEVELER
POWER DIVIDER
LOCAL OSCILLATOR
N COMPUTED
DETECTED LEVEL
LEVEL CONTROL
N MIXER
LO + 1 kHz
SSB GENERATOR
0°
90°
1 kHz GENERATOR
OVERLOAD FLAG
LOCK IF
N IF 30 MHz CF
1 kHz X N

FIGURE 4-5 NORMAL FLACTO CONVERSION METHOD

to the proper accumulator for the selected function, contains the visual display, and provides BCD output data.

## 4.9 DIRECT TO 500 MHz OPERATION

The selected low-frequency information is passed through a signal gate which is active for a time selected by the resolution switch. At the end of the gate time, the information is transferred to storage. The storage register drives an 11-digit LED readout and the parallel BCD output buffers. The information in storage is updated at the end of each gate period. (see figure 4-6).

## 4-10 WIDEBAND OPERATION

When a frequency greater than 500 MHz is to be measured, the storage register performs two functions. (see figure 4-7) The accumulator counts each zero crossing of the LO for a period of (1/R) N. Data is transferred to storage at the end of the measuring period, and the IF signal is measured during this same period. A frequency representing IF, which is stored in the control group is clocked into the storage register. The result is that the LO frequency is measured for the period which represents the selected resolution, times the computed harmonic number. The IF signal is divided by the harmonic number and measured during the same time period, then added directly to the store a LO frequency in four serial bytes. The Data Ready signal then indicates that the data on the BCD bus is valid.

## 4.11 NARROWBAND OPERATION

For maximum resolution in the shortest measuring period, stable frequencies above 500 MHz can be measured in the narrow mode. A 44-bit shift register is added to the Indication Group to shift the most significant digits, to 10 kHz resolution. (see figure 4-8) Two frequencies are measured to produce the complete answer. The LO frequency is measured for the time N X 1 millisecond. This number is then transferred to the shift register which shifts the correct number of bits to correctly place the most significant digit. The data, correctly located, is then shifted back into the accumulator. The IF signal is then measured for the time 1/R directly into the accumulator. The summed data is then transferred to storage, the accumulator is reset and the LO X 1 kHz X N R/1 kHz signal is again transferred to the accumulator from the shift register.

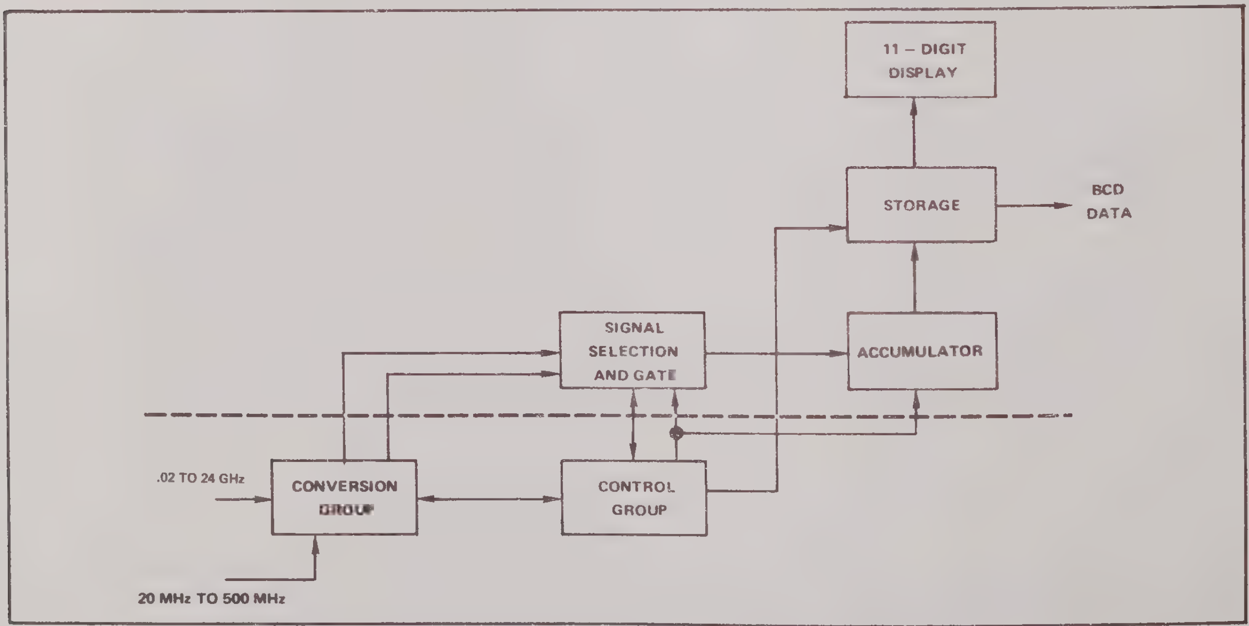


FIGURE 4-6 DIRECT COUNT, INDICATION GROUP

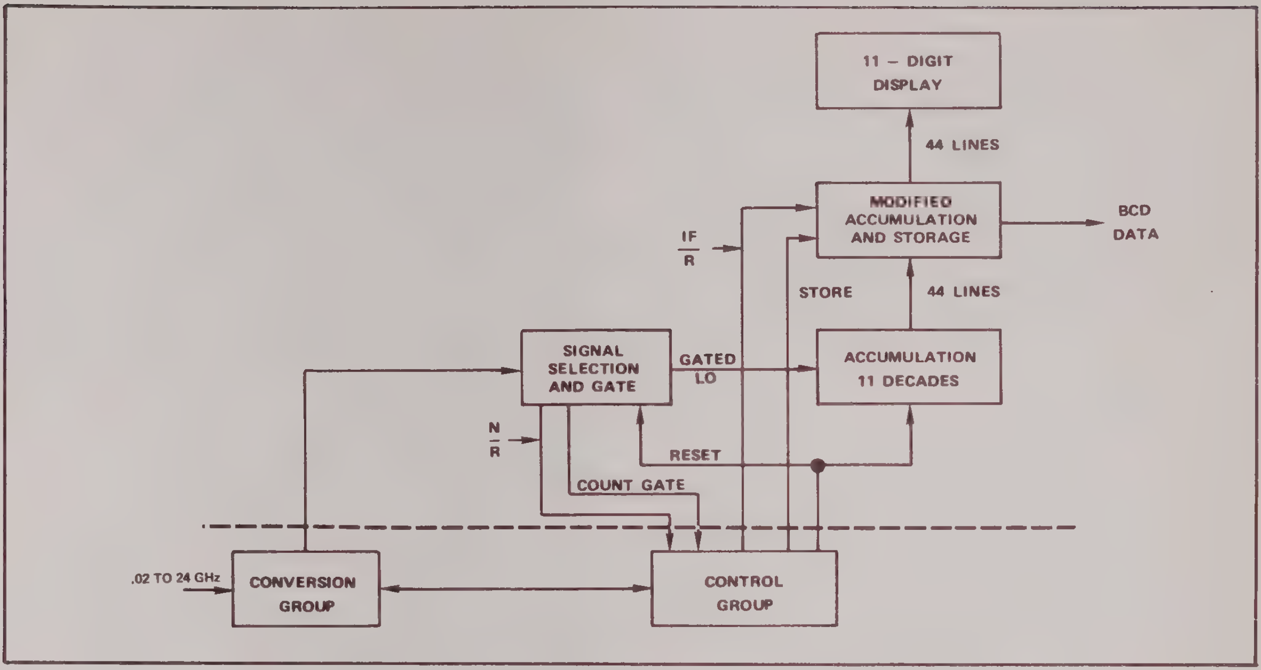
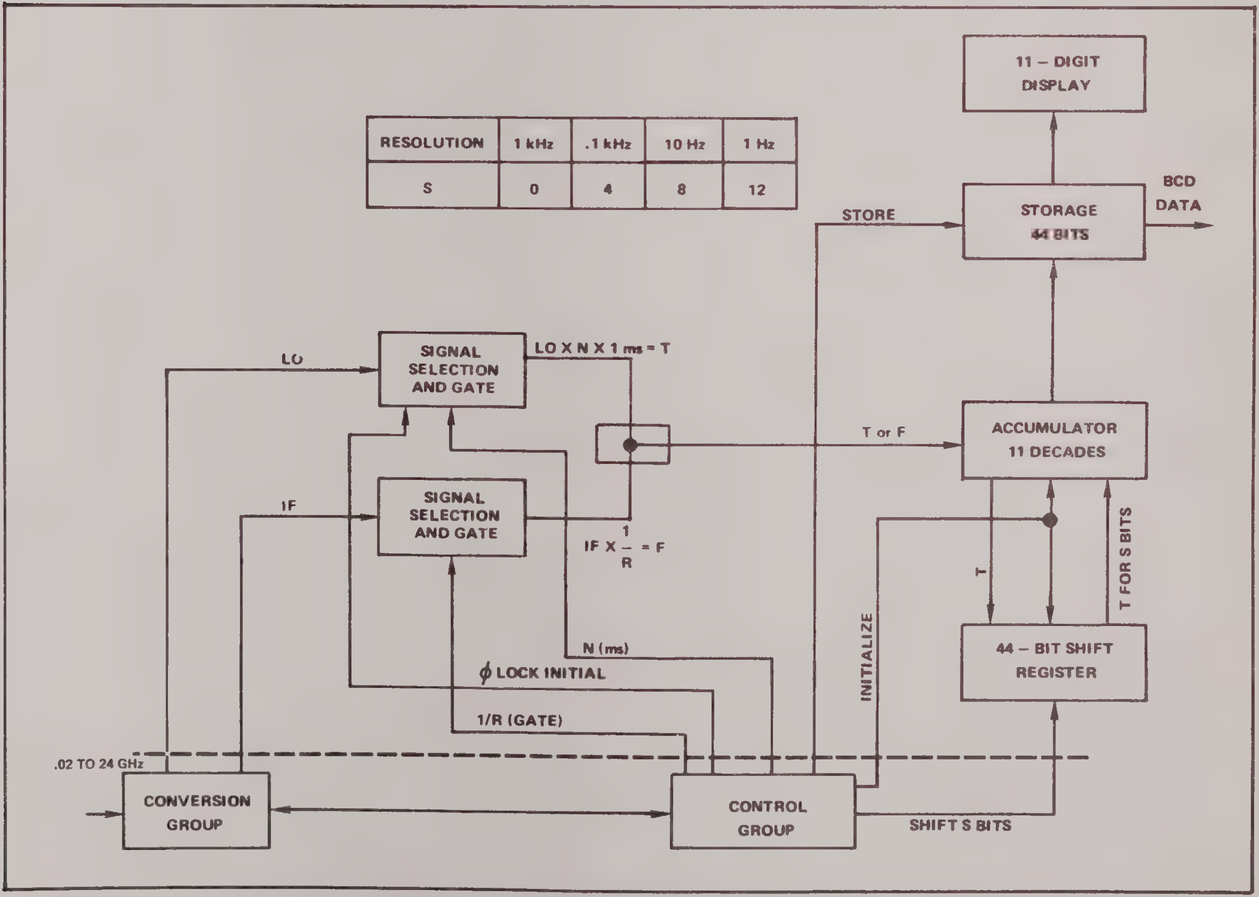

11 – DIGIT DISPLAY
44 LINES
MODIFIED ACCUMULATION AND STORAGE
BCD DATA
IF/R
STORE
44 LINES
SIGNAL SELECTION AND GATE
GATED LO
ACCUMULATION 11 DECADES
N/R
RESET
COUNT GATE
.02 TO 24 GHz
CONVERSION GROUP
CONTROL GROUP

FIGURE 4-7 WIDEBAND OPERATION, INDICATION GROUP



| RESOLUTION | 1 kHz | .1 kHz | 10 Hz | 1 Hz |
|---|---|---|---|---|
| S | 0 | 4 | 8 | 12 |

11 – DIGIT DISPLAY
BCD DATA
STORE
STORAGE 44 BITS
LO
SIGNAL SELECTION AND GATE
LO X N X 1 ms = T
T or F
ACCUMULATOR 11 DECADES
IF
SIGNAL SELECTION AND GATE
IF X 1/R = F
T
T FOR S BITS
INITIALIZE
N (ms)
44 – BIT SHIFT REGISTER
ϕ LOCK INITIAL
1/R (GATE)
.02 TO 24 GHz
CONVERSION GROUP
CONTROL GROUP
SHIFT S BITS

FIGURE 4-8 NARROWBAND OPERATION, INDICATION GROUP

## 4.12 CONTROL GROUP

The Control Group contains the circuitry required for digital manipulation, instrument event timing and the frequency standard to which all frequency measurements are compared. The circuitry includes the frequency reference, time base selection, time base modification, N computation, 10 kHz generator (LO/M), IF integrator N X (IF/N) and various timing and flag-generating circuitry.

## 4.13 DIRECT TO 500 MHz OPERATION

When the flag from the Conversion Group indicates that a frequency of less than 500 MHz is present, the Control Group is configured as a conventional frequency meter. (see figure 4-9) The resolution switch controls the selection of the time base division ratio in decade steps. The selected time base period toggles a binary, which controls the signal gate in the Indication Group. When the end of count flag is received from the Indication Group, a transfer signal is initiated which moves the data from the accumulators to storage. At the same time, the recycle rate generator is activated to run for a time set by the recycle rate front panel control. At the expiration of that time the reset generators are activated to set the initial or start conditions. The cycle then repeats. Any change to any front panel controls will set the instrument to initial conditions.

## 4.14 WIDE ACTO OPERATION

When a Signal Present/High Pass Flag is received from the Conversion Group, and the wideband mode of operation is selected, additional control circuitry is activated. (see figure 4-10) The

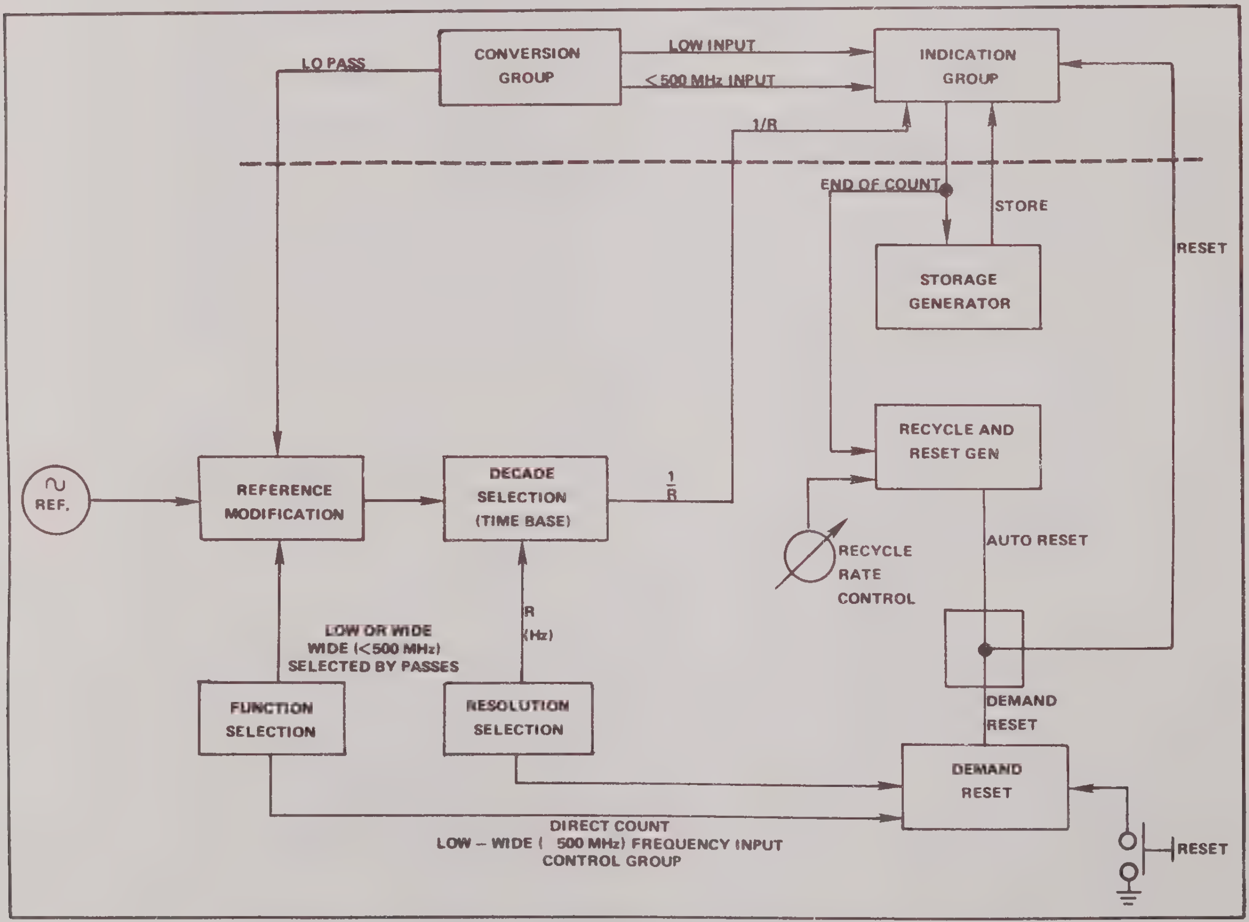

CONVERSION GROUP
LO PASS
LOW INPUT
< 500 MHz INPUT
INDICATION GROUP
1/R
END OF COUNT
STORE
RESET
STORAGE GENERATOR
RECYCLE AND RESET GEN
REF.
REFERENCE MODIFICATION
DECADE SELECTION (TIME BASE)
1/R
RECYCLE RATE CONTROL
AUTO RESET
R (Hz)
LOW OR WIDE
WIDE (<500 MHz)
SELECTED BY PASSES
FUNCTION SELECTION
RESOLUTION SELECTION
DEMAND RESET
DEMAND RESET
RESET
DIRECT COUNT
LOW – WIDE ( 500 MHz) FREQUENCY INPUT
CONTROL GROUP

FIGURE 4-9 DIRECT COUNT OPERATION, CONTROL GROUP

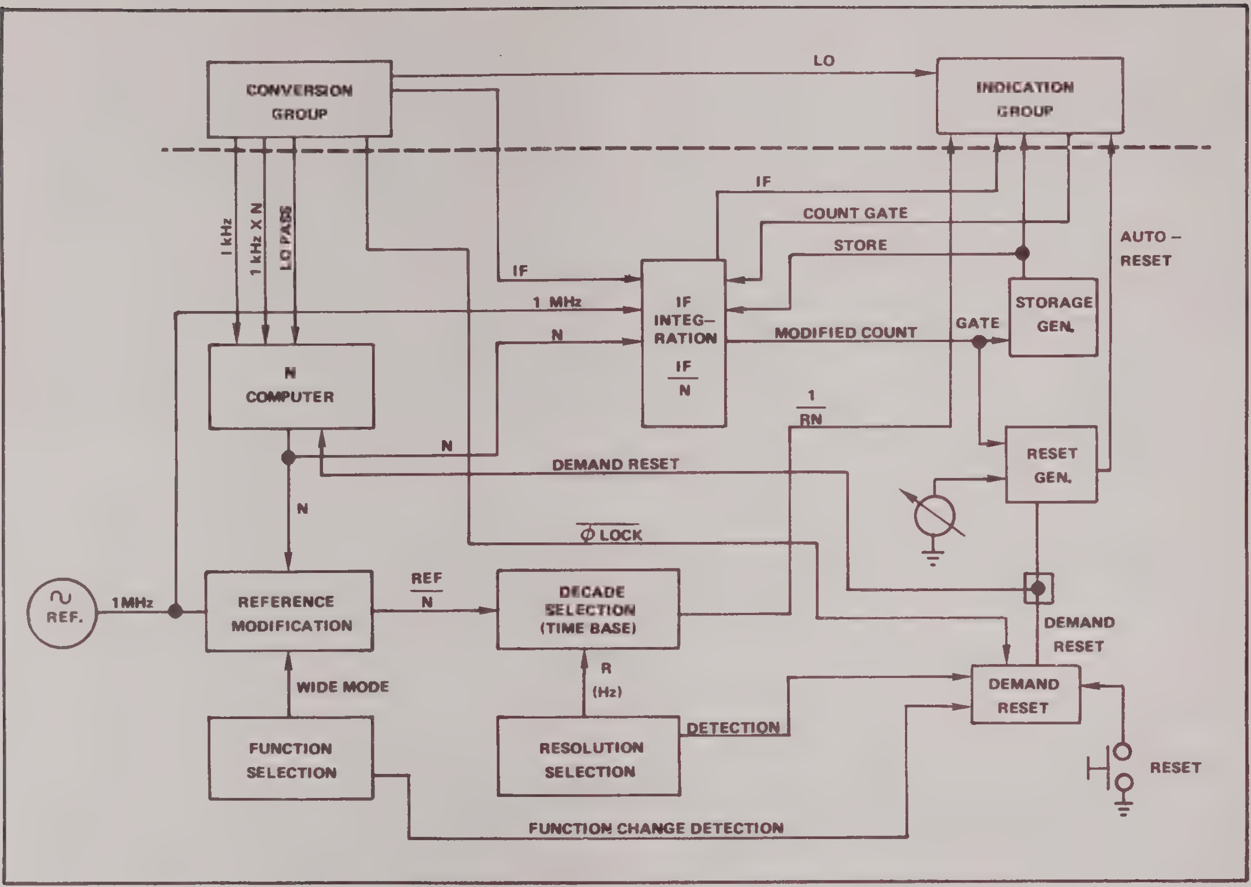

CONVERSION GROUP
LO
INDICATION GROUP
1 kHz
1 kHz X N
LO PADS
IF
COUNT GATE
STORE
AUTO – RESET
IF
1 MHz
N
IF INTEG– RATION
IF / N
MODIFIED COUNT
GATE
STORAGE GEN.
N COMPUTER
1 / RN
N
DEMAND RESET
RESET GEN.
N
Φ LOCK
REF.
1MHz
REFERENCE MODIFICATION
REF / N
DECADE SELECTION (TIME BASE)
DEMAND RESET
WIDE MODE
R (Hz)
DEMAND RESET
DETECTION
FUNCTION SELECTION
RESOLUTION SELECTION
RESET
FUNCTION CHANGE DETECTION

FIGURE 4-10 WIDE ACTO OPERATION, CONTROL GROUP

harmonic number N is computed by developing the exact ratio of N X 1 kHz/1 kHz. When the harmonic number has been computed by the N computer, that value is used to expand the selected time base by that value and divide the IF signal by the same N value. When the time base (TB) value, and the modified IF signal are available, the measurement cycle begins. The signal gates are opened for the period of TB X N to the accumulator in the Indication Group and the IF integrator in the Control Group. The data in the accumulator is transferred to storage at the end-of-gate time. The value present in the IF accumulator is then added into storage in four serial bytes. When the complete frequency of interest is in storage a Data Ready flag signals that valid information is available for peripheral equipment. The Recycle Rate controls the number of measurements displayed per minute. The number of measurements for up to 1 MHz resolution range from 15 to 1500 per minute.

## 4.15 NORMAL FLACTO OPERATION

This mode of operation is developed through the use of digital techniques. (see figure 4-11) Similar to heterodyne performance, it provides all of the benefits, yet eliminates many of the problems associated with heterodyne conversion techniques. When the narrow mode is selected and the signal present/acquisition complete flags are present, N computation again takes place. However, unlike automatic transfer oscillators, which require that the measuring time be (1/r) X N, this system has a fixed requirement of $(1/10^3)$ X N + (1/R) seconds for the first reading after N computation. The time required for the second measurement and each successive measurement is equal to (1/R) seconds. The reference frequency is divided to provide a 10 kHz reference to the Conversion Group. The local oscillator frequency is divided automatically by the M divider to produce a 10 kHz frequency. When the 10 kHz generator

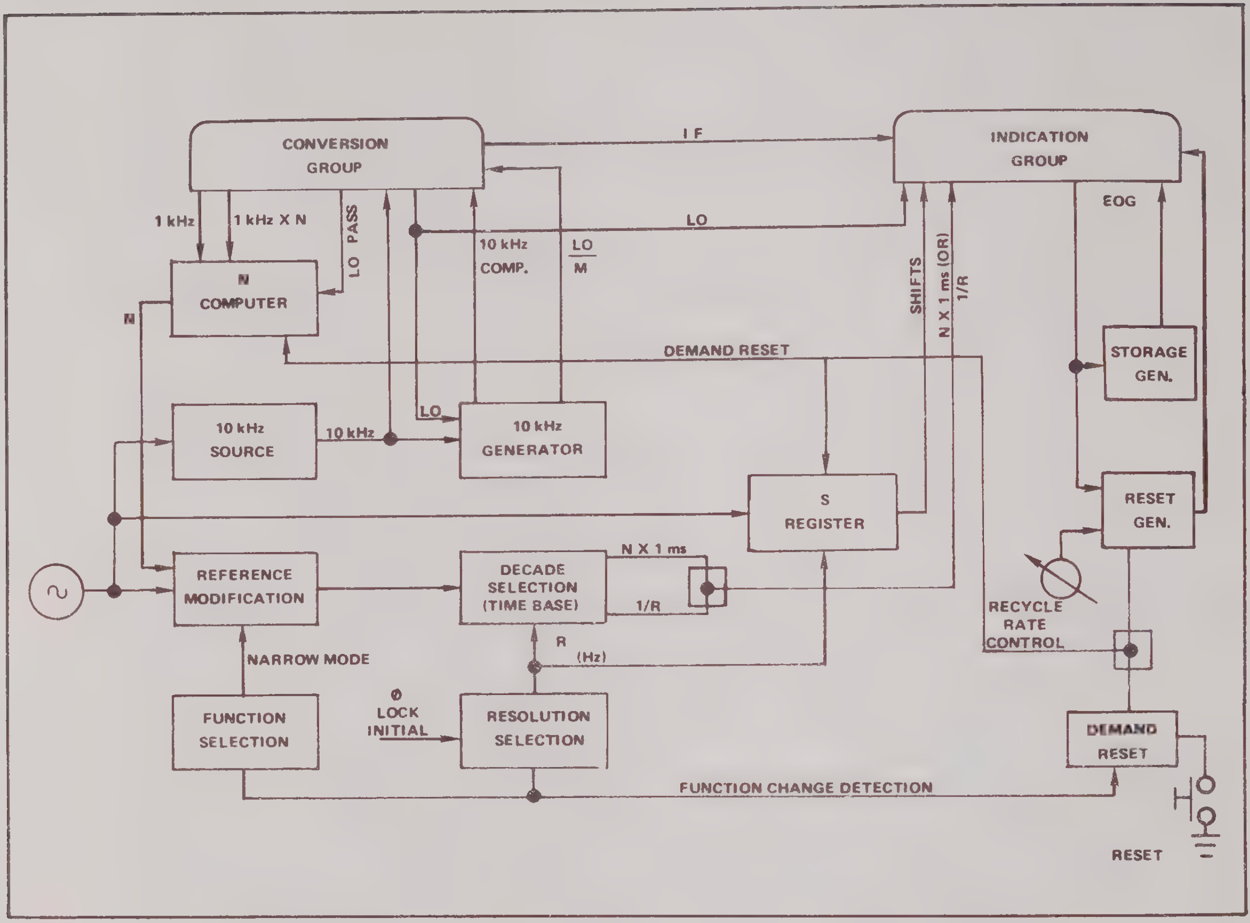

CONVERSION GROUP
I F
INDICATION GROUP
1 kHz
1 kHz X N
LO PASS
LO
10 kHz COMP.
LO/M
EOG
N COMPUTER
N
SHIFTS
N X 1 ms (OR)
1/R
DEMAND RESET
STORAGE GEN.
10 kHz SOURCE
10 kHz
LO
10 kHz GENERATOR
S REGISTER
RESET GEN.
N X 1 ms
REFERENCE MODIFICATION
DECADE SELECTION (TIME BASE)
1/R
RECYCLE RATE CONTROL
R (Hz)
NARROW MODE
FUNCTION SELECTION
0 LOCK INITIAL
RESOLUTION SELECTION
DEMAND RESET
FUNCTION CHANGE DETECTION
RESET

FIGURE 4-11 NARROW FLACTO METHOD, CONTROL GROUP

and the 10 kHz reference produce a phase lock condition for the local oscillator, a gate length equal to N X ($1/10^3$) is applied to the signal gate of the accumulator in the Indication Group. The signal measured at this time is the LO frequency, which is phase-locked to a 10 kHz increment of the reference frequency. The data is transferred from the accumulator to the shift register and is shifted the proper number of digits, dependent upon the selected resolution, and is then transferred back into the accumulator. The IF signal is measured for 1/R time to produce the complete frequency. Transfer to storage completes the first measuring cycle. Successive measurements are made by transferring the data from the shift register to the accumulator and measuring the IF frequency for 1/R time. Transfer to storage completes the second and successive measurements. In this mode any frequency within the operating range of the instrument may be measured to 1 kHz resolution in the Computer Dump mode at a rate of approximately 990 readings per second. Resolution to 1 MHz provides approximately 83,000 readings per second.

## 4.16 CIRCUIT DESCRIPTIONS

The following paragraphs (4.17 through 4.37) provide detailed circuit level description for the individual assemblies. Refer to Chapter 7 of the manual for the schematic diagrams that are referenced by the circuit analysis that follows.

## 4.17 COUNT CHAIN ASSEMBLIES A4, A3, A1

The Count Chain is comprised of the LSD Decade Assembly A3 and the MSD Decade Assembly A1 (see figure 7-5 and 7-3 schematic diagrams). The integrated circuit registers that make up the count chain are identified functionally as follows:

1. A3U2 through A3U6 are the $10^1$ through $10^5$ accumulators. The $10^0$ accumulator is located on assembly A4, and is titled as the 500 MHz Decade (see figure 7-7) Reference designated as A4U6.

2. A1U1 through A1U5, are the $10^6$ through $10^{10}$ Accumulators.

3. A3U13 through A3U18, are the $10^0$ through $10^5$ Storage Registers.

4. A1U15 through A1U19, are the $10^6$ through $10^{10}$ Storage Registers.

5. A3U8 through A3U12, are the $10^1$ through $10^5$ Shift Registers.

6. A1U8 through A1U12 are the $10^6$ through $10^{10}$ Shift Registers.

The Count Chain Circuits operate in three different functional modes:

1. Direct Counting Mode is used when the low frequency J3 input (20 Hz to 20 MHz) is counted, or when the high frequency J1 input from 20 MHz to 500 MHz is counted.

2. Wide Band Conversion (ACTO) Counting Mode, is selected, when counting RF signals (500 MHz to 24 GHz), that have low modulation index and high deviation rates, i.e. FM transmitter output measurements.

3. Normal Band Conversion (FLACTO) Counting mode is selected, when counting RF signals (500 MHz to 24 GHz) that have high modulation index and low deviation rates, this mode provides for high count resultions of AM signals.

When the Count Chain is operating in the direct count mode, the 1-2-4-8 BCD $10^0$ Accumulator output is applied to the $10^0$ Storage Register A3U13, and the $10^0$ $\overline{\text{CARRY}}$ is clocked into $10^1$ Accumulator A3U2. The $10^1$ Accumulator outputs a 1-2-4-8 BCD to the $10^1$ Storage Register A3U14. The $10^1$ Accumulator also outputs the BCD bit 8 as the $10^1$ $\overline{\text{CARRY}}$ to A3U3-8 as the $10^2$ clock input. The count accumulation proceeds down the chain to the $10^{10}$ decade in the similar manner, outputting its BCD count to the Storage Registers. At the end of count (EOC) a $\overline{\text{STORE}}$ signal is generated by the Function PCB Assembly A11 and applied to A1 pin Ⓝ and A3 pin ⑫. This will load the Storage Registers with the count data (in 8-4-2-1 BCD format) accumulated in the count chain. The Storage Registers in-turn drives the the 11 digit Display PCB Assembly A13, At the end of the display period a $\overline{\text{RESET DECADES}}$ signal is generated by the Function PCB Assembly A11, which resets all the Accumulation Registers.

When Wide Band (ACTO Conversion) mode is selected, the Accumulators count the LO frequency for a period of 1/R (N) via the $10^0$ Accumulator input A4U6-16. At the end of the count period, the $\overline{\text{STORE}}$ signal loads the 1-2-4-8 BCD count from the Accumulators to the Storage Registers. During the same period the IF Integrator Assembly A6 Counter, counts the IF signal and outputs the count in a four byte serial format to the Count Chain. The BYTE (1) serial count is applied to the upcount clock input of the $10^6$ Storage Register A1U11 allowing the counter to upcount thus adding the IF count to the LO count in the $10^6$ digit. The BYTE (2), BYTE (3) and BYTE (4) serial data is applied in a similar manner to the $10^4$, $10^2$, and $10^0$ Storage Registers. The end result of this logic operation, is that the LO frequency and the IF frequency are counted for a 1/R (N) period, then added to equal the count of the RF input measurement signal.

When Normal Band (FLACTO Conversion) counting mode is selected, the LO is phase locked to a 10 kHz increment of the Reference Oscillator, and its output is counted for a N X 1 millisecond period by the Accumulators. Then the accumulated LO count is loaded into the Shift Registers by the $\overline{\text{LOAD SR}}$ signal. The Shift Registers are then clocked by the $\overline{\text{CLOCK SR}}$ pulses to shift the count a proper number of digits to match the selected resolution. When the data in the Shift Registers is correctly located, the Accumulators are loaded with the Shift Register contents on the application of the RESET DECADES signal. The IF frequency is then counted for a 1/R period, thus adding to the count that was preset into the Accumulators from the Shift Registers. This summed count is then loaded into the Storage Registers by the $\overline{\text{STORE}}$ signal to provide display of the measurement data.

The switch selected resolution data is generated by the 20 MHz Amplifier PCB Assembly A12 and supplied as the D.P. 1-2-4-8 BCD code to the Count Chain. The D.P. decoder gates A1U7 and A3U7 decode the BCD into the D.P. 1 through D.P. 9 signals which relates to the MSD of the selected resolution. These decoded MSD signals are applied to the preceeding Storage Register decade down clock inputs allowing the Storage Registers to adjust its contents to the selected resolution. The $10^{10}$ LEAD ZERO DISABLE signal is generated by the IF Integrator PCB Assembly A6 and applied to A1 pin $\boxed{17}$, which will down clock to $10^{10}$ Storage Register A1A18. The Storage Registers signals are outputted as $10^1$ through $10^{10}$ BLANK signals to the Display PCB Assembly A13 to surpress all leading zeros from the display.

### 4.18 500 MHz DECADE AND GATE ASSEMBLY A4

The 500 MHz Decade and Gate PCB Assembly A4 (see figure 7-7 for schematic diagram) provides the following functional circuits:

1. The 20 MHz to 500 MHz Band Pass amplifier circuit (Q1 through Q7 and associated components).

2. The Count Select Gate circuit (U3, U4, U8, U9, U10 and U11).

3. The Count Gate Control M.V. (U2).

4. The Count Gate (U5 and U3).

5. The 500 MHz Decade ($10^0$ Accumulator U6).

6. Low Pass Detector circuit (U1, Q9, Q10 and associated circuits).

The 20 MHz and 500 MHz Band Pass Amplifier, receives its input from the RF "N" connector J1 via the 500 MHz Preamp, the N Mixer Assembly A19 and the 6 dB Pad U3 (see figure 6-1 Block Diagram). If the input is from 20 MHz to 500 MHz, the analog signal will be amplified and applied to the Low Pass Detector Circuit. The Low Pass Detector then generates the $\overline{\text{LOW PASS}}$ command if the LOW BAND function has not been switch selected, (a logic high on A4 pin $\boxed{14}$). The $\overline{\text{LOW PASS}}$ command outputted at A4 pin Ⓢ will disable the LO drive to the FLACTO Mixers, inhibit the N Computer and configure the Time Base to normal (1 μsecond to 1 second in decade steps). When this Auto Low function is thus configured the 500 MHz Decade will directly count the 20 MHz to 500 MHz signal applied to its clock input at U6-14.

Most digital logic operations of the A4 Assembly are ECL, and the logic translation from TTL levels is provided for by the input TTL to ECL translator gates U4 and U9. The LO and IF input analog signals are buffered by the line amplifiers U8-3 and 15. Logic translator/amplifier U8-6-7 buffers the IF input which is outputted to the N Computer Assembly A10 via A4 pins $\boxed{\text{L}}$ and $\boxed{\text{M}}$.

The input signals that control the gate selection of the decade inputs are listed and defined as to function below;

1. $\overline{\text{LOW}}$; The LOW 20 Hz and 20 MHz function has been switch selected, disable the Low Pass Detector circuit, and count the HI Z AMP 20 Hz to 20 MHz signal.

2. $\overline{\text{200-500}}$; A $\overline{\text{LOW PASS}}$ command has been generated and the Auto Low 20 MHz to 500 MHz direct count function has been configured, disable LO and IF and allow the 500 MHz Decade to count the signal applied to U6 pin 14.

3. $\overline{\text{TEST}}$; TEST INSTR switch has been pressed and latched, count the 1 MHz Reference Oscillator frequency.

4. $\overline{\text{COUNT L.O.}}$; Logic selection for ACTO conversion mode is configured, count the L.O. frequency.

5. $\overline{\text{COUNT IF}}$; the NORMAL function switch has been pressed and is latched and logic

selection for FLACTO conversion mode is configured, count the IF frequency.

Figure 4-12 A4 Functional Logic Diagram supports the following circuit analysis. When the front panel LOW function switch is pressed and latched a ground is applied to A4 pin 14 as the LOW command, which gate enables the HI Z AMP (20 Hz to 20 MHz) signal. This command also generates the LOW PASS DISABLE which disables the Low Pass Detector Circuit. This logic operation allows the 20 Hz to 20 MHz signal to be applied to U6 pin 16 for direct counting, and disables the Auto Low function signal from being counted.

When the TEST/INSTR front panel switch is pressed and latched a ground is applied to A4 pin 16 as the TEST enable, which gate enables the 1 MHz Reference Oscillator signal to be counted by the 500 MHz Decade Counter U6. The gating logic of U10-3, U10-6 and U11-11 effects an exclusive OR selection with the LOW enable.

The Local Oscillator frequency (LO IN) is exclusive OR gate selected and applied to the 500 MHz Decade via the Count Gate when a ground is applied to A4 pin R as the COUNT LO enable signal. The COUNT LO signal is generated by the Function Assembly A11, when the counter is configured for ACTO conversion.

The Lock IF frequency (IF IN) signal at A4 pin P and N is exclusive OR gate enable when a ground is applied to A4 pin S as the COUNT IF enable signal, allowing the IF frequency to be applied to the 500 MHz Decade for counting. The COUNT IF signal is generated by the Function Assembly A11, when the NORMAL function has been switch selected to configure the counter for narrow band FLACTO conversion mode of operation.

When the Auto Low direct 20 MHz to 500 MHz mode of operation is configured the 20 MHz Amplifier Assembly A12 generates the 20-500 signal which is applied to A4 pin U. The 20-500 signal

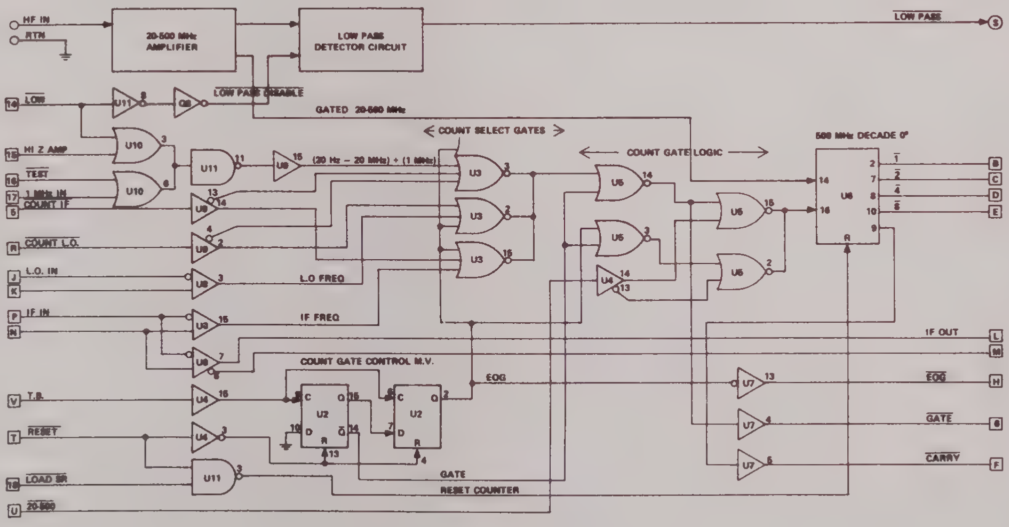

HF IN
RTN
20-500 MHz AMPLIFIER
LOW PASS DETECTOR CIRCUIT
LOW PASS
S
14
LOW
U11
Q8
LOW PASS DISABLE
GATED 20-500 MHz
COUNT SELECT GATES
15
HI Z AMP
16
TEST
17
1 MHz IN
COUNT IF
S
U10
U11
U8
(20 Hz – 20 MHz) + (1 MHz)
U3
R
COUNT L.O.
J
L.O. IN
K
L.O FREQ
P
IF IN
N
IF FREQ
COUNT GATE CONTROL M.V.
V
T.B.
U4
T
RESET
18
LOAD SR
U
20-500
U2
C
Q
D
R
EOG
GATE
RESET COUNTER
COUNT GATE LOGIC
U5
500 MHz DECADE 0°
U6
1
2
4
8
B
C
D
E
IF OUT
L
M
U7
EOG
H
GATE
G
CARRY
F

FIGURE 4-12 A4 FUNCTIONAL LOGIC DIAGRAM

will allow the 20 MHz to 500 MHz signal at pin 14 of U6 to be counted.

The T.B. signal applied to A4 pin $\boxed{V}$ as positive going transitions will enable the Count Gate for the selected count period via the Count Gate control M.V. U2. When a $\overline{\text{RESET}}$ is applied as a logic low to A4 pin $\boxed{T}$ U2 and U6 will reset and the EOG (end of gate) flag will be removed. The $\overline{\text{LOAD SR}}$ signal applied at A4 pin $\boxed{18}$ will reset U6 the 500 MHz $10^0$ Decade to zero when low.

The 500 MHz $10^0$ Decade U6 BCD outputs are translated to TTL logic levels by pulling up to +5V through U12's resistors. The EOG flag is inverted and translated to a TTL $\overline{\text{EOG}}$ by U7-13 and outputted at A4 pin $\boxed{H}$. Non-inverting ECL to TTL logic translation of the GATE and the $\overline{\text{CARRY}}$ signals is provided by U7-4 and U7-5.

## 4.19 IF INTEGRATOR PCB ASSEMBLY A6

The IF Integrator provides two major functions: it integrated the IF/N count into four 4-bit serial Bytes which is outputted to the Count Chains Shift Registers for addition to the LO count during ACTO mode operation; and allows a BCD controlled offset of the frequency measurement when Option 28 is incorporated into the instrument (see Figure 7-9 IF Integrator Assembly A6 Schematic Diagram).

The IF/N is entered into the eight decade integrator counter consisting of U16 through U23 by application of the gated IF/N signal to the up-count clock input pin 5 of U16. The output of the IF count loaded into the Integrator Counter is initiated by the $\overline{\text{STORE}}$ command inputted at A6-$\boxed{J}$, which enables the 1 MHz clock to the Integrator Control Flip-Flops consisting of U8 and U9. The Integrator Control Flip-Flops generate the four serial bytes in the following manner. The Byte 1 Flip-Flop $\overline{\text{Q}}$ output (U8-6) is gated with the 1 MHz clock by U10-3 and down clocks the $10^6$ Integrator Decade U22, and the $10^6$ borrow U22-13 is applied to the $10^7$ Integrator Decade down clock input at U23 pin 4. When all bits are low on the BCD outputs of the $10^6$ and $10^7$ decades, gating logic comprised of U15, U11-6, U5-3 and U2-11 generate a low that latches and resets the Byte 1 Control Flip-Flop U8-6. The number of clocks required to down count the $10^6$ and $10^7$ decades to all zero's is the serial Byte 1 signal and is outputted from gate U10-3 to A6 pin ⑬. The Byte 2, Byte 3, and Byte 4 Control Flip-Flops U9-6, U9-8 and U8-8 function in a similar manner down clocking the LSD's of the counter. When the last Byte (Byte 4) of the integrated IF word is generated and Flip-Flop U8-8 is latched and reset, the EOC (end-of-count) Flip-Flop is toggled and outputs the $\overline{\text{EOC}}$ and EOC signals at U7 pin 8 and 9 respectively. The $\overline{\text{LEAD ZERO DISABLE}}$ signal is removed at the end of the integrated IF word and dot AND'ed with the $\overline{\text{STORE}}$ signal and outputted at A6 pin ④.

The remote offset data is applied via PCB Assembly A11 as a 32 bit BCD word and loaded parallel into the eight decades of the integrator count chain. The decades are loaded (preset) on the presents of the $\overline{\text{PRESET DECADE}}$ signal from the Function PCB Assembly A11 and the OFFSET signal from the remote device via the offset PCB Assembly A7.

Figure 4-13 provides a timing diagram of one decade counter operation sequence of:

1. Reset to zero.
2. Preset to BCD 7 (enter offset of 7).
3. Count IF/N to 8, 9, carry, 0, 1 and 2.
4. Count down to 1, 0 and borrow (generate the first 2-bits of the integrator byte).

## 4.20 TIME BASE PCB ASSEMBLY A8

The Time Base logic (see Figure 7-11 schematic diagram) generates a Time Base gate of 1 μsecond to 100 milliseconds in decade steps, referenced to selected 1 MHz, 10 MHz or 3 MHz reference inputs and controlled by the setting of the front panel RESOLUTION switch.

The normal Reference Oscillator source is the standard internal 10 MHz Time Base Oscillator Assembly, 05512401, which inputs a 10 MHz reference to A8 pin D. This 10 MHz input is applied to A8U5, a divide-by-ten counter, which outputs a 1 MHz reference clock to exclusive OR gate A8U19-10.

When Option 11, 12 or 13 is configured an optional 3 MHz reference is supplied to A8 pin $\boxed{D}$. The 10 MHz jumper, U19-5 input, is moved to the 3

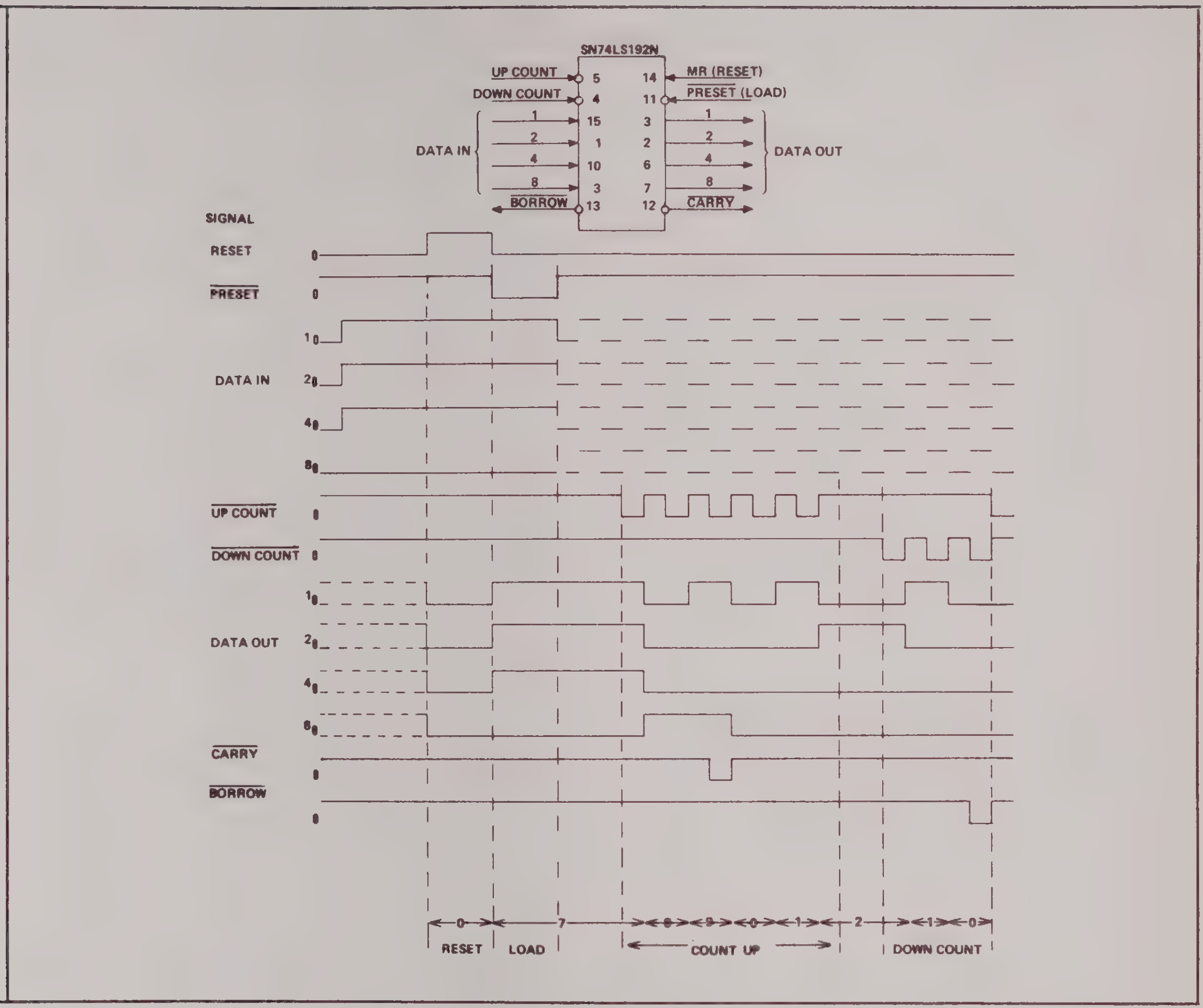

SN74LS192N
UP COUNT
DOWN COUNT
5
4
14
11
MR (RESET)
PRESET (LOAD)
DATA IN
1
2
4
8
15
1
10
3
3
2
6
7
DATA OUT
BORROW
13
12
CARRY
SIGNAL
RESET
PRESET
DATA IN
UP COUNT
DOWN COUNT
DATA OUT
CARRY
BORROW
0
7
8
9
0
1
2
1
0
RESET
LOAD
COUNT UP
DOWN COUNT

FIGURE 4-13 IF INTEGRATOR DECADE SEQUENCE TIMING DIAGRAM

MHz position, U19-1 input. The 3 MHz input is thus routed to a divide-by-three counter configured by Flip-Flops U4. The resultant 1 MHz output is routed to exclusive OR gate A8U19-10 as the reference clock.

An alternate reference source is the rear panel external BNC connector J6. When the INT/EXT selector switch S5 is placed in the EXT position an external 1 MHz or 10 MHz reference may be inserted via J6 at A8 pin $\boxed{J}$, and a ground is placed at A8 pin $\boxed{E}$ as the EXT signal. This logic low at A8 pin $\boxed{E}$ disables A8U15-3, removing the internal reference, and enables A8U15-8. The external 1 MHz of 10 MHz reference is thus routed to both the divide-by-ten counter A8U5 and the one shot shaper A8U20. If the input is 1 MHz, A8U20 holds A8U5 clear and a 1 MHz clock is coupled via A8U15-6 to A8U19-8. If the input is 10 MHz the timing circuits of A8U20 hold it off and the reference signal is divided down by A8U5 providing a 1 MHz clock at A8U19-11.

The 1 MHz reference clock outputted from the select gate A8U19-8 is applied to the rear panel 1 MHz OUT BNC connector J5, via A8U14-8 and A8 pin $\boxed{C}$. Select gate A8U19-8 also applies a 1 MHz clock to the clock Flip-Flop A8U21 at its clock input pin 3. When this D type Flip-Flop is edge triggered by the 1 MHz clock, a logic low is placed on its Q output pin 5, and a logic high is placed on the $\overline{Q}$ output pin 6. The A8U21-5 $\overline{\text{CLOCK}}$ signal is gated with the 1 MHz by A8U7-6 outputting the 1 MHz clock for the TB Counter circuits. The U19-8 1 MHz signal is also gated by A8U14-6 to supply the INST 1 MHz signal which is outputted at A8 pin $\boxed{B}$.

The selector gates comprised of A8U16-8 and A8U16-6 logic selects the 1 MHz, or the 1 MHz/N signals for time base counter clock. The time base counter is comprised of six time period decades (A8U8 through A8U13), which are preset (parallel loaded to zero) by the 1 μs through 10 ms resolution switch selected signals or $\overline{\text{P.L. INITIAL}}$ signal, and then clocked by the logic selected count applied to A8U8 pin 4. The 24-bit BCD output is gate combined by A8U1, A8U2, A8U3 and A8U6 to develop the selected time base. The time base counter operates in three different functional modes:

1. Direct Counting; A TB period of 1 μsecond to 100 milliseconds in six decade steps, as selected by the RESOLUTION switch and referenced to the reference oscillator is generated.

2. Wide Band Counting; A TB period of (1/R) N (selected resolution times the harmonic number) is generated.

3. Normal Band Counting; A TB period of N ($10^{-3}$) (harmonic number times 1 millisecond) is generated.

### 4.21 10 kHz GENERATOR PCB ASSEMBLY A9

The function of the 10 kHz Generator is to generate the VCO/N signal, which will allow the LO to phase-lock to a 10 kHz increment of the 1 MHz reference times the harmonic number (see figure 7-1 and 7-13). The LO frequency is inputted at A9 pins $\boxed{K}$ and $\boxed{J}$ and the "M" counter logic divides the LO frequency to 10 kHz as the VCO/N signal, which is applied to the Search Oscillator Assembly A15 via A9 pin ⑯. The Search Oscillator phase compares the VCO/N signal with the 10 kHz reference from the N Computer Assembly A10 and generates the VCO control level (RAMP) to drive the LO into phase-lock with the 10 kHz reference. When phase lock is obtained the N Computer A10 generates the 10 kHz GATE which is applied to A9 pin Ⓡ to set the "M" divider and lock up the loop. If phase lock is dropped a $\overline{\text{CLEAR 10 kHz}}$ is generated by the N Computer A10 and applied to A9 pin Ⓒ which will reset A9U2 and U3 thus allowing a search and rephase-lock of the LO.

### 4.22 N COMPUTER PCB ASSEMBLY A10

The N computer determines the harmonic number (N) and generates the control, command and flag signals required by WIDE mode (ACTO) and NORMAL (narrow FLACTO) conversion operations (see figure 7-1 6054B block diagram and figure 7-15 N computer schematic diagram). The N computer is divided into five basic sub-functions that are listed and defined as follows:

1. Harmonic number (N) determination; is the computation of the exact ratio of N X 1 kHz. The 1 kHz X N is inputted at A10 pin Ⓢ, which is the output of the Lock IF mixed with the N IF frequency. This signal is counted and divided by the N counter (A10U18 and U4) which outputs the N number as an 8-bit binary format. At the conclusion of N determination an N COMPUTED flag is generated and outputted at A10 pin Ⓐ .

2. 1 MHz/N signal generation: The N 8-bit is applied to the 1 MHz/N counter (A10U9 and U14) as the divisor program and the 1 MHz is applied as its clock and gate. The PE outputs of A10U9 and A10U14 pin 3 are outputted (via translator U23) at A10 pin $\boxed{1}$ as the 1 MHz/N signal.

3. IF/N signal generation; The N 8-bit binary from the N computer is applied to the IF/N counter (A10U21 and U25). The IF signal from the 500 MHz Decade A4 is a shielded pair cabled to A10 pins $\boxed{R}$ and $\boxed{P}$ , then converted from a two line 100Ω RF input to a single line ECL signal by A10U26-15. This signal is clocked into the IF/N counter and the Q outputs are OR'ed

by gates A10U22 as the IF/N signal, which is applied to the D input of flip-flop A10U27 at pin 10 and the flop-flop is toggled by the IF signal. The flip-flops $\overline{\text{Q}}$ output is converted from ECL-to-TTL by translator A10U23-13 and applied to the IF Integrator Assembly A6 via A10 pin $\boxed{\text{T}}$ output.

4. 10 kHz reference and 10 kHz GATE signal generation; the 1 MHz reference inputted at A10 pin ⑰ is counted down to 10 kHz by counters A10U17 and U12, which then toggles the D flip-flop A10U2-5, outputting a 10 kHz reference at A10 pin ⑨. The 10 kHz GATE signal is developed on the input of the $\overline{\text{PHASE LOCK}}$ flag at A10 pin ①, by flip-flops A10U3 and U8 and outputted at A10 pin ⑯. Also provided by this logic function are the 10 kHz COMPUTED, $\overline{\text{PHASE LOCK RESET}}$ and $\overline{\text{CLEAR 10 kHz}}$ flags

5. Squelch and N Inhibit generation; the SQUELCH signal from the lock IF PCB assembly A17 is routed to A10 pin ④ and then applied as the clock to the squelch counter comprised of A10U6 and A10U11-6. The counter outputs the SQUELCH signal to the Search Oscillator assembly A15 via A10 pin ⑥. The MODIFIED SQUELCH signal which is routed to the Function PCB assembly A11 via A10 pin ⑧ is generated by NAND gating SQUELCH and $\overline{\text{PHASE LOCK RESET}}$ signals (gate A10U10-6). Gate A10U13-11 NAND's the $\overline{\text{TEST}}$ and $\overline{\text{SQUELCH}}$ to generate the $\overline{\text{N INHIBIT}}$ signal, at A10 pin $\boxed{\text{S}}$.

### 4 23 FUNCTION PCB ASSEMBLY A11

The function PCB assembly generates commands and flags to control the operation of the Indication and Control Groups. **Figure 7-17 Function** Assembly A11 Schematic Diagram supports the following circuit descriptions. The eighteen discreet signals generated by the function circuit logic are listed, defined and described as to their development as follows:

1. $\overline{\text{LOAD SR}}$ pin $\boxed{\text{T}}$; A command sent to the Count Chain Assemblies A1 and A3 that allow the accumulated LO count to be loaded into the shift registers. This signal goes low at EOG time and the presentation of a N COMPUTED flag, the period of this gate is determined by the SR gate counter A11U6.

2. CLOCK SR pin $\boxed{\text{U}}$; A gated 1 MHz clock outputted to the Count Chain Assemblies A1 and A3 to shift the data a proper number of digits to match the selected resolution. The gate period is determined by the SR clock counter A11U7 and its associated gate control logic which is enabled by the resoltuion selected signals $\overline{\text{1 ms}}$, $\overline{\text{10 ms}}$, $\overline{\text{100 ms}}$ or $\overline{\text{1s}}$.

3. $\overline{\text{RESET DECADES}}$ pin $\boxed{\text{S}}$; A signal sent to the Count Chain Assemblies A1 and A3 to reset the accumulators to zero.

4. $\overline{\text{PRESET DECADES}}$ pin $\boxed{\text{V}}$; A command to the Count Chain Assemblies A1 and A3, which loads (presets) the contents in the shift registers back into the accumulator registers.

5. $\overline{\text{INHIBIT END OF COUNT}}$ pin $\boxed{\text{P}}$; An inhibit signal applied to the IF Integrator Assembly A6 which will inhibit the generation of an EOC by the EOC flip-flop A6U7. This inhibit signal is generated by gate A11U8-11 when the $\overline{\text{PHASE LOCK}}$ and LOAD SR (A11U6-5) are NAND gated.

6. $\overline{\text{PHASE LOCK INITIAL}}$ pin $\boxed{\text{5}}$; is applied to the Time Base Assembly A8 to allow the time base to generate a period N $(10^{-3})$ (harmonic number times 1 millisecond). This command is generated by A11U9-3 gating the $\overline{\text{PHASE LOCK}}$ and RESET DECADES signals.

7. $\overline{\text{COUNT IF}}$ pin $\boxed{\text{R}}$; is applied to the 500 MHz Decade Assembly A4 to enable the Lock IF frequency to be counted. This command is generated by A11U9-11 gating of the $\overline{\text{PHASE LOCK}}$ and PRESET DECADES signals.

8. $\overline{\text{COUNT L.O.}}$ pin $\boxed{\text{4}}$; is applied to the 500 MHz Decade and the Time Base Assemblies A4 and A8, to enable the L.O. frequency to be counted for a 1 MHz/N period. This command is generated by A11U16-8 gating of the $\overline{\text{FREQ LOCK}}$ and the $\overline{\text{PHASE LOCK INITIAL}}$ signals.

9. RESET pin ④ is applied to the 500 MHz Decade IF Integrator and Time Base Assemblies A4, A6 and A8. The RESET inputted to the Time Base at A8 pin Ⓢ will reset the TB counter A8U8 through A8U13 and preset the 1 MHz control flip-flop A8U21. The RESET applied to the 500 MHz Decade at A4 pin $\boxed{T}$ resets the gate M.V. A4U2-2 and the 10° accumulator A4U6. The RESET to the IF Integrator is applied to A6 pin ⑫ and will reset the EOC flip-flop as a logic low at A6U7-13. The RESET is generated by any one of the following logic operations.

a. Generation of the DEMAND CLEAR at gate A11U16-3.

b. A logic low at A11U2-4 which is a One Shot M.V. $\overline{Q}$ output that is generated at the end of the CLOCK SR signal.

c. At the end of the display period. This logic function consists of the Display Timer A11U21 which is triggered by the EOC signal inputted at A11 pin ③ and timed by the DISPLAY control potentiometer setting. At the end of the display period A11U21-3 goes low generating the reset.

d. A SAMPLE input at A11 pin Ⓒ.

e. A P.L. RESET input at A11 pin Ⓕ.

f. A CHANGE CLEAR input at A11 pin Ⓔ.

10. STORE pin Ⓓ; is applied to the Count Chain and the IF Integrator Assemblies A1, A3 and A6. The STORE inputted the Count Chain at A1 pin N and A3 pin ⑫ provide a load command for the Storage Registers. The STORE applied to the IF Integrator at A6 pin Ⓙ is dot OR'ed to generate the LEAD ZERO DISABLE signal at A6 pin ④. The STORE is generated by the Store One Shot M.V. A11U12-5 when a EOG is inputted at A11 pin $\boxed{C}$, or on a DEMAND CLEAR.

11. DEMAND CLEAR pin Ⓤ; is a reset command generated on demand by any of the following logic operations;

a. A LOW PASS input at A11 pin $\boxed{B}$ triggering the Low Pass One Shot M.V. A11U22-5.

b. A manual momentary closure of the front panel RESET pushbutton switch generating a RESET PUSH-BUTTON signal at A11 pin ⑰.

c. A momentary loss of +5 volts detected by the circuit comprising A11Q2 and its associated RC components.

d. An ACTO input at A11 pin ⑫.

e. Dropping of the MODIFIED SQUELCH signal on A11 pin Ⓜ while the ACTO line is active.

The DEMAND CLEAR at A11U16-3 is applied to pin 11 of gate A11U1 to generate a RESET command.

The DEMAND CLEAR at A11 pin Ⓤ is applied to the Count Chain Assemblies A1 and A3 to reset the Shift Registers.

12. RESET N pin $\boxed{2}$; is generated on RESET PUSHBUTTON or LOW PASS inputs and is applied to the N Computer Assembly A10 to generate the RESET ACTO signal.

13. GATE LAMP pin $\boxed{14}$; is generated by the Gate Lamp One Shot M.V. A11U2-5 when triggered by the GATE signal applied to A11 pin Ⓛ The GATE LAMP signal is applied to the Display Assembly A13 as a ground return for the GATE lamp A13DS4.

14. OVERLOAD LAMP pin Ⓝ, OVERLOAD pin Ⓟ and BLINK pin Ⓣ; are generated when the OVERLOAD signal from the Search Oscillator Assembly A15 is inputted to A11 pin $\boxed{17}$. This analog signal is translated to a logic low TTL level by A11Q1 and inverted to a logic high by A11U15-4. This OVERLOAD flag is outputted to the BCD Option 04 assembly A2 via A11 pin Ⓟ. A high applied to pin 4 of A11U14 enables the timer IC which is configured to opperate as a gated freerunning M.V., its output is a half-second rate flash alternating between ground and +5V. Inverter A11U3-8 outputs the BLINK signal to the Display Assembly A13 via A11 pin Ⓣ to flash the LSD of the display. Inverter

A11U3-6 outputs the $\overline{\text{OVERLOAD LAMP}}$ signal to the front panel OVERLOAD LED annunciator. The A11U14 pin 3 output is also applied to pin 5 of gate A11U4 to flash the LOCK LED annunciator on an overload detection. The end result of the overload flag operation is that when an overload is applied to the instruments input the OVERLOAD LED annunciator and the LOCK LED annunciator flash alternately and the LSD of the display also flashes.

15. $\overline{\text{LOCK LAMP}}$ pin Ⓢ and $\overline{\text{LOCK}}$ pin $\boxed{J}$; are generated when $\overline{\text{LOW PASS}}$ or N COMPUTED and MODIFIED SQUELCH signals are applied to the A11 Assembly and gated by A11U17-11 and A11U4-8. The $\overline{\text{LOCK}}$ signal is applied to the Remote Option 04 Assembly A5 to supply a LOCK flag to a remote device. The $\overline{\text{LOCK}}$ is also applied to NOR gate A11U4-6 where it is NOR'ed with the BLINK, to allow the LOCK LED to flash alternately with the OVERLOAD LED when an overload is detected and flagged. Inverter A11U3-4 inverts the signal to $\overline{\text{LOCK LAMP}}$ which is outputted to the front panel LOCK LED annunciator DS2.

## 4.24 20 MHz AMPLIFIER ASSEMBLY A12

The 20 MHz Amplifier Assembly (see figure 7-19 schematic diagram) provides two basic sub-functions:

1. 20 MHz High Impedance Input Amplifier; The 20 Hz - 20 MHz 1 MΩ front panel BNC connector J2 applies an input RF signal to the input of FET amplifier A12Q1 and Q2, which is capacitor coupled to a high gain operational amplifier A12U1. The operational amplifier outputs to an emitter follower A12Q3 which is capacitor coupled to a differential amplifier comprised of A12Q4 and Q5. Potentiometer A12R13 adjusts the base bias of A12Q4, and is set to provide a LOW band input sensitivity of <10 millivolts rms. The collector of A12Q5 outputs to a TTL compatible logic translator comprising A12Q6 and Q7, which outputs to the 500 MHz Decade Assembly A4 via A12 pin Ⓣ.

2. Resolution and Function Selector Switch Encoding Logic; The switch selected resolution ground enables are applied to three 4-input NAND gates (A12U3-6, U3-8 and U2-6). These gates encode the one-of-seven selected resulution into a three-line 1-2-4 octal code which is applied to the A, B, and C inputs of a filed programmed read only memory (PROM) A12 U4. Table 4-1 provides the one-of-seven to 1-2-4 encode truth table which defines the encoding logic.

**Table 4-1 Resolution Select Encode Truth Table**

| RESOLUTION | BIT 1 (A) | BIT 2 (B) | BIT 4 (C) |
|---|---|---|---|
| 1 μs | 1 | 1 | 1 |
| 10 μs | 0 | 1 | 1 |
| 100 μs | 1 | 0 | 1 |
| 1 ms | 0 | 0 | 1 |
| 10 ms | 1 | 1 | 0 |
| 100 ms | 0 | 1 | 0 |
| 1s | 1 | 0 | 0 |

Gate A12U7-3 OR's the $\overline{\text{WIDE}}$ and $\overline{\text{NORMAL}}$ function switch selections which is inputted to the E input of the PROM at A12U4-14. This gate generated $\overline{\text{WIDE+NORMAL}}$ is also applied to gate A12 U8-3 where it is AND gated with the $\overline{\text{LOW PASS}}$ signal from the low pass detector circuit located in Assembly A4. The AND gate A12U8-3 outputs the $\overline{\text{20-500}}$ flag which is routed to the 500 MHz Decade Assembly A4 via A12 pin $\boxed{11}$, this $\overline{\text{20-500}}$ signal is also applied to A12U2-8 gate which inverts it to a 20-500 signal for input to the PROM's D input at A12U4 pin 13. The PROM (A12U4) outputs decimal point location data in a 1-2-4-8 BCD format, which is routed to the Display PC Assembly A3, BCD Option 04 Assembly A2 and Count Chain Decade Assemblies A1 and A3, via A12 pin $\boxed{D}$, $\boxed{N}$ $\boxed{12}$ and $\boxed{10}$ respectively. Also generated by the PROM is unit of measurement data which is outputted as MHz, kHz, and GHz on A12U4 pins 6, 7 and 8 respectively. These unit of measurements are inverted by Buffer/drivers A12U14 to ground return enables for the unit of measurement lamps A13DS4, 5 and 6. The discrete unit of measurement signals are gated into a 1-2-4 BCD MU by gates A12U13-3 and 6 and outputted by the BCD Option 04 Assembly A2 via A12 pins $\boxed{17}$, $\boxed{16}$, and $\boxed{5}$. The flags that are gate logic generated are listed and defined as follows:

1. $\overline{\text{CHANGE CLEAR}}$ A12 pin $\boxed{15}$; A clear (reset) command to the Function PCB Assembly A11, that signifies a switch selected function or resolution has been made, or Low Pass detection has been made by the 500 MHz Decade PCB Assembly A4.

2. CLEAR ACTO A12 pin $\boxed{18}$; A clear (reset) command to the N Computer PCB Assembly A10, that signifies that WIDE (ACTO) function has been switch selected, or some other parameter has changed.

3. $\overline{\text{ACTO}}$ A12 pin $\boxed{\text{E}}$; A flag to the Function PCB Assembly A11, that signifies ACTO mode has been select initiated.

4. $\overline{\text{P.L.}}$ A12 pin $\boxed{13}$; A flag to the Function and N Computer PCB's A11 and A10, that signifies the phase lock FLACTO operation has been selected.

5. $\overline{\text{F.L.}}$ A12 pin $\boxed{\text{L}}$; A flag to the Function and N Computer PCB's A11 and A10, that signifies the frequency lock ACTO operation has been selected.

## 4.25 DISPLAY PCB ASSEMBLY A13

The display PCB Assembly (see figure 7-21 schematic diagram), provides a visual eleven digit readout of the measurement, which is supported by a visual annunciation of the measurement unit (MU) as kHz, MHz or GHz. The count from the Count Chain is applied as a 44-bit BCD word to the eleven BCD to Seven Segment Decoder/Drivers A13U1 through A13U11. The LSD ($10^0$) Decoder/Driver A13U11 has a $\overline{\text{BLINK}}$ signal applied to pin 4 when an overload flag is generated to flash the LSD of the display. The A13U1 through A13U10 pin 4 input blanks any leading zeros from the display. The L.T. (lamp test) signal applied at A13 pin ⑤ will force all seven segments of the eleven decades to illuminate thus providing a display readout of all eights as a test function.

The eleven seven segment LED numerical display indicator IC's, A13DS7 through A13DS17 will illuminate when a logic low is applied to the individual LED segment. The BCD-to-One of Ten Decoder/Driver A13U12, decodes the 4-bit BCD decimal point (DP) data to an one of ten line output which is applied to the ten LSD's of the display to illuminate the decimal point. .

The annunciator sub-assembly provides a back lighted transparency that displays the kHz, MHz, GHz measurement unit captions, and the REMOTE and GATE captions. These captions are illuminated by incandescent lamps: REMOTE, A13DS1 and A13DS2; GATE, A13DS3; kHz, A13DS4; MHz, A13DS5; and GHz, A13DS6.

## 4.26 ACTO MODULE ASSEMBLIES

The ACTO module assemblies A14 through A17 consists of PCB's mounted inside of cast RFI inclosures. The right half (component side) of the RFI inclosures have interstage RF shields integrated into the castings. The left half (circuit side) of the inclosures mount the SMA push-on RF connectors allowing intra ACTO section RF signal cabling. A cutout is provided in the case inclosures allowing PCB edge connector interface with the counter section of the instrument. The two halves of the inclosures are jointed and RF sealed by a continuous one piece RFI braid and thirteen 4-40 X 3/8 screws.

## 4.27 N IF ACTO MODULE ASSEMBLY A14

The N IF assembly generates the 1 kHz X N signal by mixing the IF output from the N Mixer assembly U3 with the LOCK IF signal from the Lock IF assembly A17 (see figure 7-24 N IF PCB assembly schematic diagram). The IF from the N Mixer assembly is applied to A14J1 which inputs to a three stage cascaded 30 MHz wide band IF amplifier composed of FET's A14Q1, Q2 and Q3 with their associated LCR components, the dotted lines on the schematic depicts the external and interstage shielding provided by the inclosure casting.

FET A14Q3 outputs to the wide band IF Amplifier A14U1. The IF output at A14U1-6 is coupled by capacitor A14C33 to the mixer A14U2. A14 U2 is an MC1496G monolithic balanced mixer, which consists of an input differential amplifier driving a pair of synchronized single-pole, double-throw switches. These switches are transistor current-mode gates with cross-coupling allowing full-wave balanced multiplication of the LOCK IF signal applied to pins 1 and 4, and the N IF signal applied to pin 8 is the switching signal. The output at pin 9 is the product of the inputs and is identified as the 1 kHz X N signal. The mixers output 1 kHz X N signal is coupled via capacitor A14C48 to the emitter follower TTL level translator A14-Q4, which outputs to the N Computer Assembly A10 via A14U3-8 a Schmitt trigger/inverter and connector XA14 pin H. The 1 kHz X N signal is also applied to the AGC circuit comprised of A14-Q5 and Q6, which develops the AGC level that is applied to gate 1 of the second stage of the IF Amplifier (A14Q2).

A14U1-6 IF output is also coupled by capacitor A14C50 and the Schottky diode A14CR1 to pin E IF Alignment.

## 4.28 SEARCH OSCILLATOR ACTO MODULE ASSEMBLY A15

The Search Oscillator Module (see figure 7-27 Search Oscillator PCB Assembly schematic diagram) is divided into four functional circuits, which are shielded by an RFI inclosure. The dotted lines on the schematic diagram depicts the external and inter-circuit shielding provided by the inclosure casting. Table 4-2 provides information of the Search Oscillator functional circuits and their input and output signals.

The Level Detector circuit is comprised of A15U1, A15Q1, and A15U2 and associated RC components. The DETECTOR OUTPUT signal is applied to operational amplifier A15U1 via SMA connector A15J1. The gain of the operational amplifier

TABLE 4-2 SEARCH OSCILLATOR FUNCTIONAL CIRCUIT INFORMATION

| CIRCUIT | INPUT SIGNAL(S) | OUTPUT SIGNAL(S) |
|---|---|---|
| Level Detector | A15J1 DETECTOR OUTPUT from Power Divider Detector U2. | A15J2 AGC, to PIN Leveler U1.<br>A15 pin A OVERLOAD flag, to Function PCB Assembly A11 pin $\boxed{17}$. |
| 1 kHz Generator | A15 pin B $\overline{\text{N COMPUTED}}$ flag, from N Computer PCB Assembly A10 pin ⑦. | A15 pin E 1 kHz 0°, to L.O./Shifter Module A16 pin 2.<br>A15 pin C 1 kHz 90°, to L.O./Shifter Module A16 pin 1.<br>A15 pin 6 1 kHz SQUARE WAVE, to N Computer PCB A10 pin ⑩. |
| Phase Detector | A15 pin 10 VCO/N, from 10 kHz Generator PCB Assembly A9 pin ⑯.<br>A15 pin F 10 kHz COMPUTER flag, from N Computer PCB Assembly A10 pin ⑤.<br>A15 pin L 10 kHz from N Computer PCB Assembly A10 pin ⑨. | A15U6-6 PHASE DETECTOR OUTPUT, to A15U10-2. |
| Search Oscillator/VCO Control | A15 pin 1 SQUELCH, from N Computer PCB Assembly A10 pin ⑥.<br>A15 pin 2 DISCRIMINATOR OUTPUT from Lock IF Module A17 pin Ⓚ. | A15 pin K SQUELCH COUNTER to N Computer PCB Assembly A10 pin ⑬.<br>A15 pin 9 VCO CONTROL (RAMP), to L.O./Shifter Module A16 pin Ⓚ. |

is adjusted by potentiometer A15R3 which sets the AGC level, and transistor A15Q1 provides the output AGC drive to the PIN leveler U1 as the PIN CONTROL voltage via connector A15J2. Transistor A15Q1 also applies the AGC level to operational amplifier A15U2 which will generate the OVERLOAD flag when an input of >+20 dBm is applied to the counters HF input connector. Potentiometer A15R8 sets the threshold of the OVERLOAD indication.

The 1 kHz Generator circuit is comprised of A15-U3 and U4 configured as a 1 kHz oscillator, the oscillator gate circuit (A15Q2 and Q3), and the square wave shaper circuit (A15Q4 and Q5). The 1 kHz oscillator outputs two 1 kHz sine waves deplaced 90° in phase tothe L.O. module A16 via A15 pins E and C. When the $\overline{\text{N COMPUTED}}$ flag is set high at A15 pin B the 1 kHz oscillator is gated off by a ground level being placed on A15U4-8. The 1 kHz sine wave is converted to a TTL square wave by the shaper circuit (A15Q4 and Q5) and outputted to the N Computer PCB assembly A10 via A15 pin 6.

The Phase Detector circuit is comprised of the phase detector (A15U5), the lead-lag RC filter (A15R33 through R39, A15C23 and C24) and differential amplifier (A15U6). The 10 kHz signal from the N Computer is applied to the phase detector V input (A15U5-3) and the VCO/N signal from the 10 kHz Generator is applied to the R input (A15U5-1). When the phase detector negative transitions of the V and R inputs are equal in frequency and phase, both outputs (UF and DF) are set high and the loop is locked. If the V input is lower in frequency or lags in phase, the UF output will go low; conversely the DF output will go low when the V input is higher in frequency or leads the reference in phase. The lead-lag RC filter, filters out the 10 kHz, thus providing a dc voltage level that is proportional to the phase error. The lead-lag RC filter inputs into the differential amplifier (A15U6), which output controls the VCO L.O. frequency and locks it to a 10 kHz increment of the N number. The 10 kHz COMPUTED flag inputted at A15 pin F is applied to A15U6-8 via A15Q6 and FET A15Q10 as a phase lock enabling control.

When the phase lock loop is not locked, the search oscillator circuit (A15U7, U8 and U9), will generate a ramp signal. This ramp is amplified by A15-U10 and outputted to the L.O. Module A16 via A15 pin 9 as the VCO CONTROL signal. Two potintiometer adjustments SWEEP LIMIT (A15R44) and DC LEVEL SHIFT (A15R57) provide for ramp alignment. Figure 4-14 depicts the search oscillator ramp signal at A15 pin 9 and its alignment of sweep and offset.

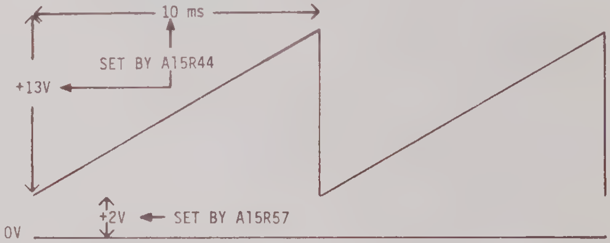


FIGURE 4-14 SEARCH OSCILLATOR RAMP

When the counter is operating in the wide band mode (ACTO) the search oscillator will lock up on the LOCK IF DISCRIMINATOR signal applied to A15 pin 2, when the SQUELCH is inputted as a gate enable at A15 pin 1. Potentiometer A15R30 set the Lock IF threshold level to the source of FET A15Q9. This configuration allows an AFC voltage to be outputted at A15 pin 9 to set up a high gain AFC loop to maintain the IF at 30 MHz.

### 4.29 LOCAL OSCILLATOR AND SHIFTER ACTO MODULE ASSEMBLY A16

The L.O./Shifter Module (see figure 7-30 L.O. and Shifter PCB Assembly schematic diagram) is divided into four functional circuits, a VCO, a SSB Generator and a pair of output Amplifier/Drivers, which are shielded by an RFI inclosure. The dotted lines on the schematic diagram depects the external and inter-circuit shielding provided by the inclosure casting.

The VCO is comprised of A16Q1 and its associated RCL components. Varicap A16CR1 is the frequency controlling device and is controlled by the VCO control voltage from the Search Oscillator Module A15 that is inputted at A16 pin K. Integrated circuit A16U1 and series regulator A16Q3 provides a

+12 volt regulated power supply for the VCO. Transistor A16Q2 is a logic level translator/driver which supplies an ECL compatible output to the SSB generator (shifter) circuits.

The VCO output is coupled via A16C15 to the clock inputs of A16U2 and U3, which are type MC1690 ECL D master-Slave high speed flip-flops having toggle rates of over 500 MHz. The Q and $\overline{Q}$ outputs of A16U3 is applied to OR/NOR gate configuration comprised of A16U4, which outputs L.O. signals as twin lines to the 500 MHz Decade Assembly A4 and the 10 kHz Generator A9. Pin 12 of A16U4 is a common input to all gate elements and is used as an L.O. inhibit, on the presences of a $\overline{\text{LOW PASS}}$ input at A16 pin C, which sets a logic low via transistor A16Q4 and A16U4-12. The gate output at A16U4-15 is applied to the lock mixer L.O. Amplifier/Driver circuit comprised of A16Q6, Q7 and associated RCL components, which outputs to the Lock Mixer A18 via SMA connector A16J2.

The main function of the SSB generator (shifter) circuit is to develop an output for the N mixer that is one kHz higher than the local oscillator frequency. This 1 kHz shift is generated by A16U5 and U6 which are MC1496G monolithic balanced mixers, each of these mixers consists of an input differential amplifier driving a pair of synchronized single-pole, double-throw switches. These switches are transistor current-mode gates with cross-coupling allowing full-wave balanced multiplication of the 1 kHz 0° and the 1 kHz 90° signals and the local oscillator signals applied to pins 7 and 8 as the switching signals. The outputs at A16U5-6 and A16U6-9 are combined, and the local oscillator frequency and the lower sideband are conceled out, leaving only the upper sideband which provides the 1 kHz shift thus outputting a resultant that is the L.O. + 1 kHz signal. Integrated circuit A16U7 functions as a buffer/inhibit gate, and will inhibit the L.O. + 1 kHz output on the presences of LOW PASS, N COMPUTED or N INHIBIT inputs. The gate output (A16U7-14) is applied to the N Mixer L.O. Amplifier/Driver comprised of A16Q8, Q9 and associated RCL components, which output the L.O. + 1 kHz signal to the N Mixer A19 via SMA connector A16J1.

## 4.30 LOCK IF ACTO MODULE ASSEMBLY A17

The Lock IF Module (see figure 7-33 Lock IF PCB Assembly schematic diagram) is comprised of three functional circuits; the Lock IF Amplifier, the Squelch Detector, and the IF Frequency Discriminator.

The 30 MHz Lock IF Amplifier has a band-pass of 10 MHz and is configured by three dual gate FET amplifier stages (A17Q1, Q2 and Q3) followed by a 30 MHz wide band operational amplifier stage (A17U1). The 10 MHz overall band-pass is achieved by stagger tuning the first three IF stages, refer to Chapter 5 paragraph 5-13 LOCK IF A17 INITIAL ALIGNMENT for the trimmer capacitor callouts and alignment procedure. Potentiometer A17R20 is the AGC level adjustment for the Lock IF chain and is normally set for IF lock-on at a -18 dBm counter input signal level.

The Lock IF output at A17U1-6 is dc coupled to the gate input of the squelch input FET amplifier (A17Q4). Its output is applied via a tuned 30 MHz LC coupling to the squelch level detector (A17U2), potentiometer A17R27 provides the SQUELCH THRESHOLD adjustment. The squelch detector outputs via amplifier/TTL level translator A17Q5 and Q6 to the N Computer PCB Assembly A10 at XA17 pin A.

The Lock IF output at A17U1-6 is also coupled via A17C32 to pin 15 of exclusive OR/NOR gate A17 U3 and its outputs pins 2 and 3 provide a twin line ECL Lock IF signal to the 500 MHz Decade PCB Assembly A4 and the N IF ACTO Module Assembly A14. The inverted output A17U3-12 inputs to the IF Discriminator circuit via delay line A17DL1. The delay line provides a 180° phase shift of the 30 MHz IF applied to the discriminator gate input A17U3-7. The inverted and non-inverted discriminator gate outputs A17U3 pins 11 and 10 feed the differential amplifier A17Q7 and Q8 through the LC tank circuits. The discriminators output at the collector of A17Q8 is applied to operational amplifier A17U4 which outputs to the Search Oscillator Module Assembly A15. The discriminator also feeds an amplifier driver circuit comprised of A17Q9 and Q10 which provides a discriminator output to the rear panel DISCRIMINATOR OUT

BNC connector J3. Potentiometer A17R49 provides a means of adjusting the discriminator output to zero volts at the 30 MHz IF cross over point. Figure 4-15 provides a plot of the discriminator output in volts verses the frequency deviation in MHz.

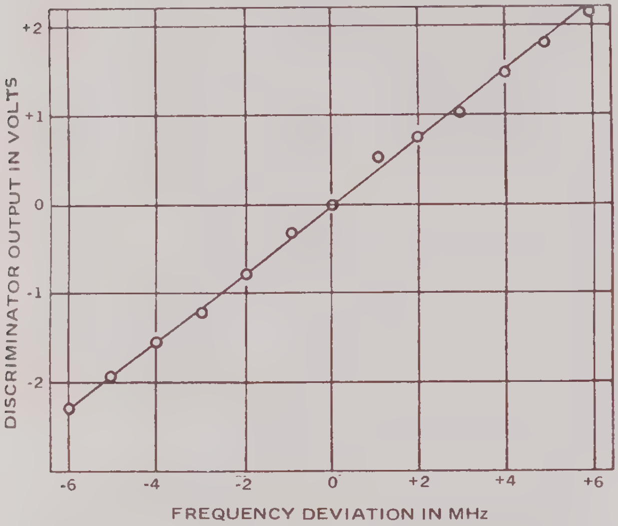


**Figure 4-15 Discriminator Output/Frequency Deviation**

## 4.31 MIXERS U3 AND U4

Mixers U3 and U4 are identical microwave sampling circuits employing conventional sampling techniques to reduce the input frequency to a frequency that may be counted using direct counting techniques. U3 is employed as the lock mixer and develops the locked IF signal. U4 is used as the N mixer and develops the mixer output signal to be direct counted. Table 4-3 describes the input/output functions of the samplers.

**TABLE 4-3 SAMPLER FUNCTION INFORMATION**

| CIRCUIT | INPUT | OUTPUT |
|---|---|---|
| U3 Lock Mixer | U3J1 RF input from U2.<br>U3J3 Lock LO input from A16J2. | U3J2 Lock IF to A17J1.<br>U3J4 50Ω termination to U4. |
| U4 N Mixer | U4J1 RF input from U2.<br>U4J3 shifted LO input from A16J1. | U4J2 N IF to A14J1.<br>U4J4 Mixer output to A4 via 6 dB pad U3. |

NOTE: Samplers U3 and U4 are identical and interchangeable. The only port identified is J3 and this is identified LO. J numbers are assigned on the block only

## 4.32 500 MHz PREAMPLIFIER

The 500 MHz Preamp is a common emitter broadband, 20 MHz to 500 MHz, amplifier with an approximate 12 dB gain.

## 4.33 POWER DIVIDER AND DETECTOR U2

U2 consists of a balance T and RF Detector. It accepts RF inputs from the pin leveler U1, splits it for distribution to the samplers and provides a detected output signal to the level detector circuits in A15.

## 4.34 PIN LEVELER U1

U1 is a broadband solid state RF control device used both as a coupler and a variable attenuator. It consists of a straight through transmission line using PIN diodes in shunt for level control attenuation. The impedance of the device is controlled by the feedback signal (PIN control output from A15) applied to the control port. Input signals within the power range of the device develop little or no feedback and the PIN diodes appear as a high impedance 50 ohm load across the line. This constitutes a minimum attenuation condition with optimum coupling. As the input signal level increases the feedback control level will increase thereby turning on the PIN and adversely affecting the line impedance. The resulting discontinuity reflects most of the incident power increasing the attenuation.

## 4.35 MODEL 6054B POWER SUPPLY

The Model 6054B power supply consists of three PCB assemblies and main chassis and rear panel mounted components (see figure 7-40 power supply schematic diagram and figure 4-16 power supply functional schematic diagram). The power supply provides ten outputs which are listed in Table 4-4, with their related rectifiers and regulator elements.

The rear panel assembly mounts the input power receptacle/line filter (U5), the main power fuse (F1), the optional oscillator power fuse (F2), the 115/230 volt line selector slide switch (S6) and the blower (B1). The main power OFF/ON toggle switch (S1) is mounted on the front panel, (see figure 7-1 interconnect block diagram).

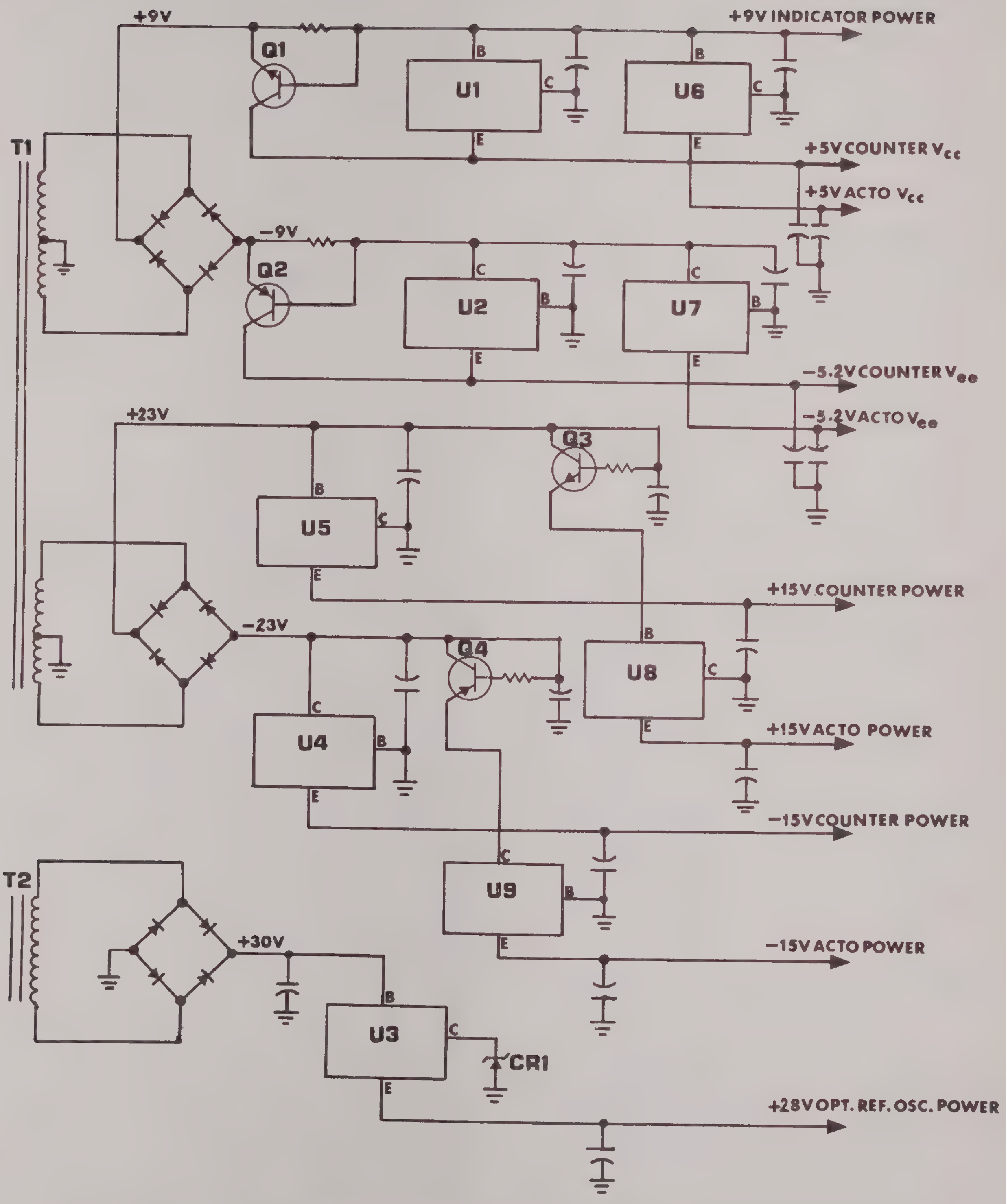

+9V
+9V INDICATOR POWER
Q1
B
U1
C
B
U6
C
E
E
+5V COUNTER Vcc
+5V ACTO Vcc
T1
-9V
Q2
C
U2
B
C
U7
B
E
E
-5.2V COUNTER Vee
-5.2V ACTO Vee
+23V
Q3
B
U5
C
E
+15V COUNTER POWER
-23V
Q4
B
U8
C
C
U4
B
E
+15V ACTO POWER
-15V COUNTER POWER
C
U9
B
T2
E
-15V ACTO POWER
+30V
B
U3
C
CR1
E
+28V OPT. REF. OSC. POWER

FIGURE 4-16 MODEL 6054B POWER SUPPLY FUNCTIONAL SCHEMATIC DIAGRAM

## TABLE 4-4 MODEL 6054B POWER SUPPLY INFORMATION

| POWER SUPPLY OUTPUT VOLTAGE AND FUNCTION | BRIDGE RECTIFIER | REGULATOR TRANSISTOR | IC REGULATOR |
|---|---|---|---|
| +9 Volt Indicator Power | Diode PC Assy 05389001 | None | None |
| +5 Volt Counter Vcc | Diode PC Assy 05389001 | Q1 (MJ2500) | U1 (LM309K) ) |
| +5 Volt ACTO Vcc | Diode PC Assy 05389001 | Q1 (MJ2500) | U6 (MC7805CP) ) |
| -5.2 Volt Counter Vee | Diode PC Assy 05389001 | Q2 (MJ3000) | U2 (LM320K-5.2) |
| -5.2 Volt ACTO Vee | Diode PC Assy 05389001 | Q2 (MJ3000) | U7 (MC7905-5.2CP) |
| +15 Volt Counter Power | CR5–8 | None | U5 (MC7815CP) |
| +15 Volt ACTO Power | CR5–8 | Q3 (2N5190) | U8 (MC7815CP) |
| -15 Volt Counter Power | CR5–8 | None | U4 (MC7915CP) |
| -15 Volt ACTO Power | CR5–8 | Q4 (2N5139) | U9 (MC7915CP) |
| +28 Volt Opt. Ref. Oscillator Power | Counter P.S. Reg. Assy 0533401 (4 each 1N4005) | None | U3 (MC7815CP) |

The 115/230 line voltage selector switch configures the power supply transformers (T1 and T2) primary windings for a parallel connection when placed in the 115 position and for a series connection when placed in the 230 position. Front panel POWER OFF/ON switch applies ac line voltage to the primary windings of transformer T1. The primary windings of the transformer T2 are connected to the line input via switch S6 and fuse F2 to allow +28 volts to be applied to the optional 3 MHz T.B. oscillator whenever the counter is plugged into the line source, regardless of the state of the POWER OFF/ON switch S1. When the standard 10 MHz T.B. oscillator is installed its +5 volt power is applied via the +5 volt counter Vcc power supply and is controlled by the POWER OFF/ON switch S1.

### 4.36 OPTION 04 BCD OUTPUT PCB ASSEMBLY A2 AND REMOTE PCB ASSEMBLY A5

System interface for computer or semi-computer application, option 04 provides, complete programmability of all switchable front panel control, with the exception of power, in a single line format. All information displayed on the front panel is outputted in parallel 8-4-2-1 BCD format. This digital output includes all 11 display digits, annunciator, decimal point and lock lamp. Logic levels are +5 volts (nominal), positive true, TTL compatible. A print command is provided for end of measurement (+5 volts nominal). Grounding the inhibit line prevents the counter from making a new measurement.

The BCD Output and Remote Assemblies (see figures 7-47 and 7-49). Outputs 44-bits BCD measurement data, 4-bits BCD decimal point data, 3-bits BCD measurement unit (MU) data and the following single line flag signals, OVERLOAD, OVERRANGE, EOC (PRINT COMMAND). to a remote device, via open collector Buffers A2U1 through A2U9. These buffer outputs are applied to the rear panel connectors A2/A5J1 and A2/A5J2. A RESET INHIBIT from the remote device is level translated and inverted by A2Q1 and Q2 to the $\overline{\text{INHIBIT RESET}}$ command.

The remote PCB assembly A5 provides for the remote control of the counters operation by a remote device or system (see figure 7-47 schematic diagram) When a logic low REMOTE is applied at the BCD/REMOTE connector J2 pin 35 inverter A5U1-6 will apply a logic high to the enable gates of the tri-state buffers A5U2 through A5U5 to allow entry of the remote control functions. The $\overline{\text{REMOTE}}$ input also will set the RESET COMMON, FUNCTION

COMMON and RESOLUTION COMMON to logic high thus inhibiting local front panel switch selection. The $\overline{\text{REMOTE LAMP}}$ at A5 pin Ⓑ will go to a logic low when the $\overline{\text{REMOTE}}$ or $\overline{\text{L.T.}}$ inputs are placed low. The $\overline{\text{LOCK}}$ signal from the Function PCB assembly A11 is applied to A5 pin ⑰ and inverted to LOCK by A5U6-6 and outputted via A2/A5J2 pin 16 to the remote device.

The Rear panel BCD and REMOTE (A2/A5J1 and A2/A5J2) connectors provide the 04 option interface between the 04 option A2 and A5 PCB assemblies and the remote device or system. Tables 4-5 and 4-6 provide the BCD and REMOTE connectors pin callouts with function or signal name and to and from the interface data.

### TABLE 4-5 BCD/REMOTE A2/A5J1 INTERFACE

| A2/A5J1 PIN NO | FUNCTION | TO | FROM | FUNCTION(S) | ASSY-PIN NO |
|---|---|---|---|---|---|
| 1 | $10^0$ BIT "1" | | A2-5 | $10^0$ BIT "1" | A2-⑥ |
| 2 | $10^0$ BIT "2" | | A2-3 | $10^0$ BIT "2" | A2-⑤ |
| 3 | $10^1$ BIT "1" | | A2-37 | $10^1$ BIT "1" | A2-⑩ |
| 4 | $10^1$ BIT "2" | | A2-7 | $10^1$ BIT "2" | A2-⑨ |
| 5 | $10^2$ BIT "1" | | A2-12 | $10^2$ BIT "1" | A2-⑮ |
| 6 | $10^2$ BIT "2" | | A2-38 | $10^2$ BIT "2" | A2-⑭ |
| 7 | $10^3$ BIT "1" | | A2-20 | $10^3$ BIT "1" | A2-$\boxed{4}$ |
| 8 | $10^3$ BIT "2" | | A2-18 | $10^3$ BIT "2" | A2-$\boxed{3}$ |
| 9 | $10^4$ BIT "1" | | A2-52 | $10^4$ BIT "1" | A2-$\boxed{9}$ |
| 10 | $10^4$ BIT "2" | | A2-49 | $10^4$ BIT "2" | A2-$\boxed{8}$ |
| 11 | $10^5$ BIT "1" | | A2-14 | $10^5$ BIT "1" | A2-$\boxed{14}$ |
| 12 | $10^5$ BIT "2" | | A2-13 | $10^5$ BIT "2" | A2-$\boxed{13}$ |
| 13 | $10^6$ BIT "1" | | A2-31 | $10^6$ BIT "1" | A2-Ⓕ |
| 14 | $10^6$ BIT "2" | | A2-33 | $10^6$ BIT "2" | A2-Ⓔ |
| 15 | $10^7$ BIT "1" | | A2-39 | $10^7$ BIT "1" | A2-Ⓜ |
| 16 | $10^7$ BIT "2" | | A2-8 | $10^7$ BIT "2" | A2-Ⓛ |
| 17 | MU BIT "1" | | A2-24 | MU BIT "1" | A2-$\boxed{R}$ |
| 18 | MU BIT "2" | | A2-16 | MU BIT "2" | A2-$\boxed{15}$ |
| 19 | DECIMAL BIT "1" | | A2-2 | DECIMAL BIT "1" | A2-Ⓑ |
| 20 | DECIMAL BIT "2" | | A2-4 | DECIMAL BIT "2" | A2-Ⓒ |
| 21 | N.C. | | | | |
| 22 | N.C. | | | | |
| 23 | N.C. | | | | |
| 24 | LO REF | | A2-28 | (INTERNAL TO PCB) | A2R4 |
| 25 | HI REF | | A2-27 | (INTERNAL TO PCB) | A2R4 |
| 26 | $10^0$ BIT "4" | | A2-32 | $10^0$ BIT "4" | A2-⑦ |
| 27 | $10^0$ BIT "8" | | A2-30 | $10^0$ BIT "8" | A2-⑧ |
| 28 | $10^1$ BIT "4" | | A2-36 | $10^1$ BIT "4" | A2-⑫ |
| 29 | $10^1$ BIT "8" | | A2-11 | $10^1$ BIT "8" | A2-⑬ |

## TABLE 4-5 BCD/REMOTE A2/A5J1 INTERFACE (Contd)

| A2/A5J1 PIN NO | FUNCTION | TO | FROM | FUNCTION(S) | ASSY-PIN NO |
|---|---|---|---|---|---|
| 30 | $10^2$ BIT “4” | | A2-41 | $10^2$ BIT “4” | A2-⑰ |
| 31 | $10^2$ BIT “8” | | A2-45 | $10^2$ BIT “8” | A2-$\boxed{2}$ |
| 32 | $10^3$ BIT “4” | | A2-22 | $10^3$ BIT “4” | A2-$\boxed{6}$ |
| 33 | $10^3$ BIT “8” | | A2-50 | $10^3$ BIT “8” | A2-$\boxed{7}$ |
| 34 | $10^4$ BIT “4” | | A2-54 | $10^4$ BIT “4” | A2-$\boxed{11}$ |
| 35 | $10^4$ BIT “8” | | A2-56 | $10^4$ BIT “8” | A2-$\boxed{12}$ |
| 36 | $10^5$ BIT “4” | | A2-23 | $10^5$ BIT “4” | A2-$\boxed{16}$ |
| 37 | $10^5$ BIT “8” | | A2-58 | $10^5$ BIT “8” | A2-⑮ |
| 38 | $10^6$ BIT “4” | | A2-38 | $10^6$ BIT “4” | A2-Ⓙ |
| 39 | $10^6$ BIT “8” | | A2-9 | $10^6$ BIT “8” | A2-Ⓚ |
| 40 | $10^7$ BIT “4” | | A2-10 | $10^7$ BIT “4” | A2-Ⓕ |
| 41 | $10^7$ BIT “8” | | A2-42 | $10^7$ BIT “8” | A2-Ⓡ |
| 42 | MU BIT “4” | | A2-43 | MU BIT “4” | A2-$\boxed{M}$ |
| 43 | GROUND | | A2-29 | GROUND | A2-⑱ |
| 44 | DECIMAL BIT “4” | | A2-34 | DECIMAL BIT “4” | |
| 45 | DECIMAL BIT “8” | | A2-6 | DECIMAL BIT “8” | |
| 46 | N.C. | | | | |
| 47 | RESET INHIBIT | A2-1 | | INHIBIT RESET | A2-Ⓘ |
| 48 | PRINT COMMAND | | A2-26 | EOC | A2-$\boxed{T}$ |
| 49 | N.C. | | | | |
| 50 | GROUND | | A2-29 | GROUND | A2-Ⓥ |

Note: N.C. = No Connection.

## TABLE 4-6 BCD/REMOTE A2/A5J2 INTERFACE

| A2/A5J2 PIN NO | FUNCTION | TO | FROM | FUNCTION(S) | ASSY-PIN NO |
|---|---|---|---|---|---|
| 1 | $10^8$ BIT “1” | | A2-46 | $10^8$ BIT “1” | A2-Ⓣ |
| 2 | $10^8$ BIT “2” | | A2-40 | $10^8$ BIT “2” | A2-Ⓢ |
| 3 | $10^9$ BIT “1” | | A2-47 | $10^9$ BIT “1” | A2-$\boxed{E}$ |
| 4 | $10^9$ BIT “2” | | A2-19 | $10^9$ BIT “2” | A2-$\boxed{D}$ |
| 5 | $10^{10}$ BIT “1” | | A2-55 | $10^{10}$ BIT “1” | A2-$\boxed{L}$ |
| 6 | $10^{10}$ BIT “2” | | A2-53 | $10^{10}$ BIT “2” | A2-$\boxed{R}$ |
| 7 | N.C. | | | | |

## TABLE 4-6 BCD/REMOTE A2/A5J2 INTERFACE (Cont'd)

| A2/A5J2 PIN NO | FUNCTION | TO | FROM | FUNCTION(S) | ASSY PIN NO |
|---|---|---|---|---|---|
| 8 | N.C. | | | | |
| 9 | $\overline{1\ \mu\text{s}}$ | A5-14 | | $\overline{1\ \mu\text{s}}$ | A5-Ⓛ |
| 10 | $\overline{10\ \mu\text{s}}$ | A5-10 | | $\overline{10\ \mu\text{s}}$ | A5-Ⓚ |
| 11 | $\overline{100\ \mu\text{s}}$ | A5-11 | | $\overline{100\ \mu\text{s}}$ | A5-Ⓙ |
| 12 | $\overline{1\text{ ms}}$ | A5-5 | | $\overline{1\text{ ms}}$ | A5-Ⓗ |
| 13 | $\overline{10\text{ ms}}$ | A5-7 | | $\overline{10\text{ ms}}$ | A5-Ⓕ |
| 14 | $\overline{100\text{ ms}}$ | A5-4 | | $\overline{100\text{ ms}}$ | A5-Ⓔ |
| 15 | $\overline{1\text{s}}$ | A5-3 | | $\overline{1\text{s}}$ | A5-Ⓓ |
| 16 | LOCK | | A5-16 | $\overline{\text{LOCK}}$ | A5-⑰ |
| 17 | N.C. | | | | |
| 18 | OVERLOAD | | A2-25 | OVERLOAD | A2-$\boxed{\text{U}}$ |
| 19 | $10^8$ bit "4" | | A2-44 | $10^8$ bit "4" | A2-$\boxed{\text{B}}$ |
| 20 | $10^8$ bit "8" | | A2-48 | $10^8$ bit "8" | A2-$\boxed{\text{C}}$ |
| 21 | $10^9$ bit "4" | | A2-21 | $10^9$ bit "4" | A2-$\boxed{\text{H}}$ |
| 22 | $10^9$ bit "8" | | A2-51 | $10^9$ bit "8" | A2-$\boxed{\text{J}}$ |
| 23 | $10^{10}$ bit "4" | | A2-15 | $10^{10}$ bit "4" | A2-$\boxed{\text{N}}$ |
| 24 | $10^{10}$ bit "8" | | A2-17 | $10^{10}$ bit "8" | A2-$\boxed{\text{P}}$ |
| 25 | N.C. | | | | |
| 26 | N.C. | | | | |
| 27 | N.C. | | | | |
| 28 | N.C. | | | | |
| 29 | $\overline{\text{NORMAL}}$ | A5-8 | | $\overline{\text{NORMAL}}$ | A5-⑧ |
| 30 | $\overline{\text{WIDE}}$ | A5-12 | | $\overline{\text{WIDE}}$ | A5-⑨ |
| 31 | $\overline{\text{LOW}}$ | A5-9 | | $\overline{\text{LOW}}$ | A5-⑦ |
| 32 | $\overline{\text{TEST}}$ | A5-5 | | $\overline{\text{TEST}}$ | A5-⑥ |
| 33 | $\overline{\text{SAMPLE}}$ | A5-13 | | $\overline{\text{SAMPLE}}$ | A5-⑩ |
| 34 | $\overline{\text{RESET}}$ | A5-2 | | $\overline{\text{RESET P.B.}}$ | A5-⑤ |
| 35 | $\overline{\text{REMOTE}}$ | A5-1 | | RESET COMMON | A5-④ |
| | | | | FUNCTION COMMON | A5-③ |
| | | | | RESOLUTION COMMON | A5-Ⓒ |
| 36 | GND | | A5-15 | GND | A5-Ⓥ |
| | | | | | A5-⑱ |

## 4.37 OPTION 05 DATA INTERCHANGE (IEEE-488 GPIB)

The Data Interface Option 05 permits operation of the Model 6054B from a general purpose interface bus (GPIB) which conforms to IEEE Standard Digital Interface for programmable Instruments - IEEE STD-488-1975.

To implement the 05 option (refer to Figure 7-50 Option 05 IEEE-488 Final Assembly and Block Diagram) a 24-pin metric dimensioned connector J5, the PROG - TALK ONLY switch S1 and a 5-digit ADDRESS switch S2 through S6 are installed on the rear panel of the instrument. The rear panel connector and switches interface via hard wiring to the pads of the Input/Output PCB Assembly 05725402 which contains the "handshake" IEEE-488 logic circuits. The I/O PCB Assembly in turn interfaces with three plug-in PCB Assemblies via hard wirings to their PCB pads. The three plug-in PCB assemblies which are also intraconnected via hard wiring are identified as to name, assembly designator, assembly number and function as follows:

1. IEEE-488 Output PCB, A2, 05725701; converts the 11-digit 1-2-4-8 BCD display data to IEEE-488 DO1 through DO7 message bytes in bit-parallel, byte serial format to the I/O PCB Assembly.

2. IEEE-488 Programming PCB, A5, 05725601; converts IEEE-488 DI1 through DI7 message bytes in bit-parallel byte serial format from the I/O PCB Assembly to a 16-line discrete resolution and mode selection and control signals.

3. IEEE-488 Offset PCB, A7, 05725901; converts IEEE-488 DI1 through DI4 message bytes in bit parallel, byte serial format from the I/O PCB Assembly to a one-of-sixteen customer-specified offset frequencies selections.

IEEE-488 Sample Rate Control PCB A21 Assembly 05788601 contains logic to disable the front panel RECYCLE RATE control and set the recycle rate at ≈100 ms when the Counter is operating in the Remote mode.

Device independent commands are received by the Counter at any time during its operation. The Counter will ignore any device dependent or independent command for which it has not been designed or programmed to respond to. When the Counter is addressed to "Talk", measurement data is transmitted in compliance with IEEE STD-488 'Handshake" process to those devices that are addressed to "Listen".

When the rear panel PROG-TALK ONLY switch is placed in it's TALK ONLY Position the Counter will transmit ASCII coded data in bit parallel byte serial format.

When not addressed to TALK or LISTEN, the Counter monitors the GPIB for instructions. In all three modes: TALK, LISTEN or MONITOR the Counter will update the measurement data.

Figure 4-17 provides a Function Block Diagram of the Option 05 Data Interface, and supports the following description of it's functional operation.

The 6054B Frequency Counter may be used on line (remote) or off line (local). The Remote mode (counter connected to the interface bus system and commanded to remote mode by the controller) enables the Counter to be programmed by the sending device dependent commands during the Counter's "Listen" mode as to the following functions:

- Mode Selection
  - Wide
  - Normal
  - Low
  - Test
- Resolution Selection
  - 1 Hz to 1 MHz in seven decade steps.
- Control
  - Hold
  - Recycle
  - Sample
  - Reset
- Offset Frequency Selection
  - 1 of 16 customer-specified offsets on it's display.

The interface functions implemented are defined by IEEE STD-488 subsets. The following is a list of the subset configuration of the Model 6054B Counter's GPIB:

| | |
|---|---|
| SH1 | Source Handshake, Full |
| AH1 | Acceptor Handshake, Full |
| T7 | Talk, Basic Talker, Unaddressed if MLA, TON function |
| TE0 | Extended Talker, None |
| L4 | Listen, Basic Listener, Unaddressed if MTA |
| LE0 | Extended Listener, None |
| SR0 | Service Request, None |
| RL2 | Remote Local, No LL0 |
| PP0 | Parallel Poll, None |
| DC0 | Device Clear, None |
| DT0 | Device Trigger, None |
| C0 | Controller, None |

The GPIB electrical, mechanical and timing requirements are detailed by IEEE STD-488.

*NOTE*

*For complete details on the interface characteristics refer to IEEE STD-488-1975.*

The bus interface lines are assigned IEEE STD-488 mnemonics which are defined as follows:

DIO1 through DIO8: Data Input/Output lines 1 through 8, transmitted message bytes in bit-parallel, byte-serial format, asynchronously and in a bi-directional manner.

DAV: Data Valid, indicates the availability of data on the DIO lines.

NRFD: Not Ready for Data, indicates when the device is ready to accept data.

ATN: Attention, indicates how the data on the DIO lines is to be interpreted.

IFC: Interface Clear, is used to set the interface system, and the devices connected to it into a known quiescent state.

NDAC: Not Data Accepted, indicates when the data received was accepted.

SRQ: *Service Request, is used to request service from a controller.

REN: Remote Enable, is used by a controller device (in conjunction with other messages generated in the local logic) to place the Frequency Counter in the Remote Mode of operation.

EOI: *End Or Identify, is used to indicate the end of a data transfer or, with the ATN line to execute a polling sequence.

*These lines are not used by the Model 6054B Counter, and are supplied with terminations only.

Table 4-7 provides the pin designation for the Rear Panel GPIB 24-pin connector.

TABLE 4-7 GPIB INTERFACE CONNECTOR

| PIN NO. | IEEE STD-488 MNEMONIC | PIN NO. | IEEE STD-488 MNEMONIC |
|---|---|---|---|
| 1 | DIO1 | 13 | DIO5 |
| 2 | DIO2 | 14 | DIO6 |
| 3 | DIO3 | 15 | DIO7 |
| 4 | DIO4 | 16 | DIO8 (not used) |
| 5 | EOI (not used) | 17 | REN |
| 6 | DAV | 18 | GND (Return) |
| 7 | NRFD | 19 | GND (Return) |
| 8 | NDAC | 20 | GND (Return) |
| 9 | IFC | 21 | GND (Return) |
| 10 | SRQ (not used) | 22 | GND (Return) |
| 11 | ATN | 23 | GND (Return) |
| 12 | GND (Shield) | 24 | GND (Logic) |

The IEEE STD-488 Multiline Interface Messages relate to ASCII code. Table 4-8 provides the IEEE STD-488 DIO bit to ASCII code relationship.

## TABLE 4-8
## IEEE STD-488 DIO CODE TO ASCII CHARACTER

| IEEE STD-488 DIO BIT | | | | | | | ASCII CHARACTER | |
|---|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | LISTEN | TALK |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | SP | |
| 0 | 1 | 0 | 0 | 0 | 0 | 1 | ! | |
| 0 | 1 | 0 | 0 | 0 | 1 | 0 | ” | |
| 0 | 1 | 0 | 0 | 0 | 1 | 1 | # | |
| 0 | 1 | 0 | 0 | 1 | 0 | 0 | $ | |
| 0 | 1 | 0 | 0 | 1 | 0 | 1 | % | |
| 0 | 1 | 0 | 0 | 1 | 1 | 0 | & | |
| 0 | 1 | 0 | 0 | 1 | 1 | 1 | ’ | |
| 0 | 1 | 0 | 1 | 0 | 0 | 0 | ( | |
| 0 | 1 | 0 | 1 | 0 | 0 | 1 | ) | |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | * | |
| 0 | 1 | 0 | 1 | 0 | 1 | 1 | + | |
| 0 | 1 | 0 | 1 | 1 | 0 | 0 | , | |
| 0 | 1 | 0 | 1 | 1 | 0 | 1 | - | |
| 0 | 1 | 0 | 1 | 1 | 1 | 0 | . | |
| 0 | 1 | 0 | 1 | 1 | 1 | 1 | / | |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | |
| 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | |
| 0 | 1 | 1 | 0 | 0 | 1 | 0 | 2 | |
| 0 | 1 | 1 | 0 | 0 | 1 | 1 | 3 | |
| 0 | 1 | 1 | 0 | 1 | 0 | 0 | 4 | |
| 0 | 1 | 1 | 0 | 1 | 0 | 1 | 5 | |
| 0 | 1 | 1 | 0 | 1 | 1 | 0 | 6 | |
| 0 | 1 | 1 | 0 | 1 | 1 | 1 | 7 | |
| 0 | 1 | 1 | 1 | 0 | 0 | 0 | 8 | |
| 0 | 1 | 1 | 1 | 0 | 0 | 1 | 9 | |
| 0 | 1 | 1 | 1 | 0 | 1 | 0 | : | |
| 0 | 1 | 1 | 1 | 0 | 1 | 1 | ; | |
| 0 | 1 | 1 | 1 | 1 | 0 | 0 | < | |
| 0 | 1 | 1 | 1 | 1 | 0 | 1 | = | |
| 0 | 1 | 1 | 1 | 1 | 1 | 0 | > | |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | ? | |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | | @ |
| 1 | 0 | 0 | 0 | 0 | 0 | 1 | | A |
| 1 | 0 | 0 | 0 | 0 | 1 | 0 | | B |
| 1 | 0 | 0 | 0 | 0 | 1 | 1 | | C |
| 1 | 0 | 0 | 0 | 1 | 0 | 0 | | D |
| 1 | 0 | 0 | 0 | 1 | 0 | 1 | | E |
| 1 | 0 | 0 | 0 | 1 | 1 | 0 | | F |
| 1 | 0 | 0 | 0 | 1 | 1 | 1 | | G |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 | | H |
| 1 | 0 | 0 | 1 | 0 | 0 | 1 | | I |
| 1 | 0 | 0 | 1 | 0 | 1 | 0 | | J |
| 1 | 0 | 0 | 1 | 0 | 1 | 1 | | K |

## TABLE 4-8
## IEEE STD-488 DIO CODE TO ASCII CHARACTER (Cont'd)

| IEEE STD-488 DIO BIT | | | | | | | ASCII CHARACTER | |
|---|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | LISTEN | TALK |
| 1 | 0 | 0 | 1 | 1 | 0 | 0 | | L |
| 1 | 0 | 0 | 1 | 1 | 0 | 1 | | M |
| 1 | 0 | 0 | 1 | 1 | 1 | 0 | | N |
| 1 | 0 | 0 | 1 | 1 | 1 | 1 | | O |
| 1 | 0 | 1 | 0 | 0 | 0 | 0 | | P |
| 1 | 0 | 1 | 0 | 0 | 0 | 1 | | Q |
| 1 | 0 | 1 | 0 | 0 | 1 | 0 | | R |
| 1 | 0 | 1 | 0 | 0 | 1 | 1 | | S |
| 1 | 0 | 1 | 0 | 1 | 0 | 0 | | T |
| 1 | 0 | 1 | 0 | 1 | 0 | 1 | | U |
| 1 | 0 | 1 | 0 | 1 | 1 | 0 | | V |
| 1 | 0 | 1 | 0 | 1 | 1 | 1 | | W |
| 1 | 0 | 1 | 1 | 0 | 0 | 0 | | X |
| 1 | 0 | 1 | 1 | 0 | 0 | 1 | | Y |
| 1 | 0 | 1 | 1 | 0 | 1 | 0 | | Z |
| 1 | 0 | 1 | 1 | 0 | 1 | 1 | | [ |
| 1 | 0 | 1 | 1 | 1 | 0 | 0 | | \ |
| 1 | 0 | 1 | 1 | 1 | 0 | 1 | | ] |
| 1 | 0 | 1 | 1 | 1 | 1 | 0 | | ∧ |
| 1 | 0 | 1 | 1 | 1 | 1 | 1 | | — |

The Talk and Listen addresses are selected by the Rear Panel 5-digit address switch. The setting of the 5-digit switch determines which talk address and the corresponding Listen address will be assigned to the Frequency Counter. Thirty-one Talk/Listen addresses may be assigned, refer to Table 4-9 for the address to ASCII Code format.

*NOTE*

*A 1-1-1-1-1 address must not be assigned to any device interfacing the bus; these addresses are reserved for the unlisten ASCII (?) and the untalk ASCII (—) commands.*

**TABLE 4-9 TALK/LISTEN ADDRESS ASSIGNMENTS VS. ASCII CHARACTER**

| ADDRESS SWITCH SETTING BITS | | | | | ASCII CHARACTER | |
|---|---|---|---|---|---|---|
| 5 | 4 | 3 | 2 | 1 | LISTEN | TALK |
| 0 | 0 | 0 | 0 | 0 | SP | @ |
| 0 | 0 | 0 | 0 | 1 | ! | A |
| 0 | 0 | 0 | 1 | 0 | ” | B |
| 0 | 0 | 0 | 1 | 1 | # | C |
| 0 | 0 | 1 | 0 | 0 | $ | D |
| 0 | 0 | 1 | 0 | 1 | % | E |
| 0 | 0 | 1 | 1 | 0 | & | F |
| 0 | 0 | 1 | 1 | 1 | ’ | G |
| 0 | 1 | 0 | 0 | 0 | ( | H |
| 0 | 1 | 0 | 0 | 1 | ) | I |
| 0 | 1 | 0 | 1 | 0 | * | J |
| 0 | 1 | 0 | 1 | 1 | + | K |
| 0 | 1 | 1 | 0 | 0 | , | L |
| 0 | 1 | 1 | 0 | 1 | - | M |
| 0 | 1 | 1 | 1 | 0 | . | N |
| 0 | 1 | 1 | 1 | 1 | / | O |
| 1 | 0 | 0 | 0 | 0 | 0 | P |
| 1 | 0 | 0 | 0 | 1 | 1 | Q |
| 1 | 0 | 0 | 1 | 0 | 2 | R |
| 1 | 0 | 0 | 1 | 1 | 3 | S |
| 1 | 0 | 1 | 0 | 0 | 4 | T |
| 1 | 0 | 1 | 0 | 1 | 5 | U |
| 1 | 0 | 1 | 1 | 0 | 6 | V |
| 1 | 0 | 1 | 1 | 1 | 7 | W |
| 1 | 1 | 0 | 0 | 0 | 8 | X |
| 1 | 1 | 0 | 0 | 1 | 9 | Y |
| 1 | 1 | 0 | 1 | 0 | : | Z |
| 1 | 1 | 0 | 1 | 1 | ; | [ |
| 1 | 1 | 1 | 0 | 0 | < | \ |
| 1 | 1 | 1 | 0 | 1 | = | ] |
| 1 | 1 | 1 | 1 | 0 | > | ^ |
| 1 | 1 | 1 | 1 | 1⊕ | ? | — |

⊕Not to be device assigned

A number of device dependent local message mnemonics and commands are used in the Option 05 schematics and texual description, listed below are these local mnemonics and commands with their functional definitions.

*NOTE*

*Certain local message mnemonics are conveyed as remote message mnemonics and vice versa. These mnemonics and commands may be either true or false, a false logic state is identified by a "not bar" over it's statement.*

DI1 through DI7: Data Input bits 1 through 7.

DO1 through DO7: Data Output bits 1 through 7.

DACI: Data Accepted In.

DACO: Data Accepted Out.

DAVI: Data Valid In.

DAVO: Data Valid Out.

RFDI: Ready For Data In.

RFDO: Ready For Data Out.

PON or PO: Power On.

MLA: My Listen Address

MTA: My Talk Address.

TON: Talk Only.

OTA: Other Talk Address.

GTL: Go To Local.

UNL: Un-Listen.

UNT: Un-Talk.

COMP or ADD COMP: Address Compare.

TALK: Transmit Data.

SPD: Serial Poll Disable.

SPE: Serial Poll Enable.

The IFC command is issued by the controller device and will cause the Counter to monitor the GPIB for further instructions; all data transmission is terminated. If the Counter was addressed as a listener, it will be unaddressed, if it was addressed as a talker, it will be unaddressed. DIO1 through DIO7 lines will go the the tri-state mode.

The REN command is issued by the controller device. If the Counter receives it's listen address while the REN line is active, the Counter will enter it's Remote mode and listen for programming data. All front panel controls will become inoperative.

When the REN line goes inactive, the Counter will enter it's Local mode and the Counter's front panel controls will become operative.

The Counter's addressing process is controlled by the GPIB ATN line. The counter is addressed to Talk or Listen by the controller issuing it's assigned Talk or Listen address while the ATN line is set active. If the Counter was addressed to Talk, and the controller issues a Talk address other than the Counter's assigned Talk address the Counter will automatically deselect itself as a talker. If the Counter was addressed to Talk, and the controller issues the Counter's Listen address, the Counter will automatically deselect as a Talker. If the controller issues an untalk (UNT) ASCII — command, the Counter will automatically deselect as a talker. If the Counter was addressed to Listen and the concontroller issues its Talk address, the Counter will automatically deselect itself as a Listener, and be reassigned as a Talker. If the Counter was addressed to Listen, and the unlisten (UNL) ASCII ? command is issued by the controller, the Counter will deselect as a Listener.

When the Counter is turned on its "wake-up" state is as follows:

1. Counter is placed in the Monitor mode and the DIO1 through DIO7 lines are set in their tri-state mode.

2. The Resolution is set to 1 Hz (ASCII G).

3. The Mode selection is set to NORMAL (ASCII I).

4. The HOLD Control function is selected (ASCII L).

5. The Offset function is programmed to No offset (ASCII P).

Device dependent data can be programmed into the Counter when it's placed in the Remote mode and addressed to Listen. The programmed data may be entered in serial bytes, consisting of 7 parallel bits. The data bytes can be entered in any order and need not be sequenced. Table 4-10 provides the Program format for the Model 6054B Counter.

TABLE 4-10 IEEE STD-488 PROGRAM FORMAT

| BYTE | PROGRAM BITS 7 | 6 | 5 | 4 | 3 | 2 | 1 | ASCII CHARACTER | FUNCTION | GROUP |
|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | @ | 1 MHz | Resolution Selections |
|  | 1 | 0 | 0 | 0 | 0 | 0 | 1 | A | 1 MHz |  |
|  | 1 | 0 | 0 | 0 | 0 | 1 | 0 | B | 100 kHz |  |
|  | 1 | 0 | 0 | 0 | 0 | 1 | 1 | C | 10 kHz |  |
|  | 1 | 0 | 0 | 0 | 1 | 0 | 0 | D | 1 kHz |  |
|  | 1 | 0 | 0 | 0 | 1 | 0 | 1 | E | 100 Hz |  |
|  | 1 | 0 | 0 | 0 | 1 | 1 | 0 | F | 10 Hz |  |
|  | *1 | 0 | 0 | 0 | 1 | 1 | 1 | G | 1 Hz |  |
| 2 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | H | Wide | Mode Selection |
|  | 1 | 0 | 0 | 1 | 1 | 1 | 1 | O | Reset |  |
|  | *1 | 0 | 0 | 1 | 0 | 0 | 1 | I | Normal |  |
|  | 1 | 0 | 0 | 1 | 1 | 1 | 1 | O | Reset |  |
|  | 1 | 0 | 0 | 1 | 0 | 1 | 0 | J | Low |  |
|  | 1 | 0 | 0 | 1 | 1 | 1 | 1 | O | Reset |  |
|  | 1 | 0 | 0 | 1 | 0 | 1 | 1 | K | Test |  |
|  | 1 | 0 | 0 | 1 | 1 | 1 | 1 | O | Reset |  |
| 3 | *1 | 0 | 0 | 1 | 1 | 0 | 0 | L | Hold | Control |
|  | 1 | 0 | 0 | 1 | 1 | 0 | 1 | M | Recycle |  |
|  | 1 | 0 | 0 | 1 | 1 | 1 | 0 | N | Sample |  |
|  | 1 | 0 | 0 | 1 | 1 | 1 | 1 | O | Reset |  |
| 4 | *1 | 0 | 1 | 0 | 0 | 0 | 0 | P | No Offset | Positive Offsets |
|  | 1 | 0 | 1 | 0 | 0 | 0 | 1 | Q | Offset |  |
|  | 1 | 0 | 1 | 0 | 0 | 1 | 0 | R | Offset |  |
|  | 1 | 0 | 1 | 0 | 0 | 1 | 1 | S | Offset |  |
|  | 1 | 0 | 1 | 0 | 1 | 0 | 0 | T | Offset |  |
|  | 1 | 0 | 1 | 0 | 1 | 0 | 1 | U | Offset |  |
|  | 1 | 0 | 1 | 0 | 1 | 1 | 0 | V | Offset |  |
|  | 1 | 0 | 1 | 0 | 1 | 1 | 1 | W | Offset |  |
|  | 1 | 0 | 1 | 1 | 0 | 0 | 0 | X | Offset | Negative Offsets |
|  | 1 | 0 | 1 | 1 | 0 | 0 | 1 | Y | Offset |  |
|  | 1 | 0 | 1 | 1 | 0 | 1 | 0 | Z | Offset |  |
|  | 1 | 0 | 1 | 1 | 0 | 1 | 1 | [ | Offset |  |
|  | 1 | 0 | 1 | 1 | 1 | 0 | 0 | / | Offset |  |
|  | 1 | 0 | 1 | 1 | 1 | 0 | 1 | ] | Offset |  |
|  | 1 | 0 | 1 | 1 | 1 | 1 | 0 | ⁀ | Offset |  |
|  | 1 | 0 | 1 | 1 | 1 | 1 | 1 | - | Offset |  |

*Wake up states

When the Model 6054B Counter is in the Talk mode it outputs data in a 16-byte, 7-bit format in a byte serial, bit parallel sequence. Table 4-11 provides data output sequence as it relates to the data output format and equivalent ASCII characters.

TABLE 4-11 GPIB OUTPUT DATA FORMAT

| | BIT | | | | | | | ASCII CHARACTER | DATA FUNCTION |
|---|---|---|---|---|---|---|---|---|---|
| BYTE | 7 | 6 | 5 | 4 | 3 | 2 | 1 | | |
| 1 | 0 | 1 | 1 | X | X | X | X | 0 → 9 | $10^{10}$ Digit MSD |
| 2 | 0 | 1 | 1 | X | X | X | X | 0 → 9 | $10^{9}$ Digit |
| 3 | 0 | 1 | 1 | X | X | X | X | 0 → 9 | $10^{8}$ Digit |
| 4 | 0 | 1 | 1 | X | X | X | X | 0 → 9 | $10^{7}$ Digit |
| 5 | 0 | 1 | 1 | X | X | X | X | 0 → 9 | $10^{6}$ Digit |
| 6 | 0 | 1 | 1 | X | X | X | X | 0 → 9 | $10^{5}$ Digit |
| 7 | 0 | 1 | 1 | X | X | X | X | 0 → 9 | $10^{4}$ Digit |
| 8 | 0 | 1 | 1 | X | X | X | X | 0 → 9 | $10^{3}$ Digit |
| 9 | 0 | 1 | 1 | X | X | X | X | 0 → 9 | $10^{2}$ Digit |
| 10 | 0 | 1 | 1 | X | X | X | X | 0 → 9 | $10^{1}$ Digit |
| 11 | 0 | 1 | 1 | X | X | X | X | 0 → 9 | $10^{0}$ Digit LSD |
| 12 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | E | Delimiter |
| 13 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | + | Exponent Point |
| 14 | 0 | 1 | 1 | 0 | X | X | X | 0 → 6 | Exponent Value |
| 15 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | CR | Delimiter |
| 16 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | LF | Delimiter |

## 4.38 OSCILLATOR OPTIONS 11, 12 and 13

Increased time base stability is provided when equipped with one of these options. Table 1-2 of Chapter 1 in this manual, outlines the respective stability characteristics.

## 4.39 OPTION 20 REAR PANEL INPUTS

For system applications the Counters front panel connectors are available on the rear panel. Low frequency 20 Hz - 20 MHz BNC connector is paralleled with a second BNC mounted on the rear panel and terminated with 50 ohms. High frequency 20 MHz - 24 GHz SMA connector is removed from the front panel and relocated on the rear panel.

## 4.40 OPTION 27 50-60/400 Hz OPERATION

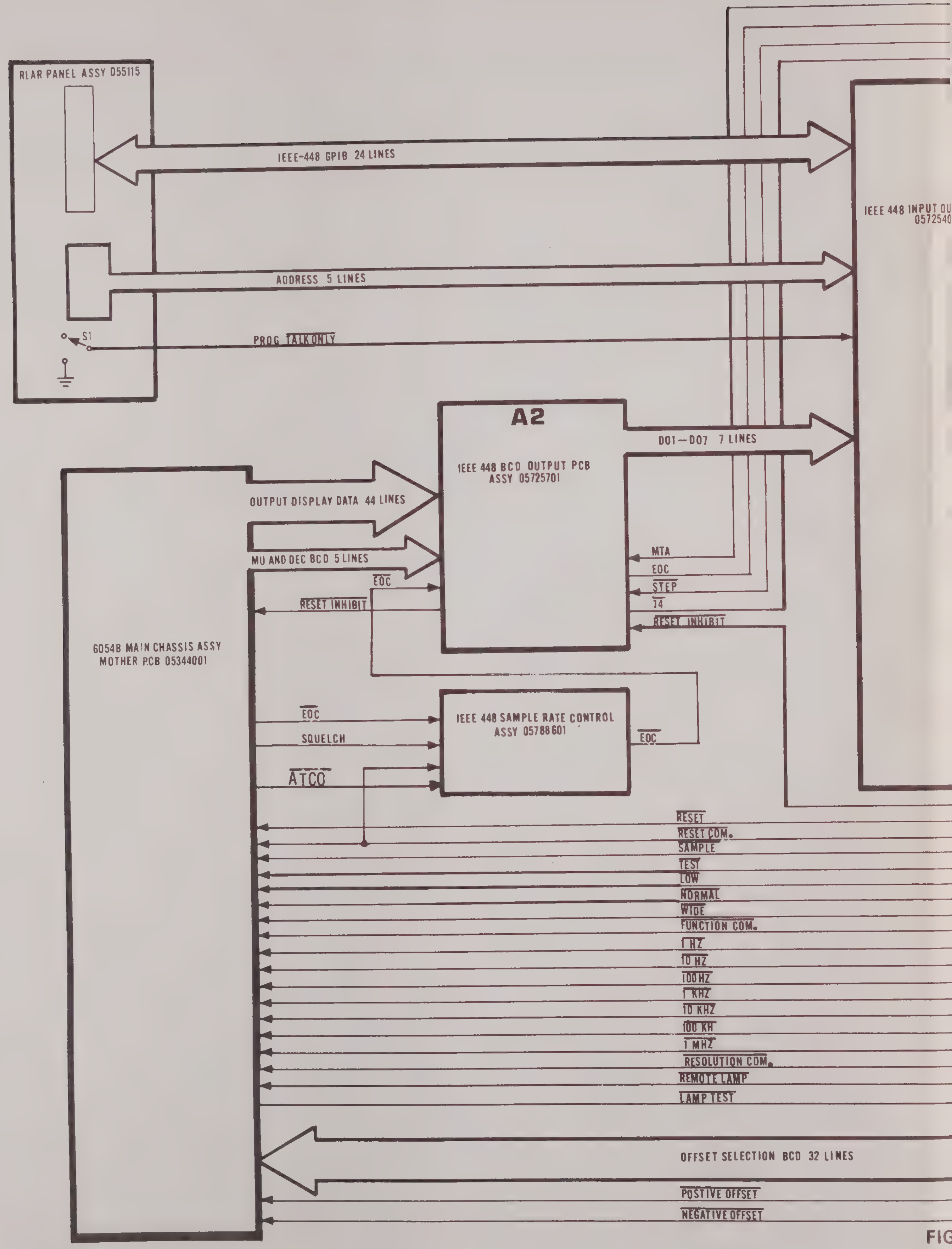
For applications where line frequency is other than 60 Hz, this option allows operation at 50 to 60 Hz and 400 Hz (±10%) without effecting the Counter specifications.

## 4.41 OPTION 28X IF OFFSETS

In many receiver applications the user may desire to have a direct display of the received frequency. Fifteen customer-specified offset frequencies may be selected to add to or subtract from the display.

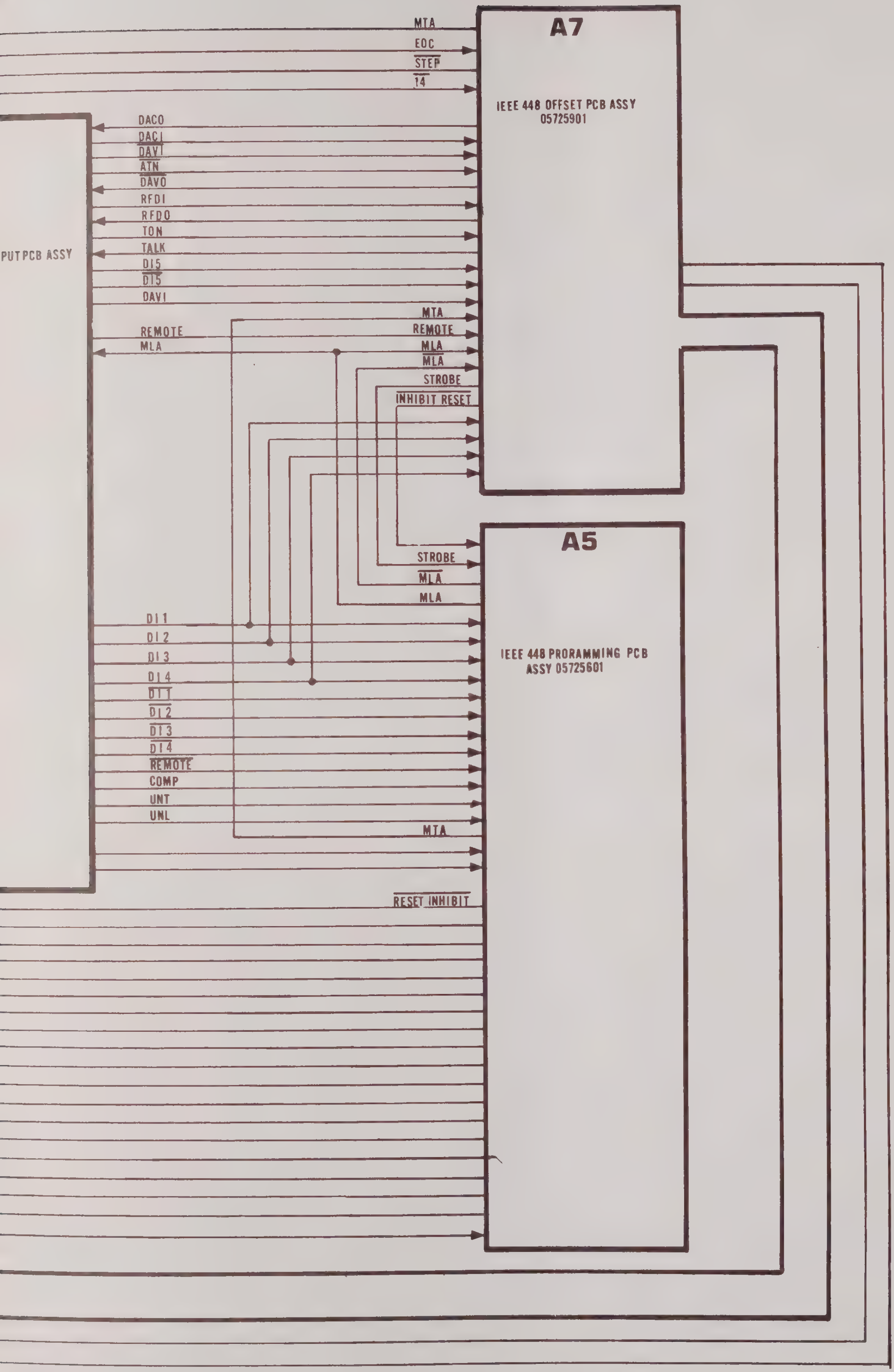
## 4.42 OPTION 18 18 GHz OPERATION

Option 18 provides Type N input connector, replacing the Type SMA. Due to the frequency limitations of a Type N connector the input frequency range is limited to 18 GHz. All operating specifications as listed still apply other than the 18 GHz input frequency limit.


RLAR PANEL ASSY 055115
IEEE-448 GPIB 24 LINES
ADDRESS 5 LINES
S1
PROG TALKONLY
IEEE 448 INPUT OU
0572540
A2
IEEE 448 BCD OUTPUT PCB
ASSY 05725701
D01—D07 7 LINES
OUTPUT DISPLAY DATA 44 LINES
MU AND DEC BCD 5 LINES
EOC
RESET INHIBIT
MTA
EOC
STEP
14
RESET INHIBIT
6054B MAIN CHASSIS ASSY
MOTHER PCB 05344001
EOC
SQUELCH
ATCO
IEEE 448 SAMPLE RATE CONTROL
ASSY 05788601
EOC
RESET
RESET COM.
SAMPLE
TEST
LOW
NORMAL
WIDE
FUNCTION COM.
1 HZ
10 HZ
100 HZ
1 KHZ
10 KHZ
100 KH
1 MHZ
RESOLUTION COM.
REMOTE LAMP
LAMP TEST
OFFSET SELECTION BCD 32 LINES
POSTIVE OFFSET
NEGATIVE OFFSET

FIG

OPTION 05 DATA INTERFAC


A7
MTA
EOC
STEP
14
IEEE 448 OFFSET PCB ASSY
05725901
DACO
DACI
DAVI
ATN
DAVO
RFDI
RFDO
TON
TALK
PUT PCB ASSY
DI5
DI5
DAVI
MTA
REMOTE
REMOTE
MLA
MLA
MLA
MLA
STROBE
INHIBIT RESET
A5
STROBE
MLA
MLA
IEEE 448 PRORAMMING PCB
ASSY 05725601
DI 1
DI 2
DI 3
DI 4
DI 1
DI 2
DI 3
DI 4
REMOTE
COMP
UNT
UNL
MTA
RESET INHIBIT

URE 4-17

FUNCTIONAL BLOCK DIAGRAM

# CHAPTER 5

# MAINTENANCE

## 5.1 INTRODUCTION

This chapter contains maintenance procedures for corrective maintenance, performance test and calibration. Corrective maintenance is troubleshooting the instrument to isolate the defective component, assembly, etc. Performance test is used to ascertain the operational status of the instrument and calibration to adjust the respective circuits so as to return them to required specifications.

## 5.2 TEST EQUIPMENT REQUIRED

Table 5-1 lists the recommended test equipment required for the testing and alignment procedures outlined in the corrective maintenance, performance test and calibration procedures.

TABLE 5-1 RECOMMENDED TEST EQUIPMENT

| INSTRUMENT TYPE | CRITICAL SPECIFICATION | RECOMMENDED MODEL | USE* |
|---|---|---|---|
| 1. Auto-transformer | 100V ac – 130V ac | Superior UC1M | T |
| 2. Attenuator | | Tektronic 011-0059-01 | PAT |
| 3. Digital Voltmeter | ±0.1% ac, dc | S-D 7004 | AT |
| 4. Frequency Standard | | Gen'l Tech 304B/Tracor | A |
| 5. Frequency Synthesizer | 2.0 GHz - 4.0 GHz | S-D 1600 Series | PT |
| 6. Frequency Counter | 120 MHz | S-D 6241A | AT |
| 7. Oscilloscope | 100 MHz Bandwidth<br>0.1 μsec Sweep | Tektronic 7704 | AT |
| 8. Power Amplifier | +20 dBm Output @500 MHz | ENI 503L | PA |
| 9. Power Meter | +20 dBm with attenuator | S-D 4020 w/Opt M1 | PAT |
| 10. Signal Generator | 20 Hz - 10 MHz | HP 651B | PAT |
| 11. Signal Generator | 100 Hz - 1 GHz | S-D 1702 | PAT |
| 12. Signal Generator | 0.8 GHz - 2.4 GHz | HP 8614A | PAT |
| 13. Signal Generator | 1.8 GHz - 4.5 GHz | HP 8616A | PAT |
| 14. Signal Generator | 3.8 GHz - 7.6 GHz | HP 618B | PAT |
| 15. Signal Generator | 7.0 GHz - 11.0 GHz | HP 620B | PAT |
| 16. Signal Generator | 10.0 GHz - 15.5 GHz | HP 626A | PAT |
| 17. Signal Generator | 15.0 GHz - 21.0 GHz | HP 628A | PAT |
| 18. Signal Generator | 18.0 GHz - 26.5 GHz | HP 938A | PAT |
| 19. Sweep Generator | 20 MHz - 525 MHz Sweep | Wavetek 2001 | PAT |
| 20. Test Fixture | BCD and Remote Interface | S-D | P |
| 21. Programmable Calculator | IEEE 488 Interface | HP 9825 | PT |

*P = Performance Test A = Calibration Adjustment T = Troubleshooting

## 5.3 PERFORMANCE TEST PROCEDURES

The performance test procedures provide verification of specifications and proper operation of all circuits within the 6054B frequency counter. This procedure may also be utilized for incoming inspection and troubleshooting.

### 5.3.1 Instrument Self Test

The following procedure performs an operational self test of the timebase, resolution, count chain and display circuits using the internal reference oscillator as a signal source. No special test equipment is required to perform this test.

Procedure: Counts 1 MHz for the gate times selected by the resolution switch.

Specifications: Resolution, switch selectable in decade steps 1 MHz to 1 Hz.

Set counter controls as follows:

Set POWER switch to ON.
Press TEST INSTR switch.
Adjust RECYCLE RATE to MAX (full CW)
Set INT/EXT Time Base switch to INT.

Step the RESOLUTION switch 1 MHz thru 1 Hz and observe the visual display as shown on Table 5-2.

TABLE 5-2 SELF TEST VISUAL DISPLAY

| RESOLUTION | DISPLAY * | ANNUNCIATOR |
|---|---|---|
| 1 MHz | 1. | MHz |
| 0.1 MHz | 1.0 | MHz |
| 10 kHz | 1.00 | MHz |
| 1 kHz | 1000. | kHz |
| 0.1 kHz | 1000.0 | kHz |
| 10 Hz | 1000.00 | kHz |
| 1 Hz | 1000.000 | kHz |
| *All readings are ±1 count on the LSD | | |

Procedure: Low range function test for gate times selected by the resolution switch.

Set counter controls as follows:

Set POWER switch ON.
Press LOW switch.
Adjust RECYCLE RATE to MAX.
Set INT/EXT time base switch to INT.

Step the RESOLUTION switch 1 MHz thru 1 Hz and observe the visual display as shown on Table 5-3.

TABLE 5-3 LOW RANGE TEST DISPLAY

| RESOLUTION | DISPLAY | ANNUNCIATOR |
|---|---|---|
| 1 MHz | 0. | MHz |
| 0.1 MHz | .0 | MHz |
| 10 kHz | .00 | MHz |
| 1 kHz | 0. | kHz |
| 0.1 kHz | .0 | kHz |
| 10 Hz | .00 | kHz |
| 1 Hz | .000 | kHz |

Procedure: RF Bandwidth WIDE range function test for gate times selected by the resolution switch.

Set counter controls as follows:

Set POWER switch ON.
Press WIDE switch.
Adjust RECYCLE RATE to MAX.
Set INT/EXT time base switch to INT.

Step the RESOLUTION switch 1 MHz thru 1 Hz and observe the visual display as shown on table 5-4.

TABLE 5-4 WIDE RANGE TEST DISPLAY

| RESOLUTION | DISPLAY | ANNUNCIATOR |
|---|---|---|
| 1 MHz | .000 | GHz |
| 0.1 MHz | .0000 | GHz |
| 10 kHz | .00000 | GHz |
| 1 kHz | .000000 | GHz |
| 0.1 kHz | .0000000 | GHz |
| 10 Hz | .00000000 | GHz |
| 1 Hz | .000000000 | GHz |

This completes instrument self test and function tests. If the counter fails any of the above steps repair and/or alignment may be required.

### 5.3.2 Indicator Test

The following procedure test all visual readout indications; all segments of the eleven digit readout display, Annunciator, Gate, Overload and Lock indicators. No special test equipment is required for this test.

Procedure: Lamp test.

Specifications: All segments light plus annunciators, overload and lock indicator.

Set counter controls as follows:

Set POWER switch to ON.
Press TEST LAMP and hold.

Observe front panel display. All eleven digits should read 8, the annunciator lamps GATE, GHz, MHz, and kHz, and the LOCK and OVERLOAD lamps are illuminated. If the counter fails any of the above steps repair may be required.

### 5.3.3 Recycle Rate

The following procedure verifies display time and automatic reset functions. No special test equipment is required for this test.

Procedure: Variable recycle rate, automatic reset, hold and manual reset.

Specifications: Recycle rate, continuously variable ≈0.5 ms to ≈5 seconds and hold.

Set counter controls as follows:

Set POWER switch to ON.
Set RESOLUTION switch to 1 kHz.
Adjust RECYCLE RATE control to MAX.
Press TEST INSTR switch
Set INT/EXT time base switch to INT.

Observe the GATE lamp and the display and rotate the rate control slowly CCW to HOLD detent; do not engage hold. The gate lamp will blink and the display should read 1000 kHz. Note that the Gate lamp off time increases as the rate control is rotated from the MAX position. Gate off time is continuously variable from approximately 5 milliseconds to 5 seconds.

Set RECYCLE RATE to HOLD.

Observe the display and GATE lamp and press RESET. The counter should reset and display 0000.000 kHz, the gate lamp should blink once and the display should read 1000.000 kHz and hold this reading indefinitely.

If the counter fails any of the above steps repair may be required.

### 5.3.4 Low Frequency Test

The following procedure verifies operational characteristics for low frequency, 20 Hz to 20 MHz, inputs. Signal Generators with 20 Hz to 10 MHz and 10 MHz to 480 MHz frequency ranges as listed on Table 5-1 are required to perform these tests.

Procedure: Measure low frequency inputs 20 Hz to 20 MHz at 10 mVrms levels.

Specifications:

| | |
|---|---|
| Range: | 20 Hz to 20 MHz |
| Sensitivity: | 10 mVrms. |
| Impedance: | 1 MΩ/20 pF. |
| Coupling: | ac |
| Input Connector: | BNC |
| Maximum Input Without Damage: | 20 Hz to 100 Hz; 200 Vrms<br>100 Hz to 100 kHz; 20 Vrms<br>100 kHz to 20 MHz; 2 Vrms |

Set counter controls as follows:

Set POWER Switch to ON.
Press LOW range switch.
Set RESOLUTION switch as desired.
Adjust RECYCLE RATE to MAX.
Set INT/EXT time base switch to INT.

Connect 20 Hz to 10 MHz Signal Generator to the 20 Hz - 200 MHz low frequency range input with 50Ω termination at counter end. Adjust signal generator for a 10 mVrms output level. Observe the display and vary the signal generator frequency output 20 Hz thru 10 MHz, maintain 10 mVrms output level. The counter should display all frequencies.

If the counter fails any of the above steps repair may be required.

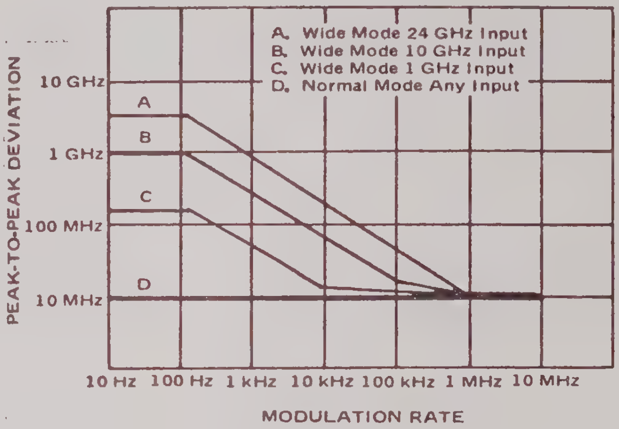
### 5.3.5 RF Input Normal and Wide Test

The following procedure verifies operational characteristics for high frequency 20 MHz to 24 GHz, inputs in both Normal and Wide modes. Appropriate signal generators as listed on Table 5-1 for frequency ranges 20 MHz to 24 GHz are required for this test.

Procedure: Measure high frequency inputs, 20 MHz to 10 GHz at -30 dBm, 10 GHz to 18 GHz at -25 dBm and 18 GHz to 24 GHz at -20 dBm.

Specifications:

| | |
|---|---|
| Range: | 20 MHz to 24 GHz |
| Sensitivity: | -30 dBm to 10 GHz<br>-25 dBm to 18 GHz<br>-20 dBm to 24 GHz |
| Impedance: | 50Ω nominal |
| Coupling: | ac |
| Input Connector: | SMA |
| Maximum Input without Damage: | +20 dBm prior to acquisition. +30 dBm after acquisition. |
| Acquisition Time, Wide Mode: | |
| First Reading: | 400 μs + 56 ms + 1/R x N sec. |
| Subsequent Reading: | 400 μs + 1/R x N sec. |
| Acquisition Time, Normal Mode: | |
| First Reading: | 157 ms + N x 1 ms + 1/R sec. |
| Subsequent Reading: | 1/R sec. |
| Amplitude Discrimination of two Frequencies: | 20 dB (10 dB typical) |
| AM Modulation: | Any modulation index providing the minimum voltage of the signal is not less than specified sensitivity. |
| FM Modulation: | |



Kickback Noise: -65 dBm typical.

Set counter controls as follows:

Set POWER switch to ON.
Press NORMAL switch.
Set RESOLUTION switch as desired.
Adjust RECYCLE RATE to MAX.
Set INT/EXT time base switch to INT.

Connect appropriate signal generator(s), to input 20 MHz to 10 GHz at -30 dBm, to the 20 MHz - 24 GHz input connector. Observe the display and lock indicator and tune the signal generator through the 20 MHz to 10 GHz range while maintaining a -30 dBm output level. Allow ample time between each frequency change for the counter to make the measurement. Counter LOCK indicator should illuminate and display readout all frequencies with leading zero's suppression.

Tune all frequencies between 10 GHz and 18 GHz at -25 dBm. The counter should display all frequencies and indicate LOCK.

Tune all frequencies between 18 GHz and 24 GHz at -20 dBm. The counter should display all frequencies and indicate LOCK.

Decrease the input level, observe the display and LOCK indicator. When the input level goes below the inputs sensitivity level the LOCK indicator will go out and the visual display is blanked.

Press WIDE range switch.

Repeat the NORMAL range procedures in the Wide range mode. The Counter should display the correct frequencies and indicate LOCK across the band.

If the Counter fails any of the above steps, repair may be required.

### 5.3.6 Overload

The following procedure verifies overload operational characteristics for 20 MHz to 24 GHz band inputs. Overload is identified by alternately flashing LOCK, OVERLOAD lamps and the least significant digit of the display with input levels at approximately +20 dBm. Appropriate signal generators, power amplifier, attenuator and power meters as listed in Table 5-1 are required for this test.

Procedure: Simulated overload condition by applying +20 dBm at 550 MHz to 20 MHz - 24 GHz input.

Specifications:
Maximum input without damage: +20 dBm.

Set Counter controls as follows:
Set POWER switch to ON.
Press NORMAL switch.
Set RESOLUTION switch as desired.
Adjust RECYCLE RATE to MAX.
Set INT/EXT time base switch to INT.

Connect test equipment as shown in Figure 5-1 and adjust signal generator for +0 dBm reading on the power meter at 550 MHz. Disconnect power amplifier from the attenuator and connect it to the Counters 20 MHz - 24 GHz input. Observe that the Counters OVERLOAD, LOCK and least significant digit blink.

If the Counter fails to indicate an overload warning repair or adjustment may be required.

### 5.3.7 Time Base Stability

The following procedure will test short term time base reference oscillator stability. A frequency standard and an oscilloscope as listed in Table 5-1 are required to perform this test.

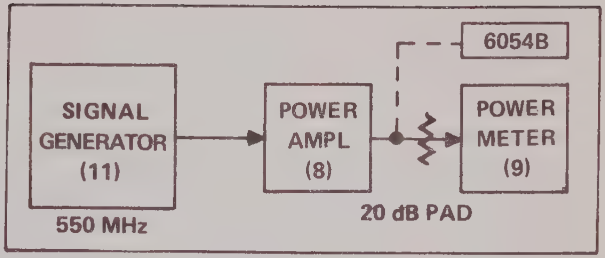


FIGURE 5-1 OVERLOAD ADJUSTMENT TEST SETUP

Procedure: Measure the reference oscillator 1 MHz out on an oscilloscope synched to a frequency standard.

Specifications:

| | |
|---|---|
| Crystal Frequency: | 10 MHz. |
| Aging Rate After Warm-up: | ±1 part $10^6$ /year. |
| Frequency Retrace for Off Periods up to 24 hours. | ±5 parts $10^7$ within 10 seconds. |
| Short Term Aging Rate: | ±5 parts in $10^8$ /day average for 3 days. |
| Temperature Variation: | TCXO with variation of 1 part in $10^6$ over temperature range +0°C to +50°C. |
| 10% Line Voltage Variation: | ±5 parts in $10^8$. |
| Long Term Aging Rate: | ±3 parts in $10^7$ for 30 days. |
| Output Frequency: | 1 MHz $\geq$2.4V Squarewave. |

Set Counter controls as follows:
Set POWER switch to ON.
Set INT/EXT time base switch to INT.

Connect frequency standard to oscilloscope External Trigger, connect Counters 1 MHz to oscilloscope and observe the oscilloscope sweep. Adjust scope controls for a stable sweep and observe the rate of change. The 1 MHz rate of change should not exceed 1 cycle per second.

If the Counter fails this test repair and/or alignment may be required.

### 5.3.8 Data Interface Test

To verify the operation of the data interface, ensure that the Counter operates properly when used as a stand-alone instrument. After proper operation is established, the following procedure is used to test the GPIB interface circuits. A controller, such as the programmable calculator (21) and the signal generators listed in Table 5-1 are required to perform the test.

Procedure: Check talk and listen modes.

Set Counter controls as follows:

Set POWER to off (down position)
Set EXT/INT time base to INT.
Set PROG-TALK ONLY to PROG.
Set ADDRESS switches to the address assigned to the Counter.

Connect appropriate signal generators to 20 Hz - 20 MHz and 20 MHz - 24 GHz inputs; and connect programmable calculator to the IEEE 488 INTERFACE connector.

Set POWER to on (up position). Counter should be in monitor mode with the following wake-up conditions present:

Resolution at 1 Hz
Mode selection set to NORMAL
HOLD control function selected

Verify the operation performing the procedures outlined in 3.7.3 for all functions listed in Table 3-6.

If the Counter fails any of the above steps repair may be required.

## 5.4 CALIBRATION AND ALIGNMENT PROCEDURES

The following alignment procedures provide instructions for adjusting the Counter to within operating tolerances. Figure 5-2 identifies the location of the major assemblies used in these procedures.

### 5.4.1 Power Supply Operation Check

Prior to making any alignment steps ascertain normal power supply operation.

Procedure: Power Supply voltage checks. Monitor the respective voltages as outlined in Table 5-5.

Should any of the voltages check out of tolerance perform the power supply check out procedure and troubleshoot the appropriate supply.

Procedure: Power Supply resistance checks.

*WARNING*

*Before performing the resistance checks, ensure that the instrument is disconnected from the power source.*

**TABLE 5-5 POWER SUPPLY OUTPUT VOLTAGES**

| Power Supply | dc Voltage Within | Measure From |
|---|---|---|
| Counter P.S. +5V | +4.8 to +5.2 | Mother Board Interconnect Assy. See Test Assy. dwg. 057164 +5V to ground. |
| Counter P.S. -5.2V | -5.0 to -5.4 | Mother Board Interconnect Assy. See Test Assy. dwg. 057164 -5.2V to ground. |
| Counter P.S. +15V | +14.4 to +15.6 | Mother Board Interconnect Assy. See Test Assy. Dwg. 057164 +15V to ground. |
| Counter P.S. -15V | -14.4 to -15.6 | Mother Board Interconnect Assy. See Test Assy. dwg. 057164 -15V to ground. |
| Indicator Power +9V | +8.5 to +11.5 | Main Chassis Assy. emitter Q1. See Test Assy Dwg. 057164 +9V to ground. |
| ACTO P.S. +5V | +4.8 to +5.2 | Main Chassis Assy. emitter U6. See Test Assy. dwg. 057164. |
| ACTO P.S. -5.2V | -5.0 to -5.4 | Main Chassis Assy. emitter U7. See Test Assy. dwg. 057164. |
| ACTO P.S. +15V | +14.4 to +15.6 | Main Chassis Assy. emitter U8. See Test Assy. dwg. 057164. |
| ACTO P.S. -15V | -14.4 to -15.6 | Main Chassis Assy. emitter U9. See Test Assy. dwg. 057164. |

Remove power cord.
Set POWER switch to on, (up position).
Set main power line switch (rear panel) to 115 position.

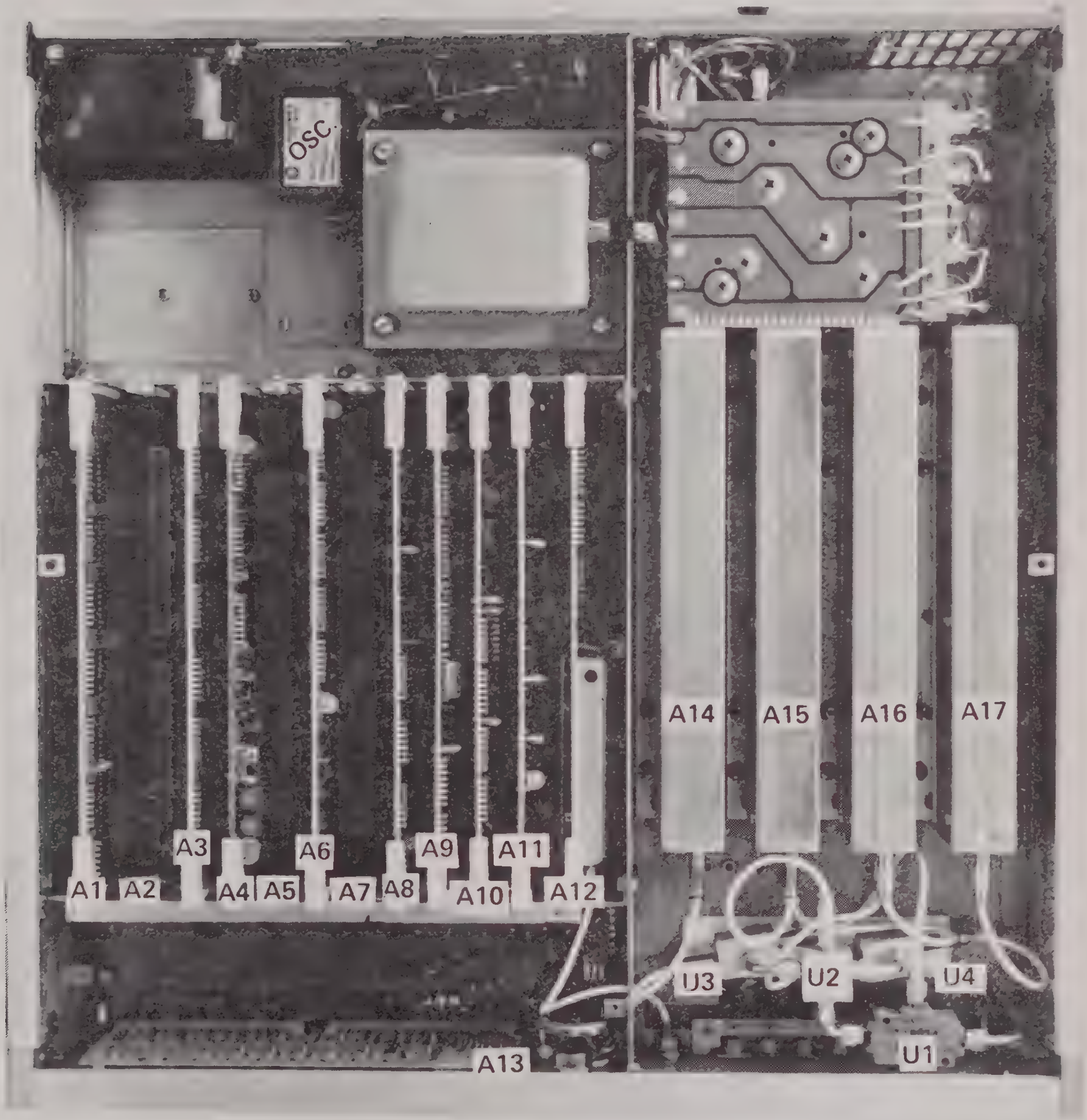

OSC.
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
A12
A13
A14
A15
A16
A17
U3
U2
U4
U1

FIGURE 5-2 COMPONENT LOCATIONS

With DVM (3) measure the resistance between points as listed in Table 5-6. Refer to power supply schematic and associated assembly drawings for details.

*NOTE*

*All resistive measurements are with respect to chassis ground unless otherwise stated.*

**TABLE 5-6 POWER SUPPLY RESISTANCE**

| Measure | Resistance | Measure From |
|---|---|---|
| Line to line on power connector | 7 ohm nominal | power connector |
| Power connector line input and instrument chassis. | infinite | power connector |
| Diode PC Assy pin 4 | >20 ohms | Diode PC Assy, Dwg. 05789001 |
| Diode PC Assy pin 8 | 35 ohms | Diode PC Assy, Dwg. 05389001 |
| Diode PC Assy pin 7 | >100 ohms | Diode PC Assy, Dwg. 05389001 |
| Diode PC Assy pin 2 | 400 ohms | Diode PC Assy, Dwg. 05389001 |
| Counter P.S. Reg. +5V | 200 ohms | Mother Board Interconnect Assy. See Test Assy. Dwg. 057164 |
| Counter P.S. Reg. -5.2V | 130 ohms | Mother Board Interconnect Assy. See Test Assy. Dwg. 057164 |
| Counter P.S. Reg. +15V | 1000 ohms | Mother Board Interconnect Assy. See Test Assy. Dwg. 057164 |
| Counter P.S. Reg. -15V | 600 ohms | Mother Board Interconnect Assy. See Test Assy. Dwg. 057164 |
| ACTO Power +5V | 400 ohms | Main Chassis Assy. emitter U6. See Test Assy. Dwg. 057164 |
| ACTO Power -5.2V | 75 ohms | Main Chassis Assy. emitter U7. See Test Assy. Dwg. 057164 |
| ACTO Power +15 | 100 ohms | Main Chassis Assy. emitter U8. See Test Assy. Dwg. 057164 |
| ACTO Power -15V | 500 ohms | Main Chassis Assy. emitter U9. See Test Assy. Dwg. 057164 |

Procedure: Power Supply voltage checks.

Connect Counter through auto-transformer (1) to 115 Vac power source.

Adjust auto-transformer to obtain minimum voltage out (full counterclockwise).

Connect DVM (3) to +5V connector power supply. Set DVM for voltage measurement.

Set POWER switch to POWER.

Adjust auto-transformer to obtain 115, ±1, volts ac. Monitor +5V output on DVM; +5V should not exceed +5.2V.

Measure dc supplies output as listed in Table 5-5.

Adjust auto-transformer to obtain 103.5 ±1 Vac.

Connect oscilloscope to Counter power supply +5V.

Set vertical input to 50 mV/div. scale.

Observe the scope display and press LAMP TEST. The 120 Hz ripple should be absent.

Set POWER to off, down position, and remove Test equipment.

### 5.4.2 A4, 500 MHz Decade and Gate

Procedure: Low pass filter alignment and Low to ACTO mode switching centered around 500 MHz.

Test Equipment required:

Oscilloscope (7)
525 MHz Sweep Generator (19)
Signal Generator (11)
Power Meter (9)

Set RESOLUTION to 1 kHz

Press WIDE band switch.

Using the Signal Generator input 500 MHz at -32 dBm and observe the visual display.

At inputs less than 550 MHz while turning up the Counter should shift to ACTO mode and display the input signal in GHz. While turning down from 550 MHz the Counter should shift to Low before reaching 500 MHz. The MHz annunciator is displayed in the Low count mode and the GHz annunicator when in the ACTO Mode. Should the counter fail to switch as appropriate alignment may be required.

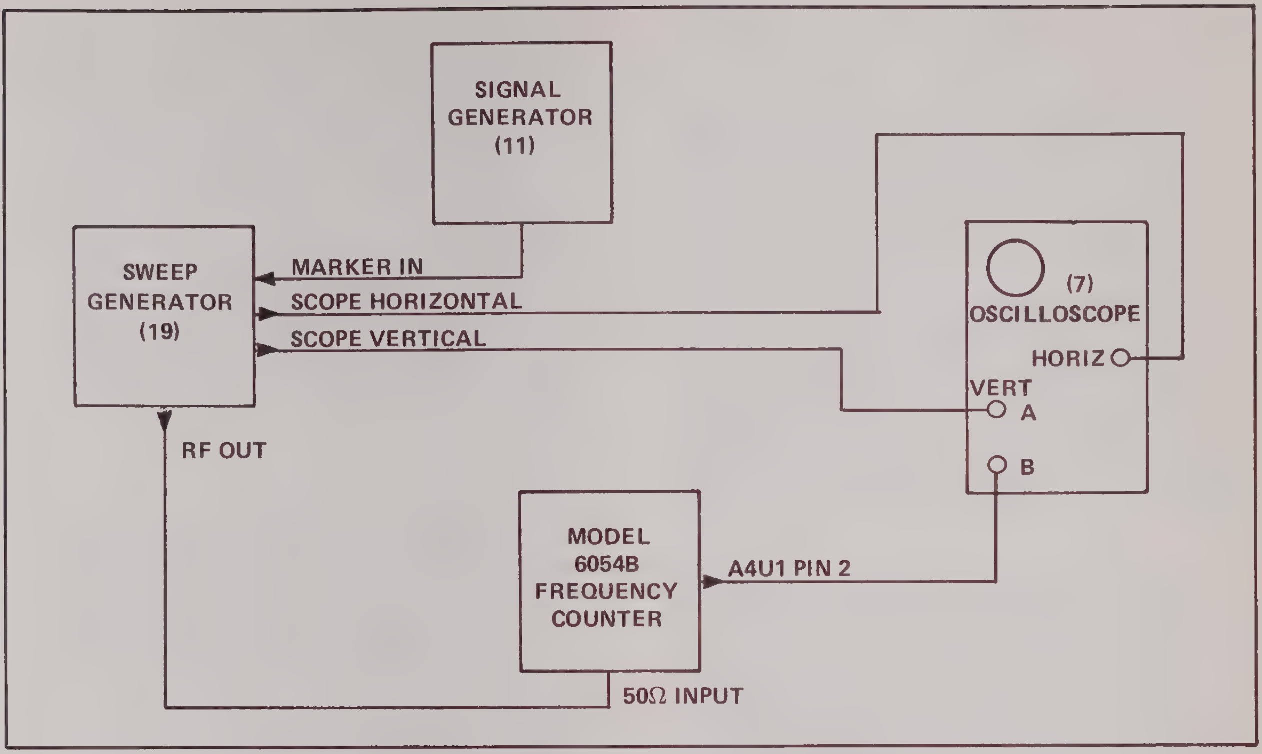

SIGNAL GENERATOR (11)
SWEEP GENERATOR (19)
MARKER IN
SCOPE HORIZONTAL
SCOPE VERTICAL
(7)
OSCILLOSCOPE
HORIZ
VERT
A
B
RF OUT
MODEL 6054B FREQUENCY COUNTER
A4U1 PIN 2
50Ω INPUT

FIGURE 5-3 A4, 500 MHz DECADE AND GATE ALIGNMENT TEST SETUP

Alignment: Connect test equipment as shown in Figure 5-3, set RESOLUTION to 1 kHz and press WIDE band switch.

1. Adjust Sweep Generator for 20 MHz to 525 MHz sweep at -30 dBm output. Use the marker at 500 MHz for reference.

2. Set the oscilloscope controls as follows:
   HORIZONTAL: EXT
   VERTICAL A: 200 mV/div
   VERTICAL B: 100 mV/div

3. Observe the wave form at A4U1 pin 2. See Figure 5-4.

4. If the proper low pass bandpass is not present the inductors L4 and L5 will have to be trimmed. These inductors consist of preformed 22 guage wire loops that can be reformed to increase or decrease their diameter, this should only be done as a last resort measure.

R23 should be fully counterclockwise for optimum output of the bandpass amplifier. Trim L4 and L5 as appropriate to obtain the low pass filter pass band as shown in Figure 5-4.

5. Disconnect test equipment.

6. Rotate LP ADJUST R42 fully counterclockwise. The counter should display .00X MHz.

7. Rotate R42 until display indicates .000000 GHz.

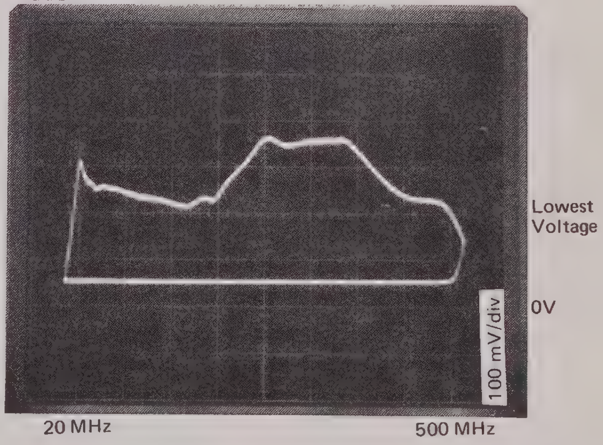


FIGURE 5-4 LOW PASS FILTER PASSBAND WAVEFORM

8. Connect signal generator (11) to counter 50Ω input. Adjust signal generator output level to -32 dBm, (use power meter as required to measure output level).

9. Vary the frequency of the signal generator between 500 MHz and 550 MHz.

10. Readjust R42, as necessary, so that while tuning signal generator upward in frequency, the counter switches to ACTO mode of operation before reaching 540 MHz. Also, while tuning down from 550 MHz, counter switches to low mode before reaching 500 MHz. The MHz, GHz annunciator lamps indicate when in the low count mode or ACTO mode respectively.

11. Increase signal generator output level to -15 dBm and repeat step 10.

12. Using appropriate signal generators with an output level of -32 dBm, tune through the frequency range 20 MHz to 530 MHz. The counter should display all frequencies.

### 5.4.3 A12, 20 MHz Amplifier Alignment

Procedure: Low frequency counting 20 Hz to 20 MHz at 10 mVrms.

Test equipment required:
Signal Generator (11) 100 Hz to 1 GHz.

Set RESOLUTION to 1 kHz and press LOW for low range frequency mode.

Using signal generator (11) input 20 MHz at 10 mVrms and observe the display. Vary the input frequency while maintaining 10 mV, the counter should display all frequencies. Should the counter fail to measure inputs at 10 mV alignment of A12 may be required.

Alignment: Connect signal generator (11), set to 20 MHz at 10 mVrms with 50Ω termination at the counter end of the input cable, to the 1 MΩ input.

1. Set RESOLUTION to 1 kHz and press LOW.

2. Adjust R13 for a stable readout of 20XXX kHz.

3. Decrease the input level and further adjust R13 for a stable readout until maximum sensitivity is realized. The measured input signal level should be typically 7 mVrms and not greater than 10 mV.

4. Tune the signal generator from 20 MHz down to 10 MHz while maintaining input level acquired in step 3, in any case not above 10 mV. The instrument should display all frequencies.

5. Change RESOLUTION to 1 Hz and connect 20 Hz to 10 MHz signal generator (10) to the input and repeat step 4 for 20 Hz to 10 MHz inputs. The instrument should display all frequency inputs at levels attained in step 3.

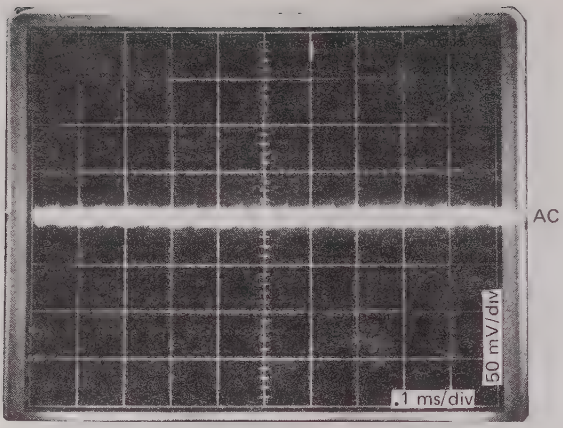
### 5.4.4 ACTO Modules Confidence Checks

Procedure: ACTO Alignment checks to be performed as an operational confidence check.

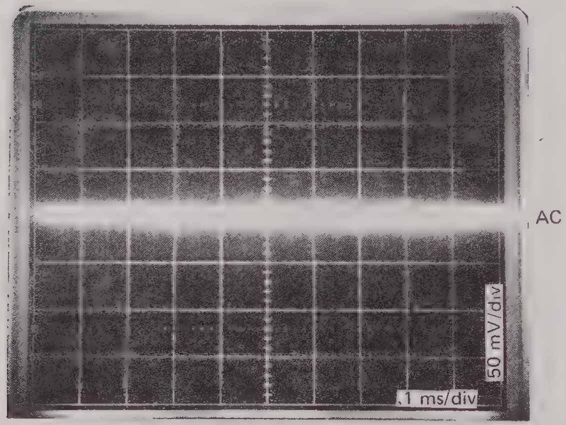
Test equipment required:
Sweep Generator (19)
Signal Generators (as appropriate)
Oscilloscope (7)
Frequency Counter (6)

1. Place instrument in WIDE mode and input 550 MHz at -30 dBm. Connect frequency counter to XA17-F or H and observe for a frequency readout of 30 MHz ±0.1 MHz.

2. Place instrument in NORMAL mode. Observe the signal at XA15-L for less than 10 mVpp 10 kHz signal. See figure 5-5.



ABNORMAL



NORMAL

FIGURE 5-5 XA15-L 10 kHz SIGNAL

3. Place instrument in NORMAL mode. Ground XA15-1, connect scope horizontal to XA15-9 and observe vertical at XA17-J.

Input any signal from 0.5 GHz to 24 GHz at specification sensitivity -2 dBm and observe the signal for lock sensitivity beats >200 mV. See Figure 5-6.

4. Place instrument in TEST mode. Ground XA15-1, connect scope horizontal to XA15-9 and observe vertical at XA17-J and XA14-E.

Compare N (XA14-E) and LOCK (XA17-J) while changing input frequency from 5 GHz to 24 GHz. Adjust input level to get lock beats = 200 mV for all inputs and N beats should be >100 mV. See Figure 5-7.

5. Place the instrument in NORMAL mode. Ground XA15-1, and observe the signal at XA17-J, for a baseline shift less than 175 mV, with inputs from 1-24 GHz at 0 dBm level. See Figure 5-8.

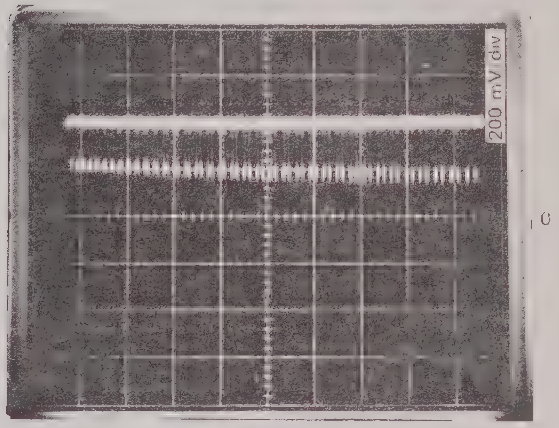
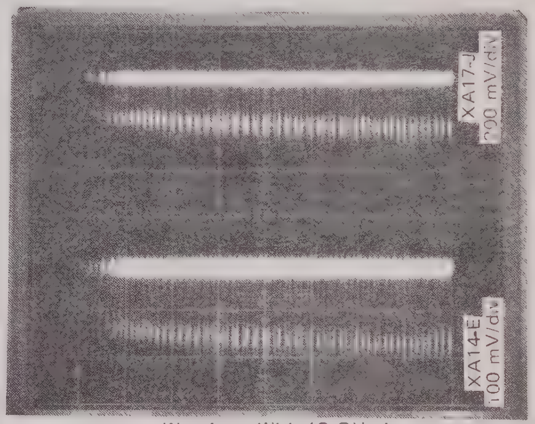


FIGURE 5-6 XA17-J LOCK SENSITIVITY BEATS



Waveform With 18 GHz Input

FIGURE 5-7 XA17-J LOCK IF AND XA14-E N IF BEATS

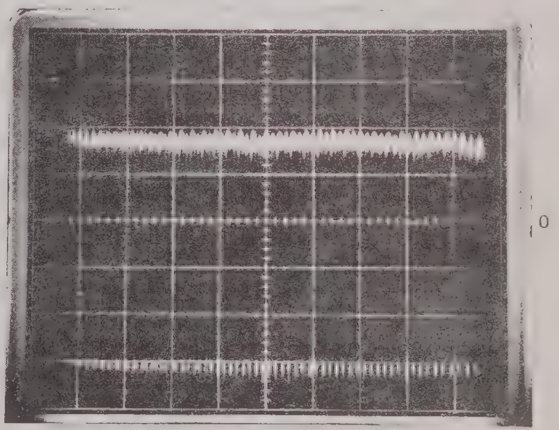


FIGURE 5-8 XA17-J BASE LINE SHIFT

6. Should the instrument fail to perform any of the above procedures alignment may be required.

### 5.4.5 ACTO Modules Alignment

Alignment of the ACTO modules require that all four modules, A14,A15,A16 and A17; mixers U3 and U4; power divider U2 and PIN leveler U1 be installed. The modules are aligned individually in sequence then peaked as a system. Complete alignment as outlined below is not required unless all ACTO modules are replaced/repaired. Prior to alignment of the respective boards ascertain the necessity for alignment by first monitoring the appropriate test point for the proper signals. If repair/ replacement has not been made alignment probably is not required.

On completion of individual ACTO Alignment final ACTO alignment, as outlined in 5.4.6 must be performed.

### 5.4.5.1 Search Oscillator A15 Initial Alignment

Procedure: Ramp Adjustments.

Test equipment required:
Oscilloscope (7)

1. Place A15 on ACTO Extender, RFI cover not required for alignment.

2. Place instrument in TEST and observe the signal at XA15-6. See Figure 5-9.

Adjust C11 to obtain 1 kHz output.

3. Connect scope to XA15-9.

Adjust R57 DC LEVEL SHIFT for 2V at the bottom of the waveform as shown in Figure 5-10.

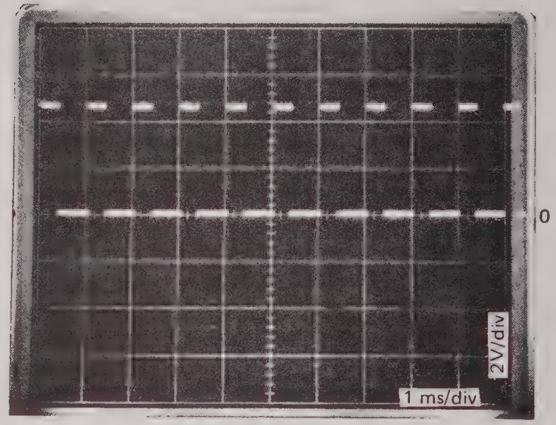


FIGURE 5-9 XA15-6 1 kHz SQUAREWAVE

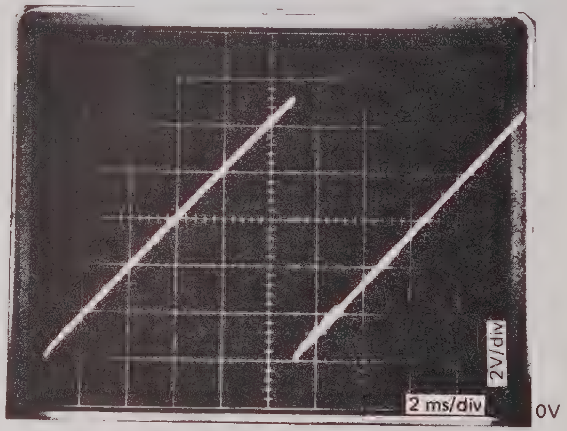
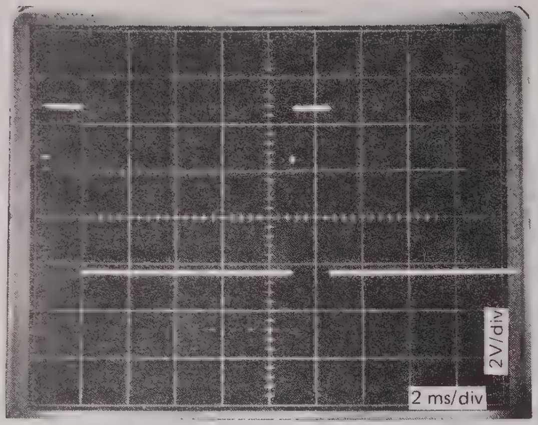


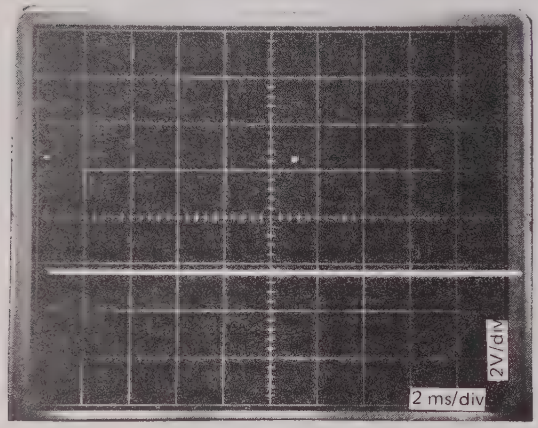
FIGURE 5-10 XA15-9 RAMP SWEEP RATE WAVEFORM

4. Connect scope to XA15-K and observe squelch counter reset pulse, Figure 5-11.

Adjust R44 SWEEP LIMIT CCW until pulse width increases, then CW 1/8 of a turn past where pulse narrows.


0
2V/div
2 ms/div

WIDE SIGNAL


0
2V/div
2 ms/div

NARROW SIGNAL

FIGURE 5-11 XA15-K SQUELCH COUNTER RESET

### 5.4.5.2 A17, Lock IF Initial Alignment

Procedure: Lock IF, Squelch and Discriminator Out adjustments.

Test equipment required:

Oscilloscope (7)  
Sweep Generator (19)  
Signal Generator (11)

1. Place A17 on ACTO Extender. RFI Test cover required. See Figure 5-12 for Adjustment component location.

2. Place instrument in Test mode and ground XA15-1. Connect Scope horizontal to XA15-9 and observe the vertical input at XA17-J, A, and L.

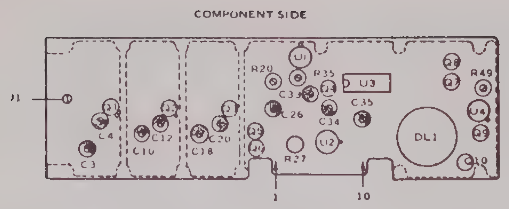

COMPONENT SIDE
J1
R20
R35
U3
C33
C26
C34
C35
R49
DL1
L4
C3
C10
C12
C18
C20
R27
1
10

FIGURE 5-12 A17 LOCK IF ASSEMBLY ADJUSTMENTS COMPONENT LOCATION

3. Apply an input signal 520 to 550 MHz at -40 dBm [Sweep Generator (19)] to the 50Ω input.

4. Apply frequency marker, use Signal Generator (11), to U3's N Mixer RF Output. See Test setup Figure 5-13. To input markers disconnect N Mixer cable at the 500 MHz Preamp.

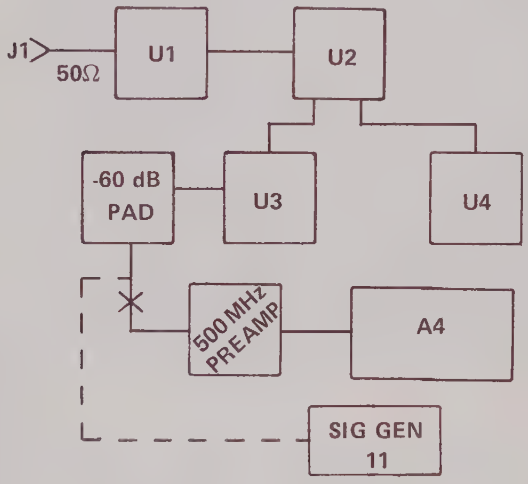

J1
50Ω
U1
U2
-60 dB PAD
U3
U4
500 MHz PREAMP
A4
SIG GEN 11

FIGURE 5-13 A17, TEST SETUP

Observe negative deflection on scope, see Figure 5-14a.

Adjust scope horizontal and generator level to obtain:

30 MHz marker at center of sweep  
36 MHz marker 3 divisions to the left  
24 MHz marker 3 divisions to the right.

Remove marker signal.

5. Retune A17C3, C10, C12, C18, C20, C26 C33, C34, C35 and R20, to obtain waveform as shown in Figure 5-14b at A17-J use R20 to trim for 200 mV dip at 30 MHz center division.

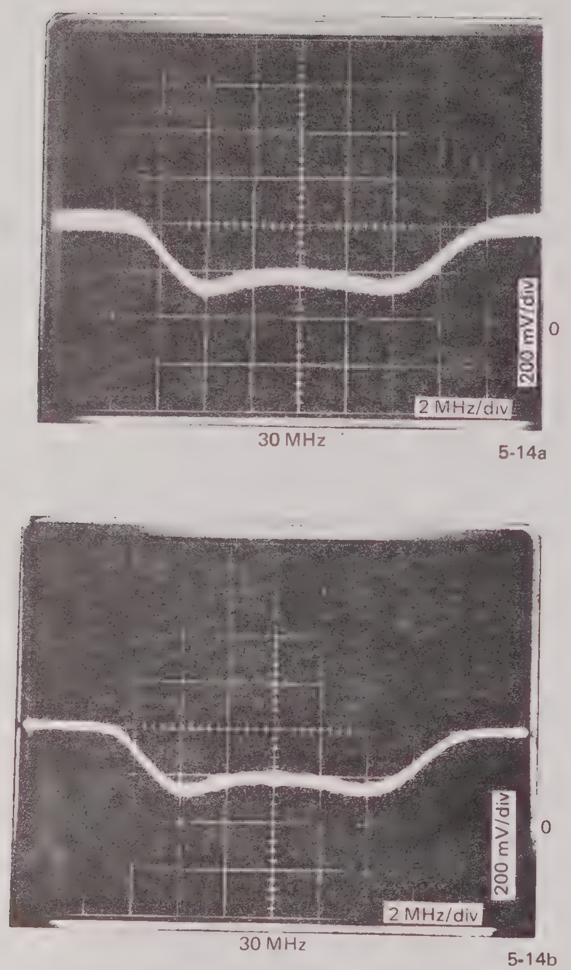


FIGURE 5-14 XA17-J SQUELCH TEST POINT WAVEFORM, LOCK IF BANDPASS

6. Adjust R27 to obtain waveform as shown in Figure 5-15 at A17-A. Tune R27 so that the waveform just drops out in the center.

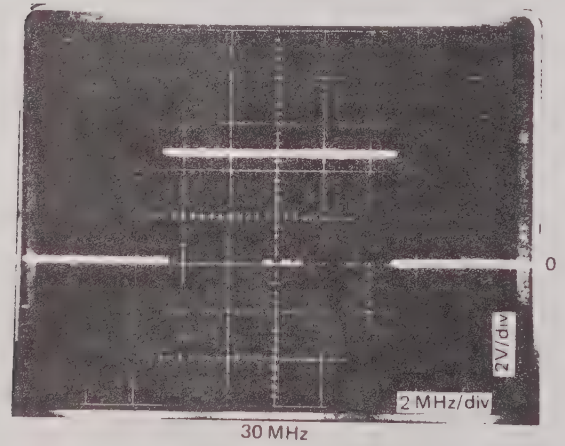


FIGURE 5-15 XA17-A SQUELCH ADJUST WAVEFORM

7. Adjust R35 and R49 to obtain waveform as shown in Figure 5-16 at A17-L. This signal may also be monitored at the DISC OUT connector on the rear panel.

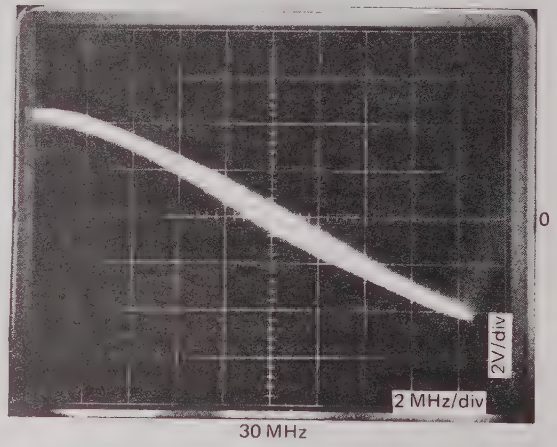


FIGURE 5-16 XA17-L DISCRIMINATOR OUTPUT WAVEFORM

8. As a final step recheck output at A17-J for 200 mV dip at the center division, see Figure 5-14.

### 5.4.5.3 A14 N IF Initial Alignment

Procedure: N IF and 1 kHz x N adjustments.

Test equipment required:
Oscilloscope (7)
Sweep Generator (19)

1. Place A14 on ACTO Extender, Preset trimmers caps to approximate settings as shown in Figure 5-17.

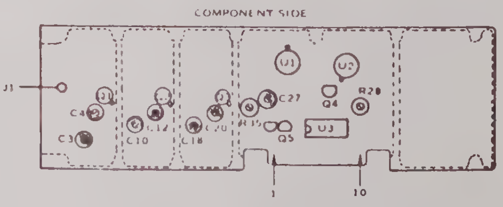


FIGURE 5-17 A14 N IF ASSEMBLY ADJUSTMENTS COMPONENT LOCATION

Adjust R28 and R35 to maximum clockwise. RFI cover required for alignment.

2. Place instrument in TEST mode, ground XA15-1 connect scope horizontal to XA15-9 and observe vertical on XA14-E and J.

3. Apply input signal 520-550 MHz at -40 dBm to the 50Ω input (Generator 19).

4. Adjust A14C3, C4, C10, C12, C18, C20, C27 and R28 to obtain optimum waveform as shown in Figure 5-18 at A14-E.

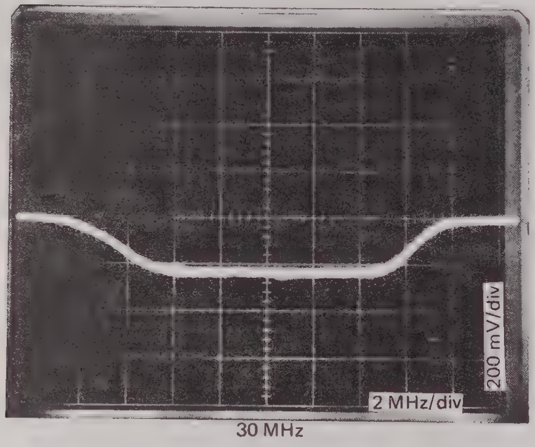


FIGURE 5-18 XA14-E N IF BANDPASS WAVEFORM

5. Remove ground at XA15-1, increase 550 MHz input to -15 dBm. Set scope to 0.5 ms Timebase.

6. Adjust A14R35 until signal at A14-J is 2 Vpp sinewave as shown in Figure 5-19 and is just affected by A14R35.

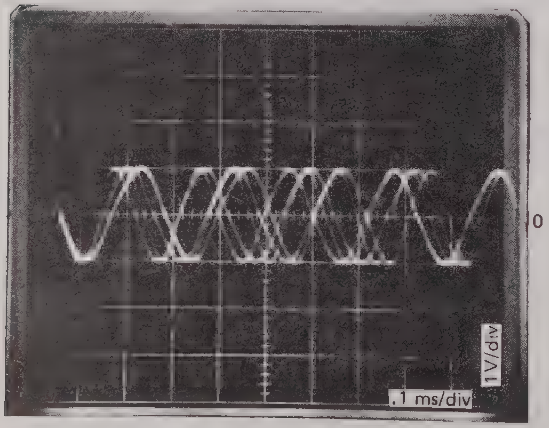


FIGURE 5-19 XA14-J 1 kHz x N TEST POINT WAVEFORM

7. Remove 550 MHz input signal and adjust A14R28 to obtain maximum signal at XA14-H. See Figure 5-20.

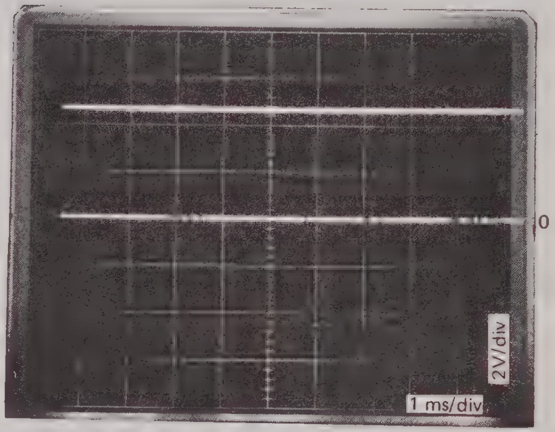


FIGURE 5-20 XA14-H 1 kHz x N OUTPUT WAVEFORM

### 5.4.5.4 A16 LO and Ø Shifter Initial Alignment

Procedure: LO drive to Lock and N Mixers adjustments.

Test equipment required:
Oscilloscope (7)
Sweep Generator (19)
Signal Generator (11)

1. Place A15 and A16 on ACTO Extenders. RFI cover required for alignment.

2. Place instrument in TEST mode, ground XA15-1, disconnect N Mixer RF output cable to A4, connect scope horizontal (dc) to XA15-9.

3. Apply 500 MHz at -20 dBm to 50Ω input, and observe vertical on XA17-J see Figure 5-21.

4. Increase input frequency to approximately 593 MHz and observe XA17-J for waveform as shown in Figure 5-22.

5. Increase RF input level to 0 dBm and adjust A15-R3 to obtain a voltage level of 4 mV at A15-J1. (PIN leveler U1 must be operational).

6. Apply inputs from 15-24 GHz at less than -20 dBm (LOW level) and 0 dBm or more (high level) and observe signal at XA17-J and XA14-E.

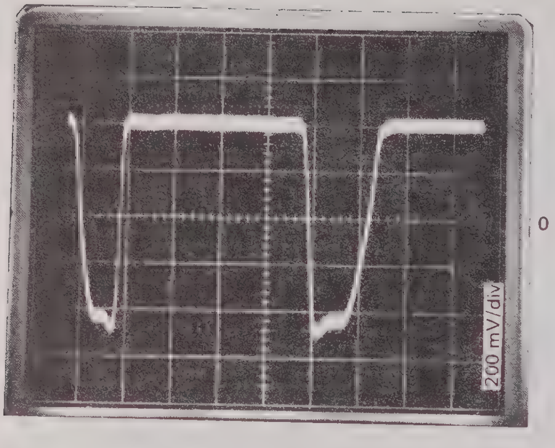


FIGURE 5-21 XA17-J WAVEFORM 500 MHz @ –20 dBm

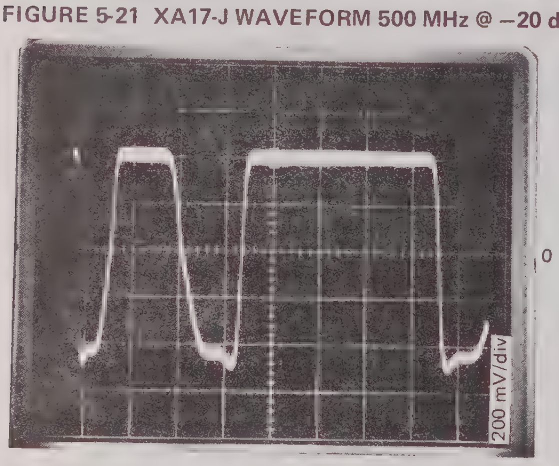


FIGURE 5-22 XA17-J WAVEFORM 593 MHz @ –20 dBm

Adjust A16-R58 for even beats at XA17-J for low input levels and an even baseline increase at high input levels.

Adjust A16-R59 for even beats at XA14-E at low input levels.

### 5.4.6 Final ACTO Alignment

ACTO alignment must be finalized to bring the individual assemblies together into the unit as a closed system.

#### 5.4.6.1 A15 Lock IF Final Adjust

1. Place instrument in WIDE mode. Remove ground at XA15-1 and apply 550 MHz at -30 dBm to J1 20 MHz -24 GHz input connector.

2. Monitor the frequency, use frequency counter (6) at XA17-F or H and adjust A15-R30 for an IF output of 30 ±.01 MHz.

#### 5.4.6.2 A15 Search Oscillator Final Ramp Adjust

1. Place instrument in NORMAL mode.

2. Observe the ramp output, use scope (7), at XA15-9 and adjust A15-R36 for a minimum (less than 10 mVpp) 10 kHz signal. See Fig. 5-23.

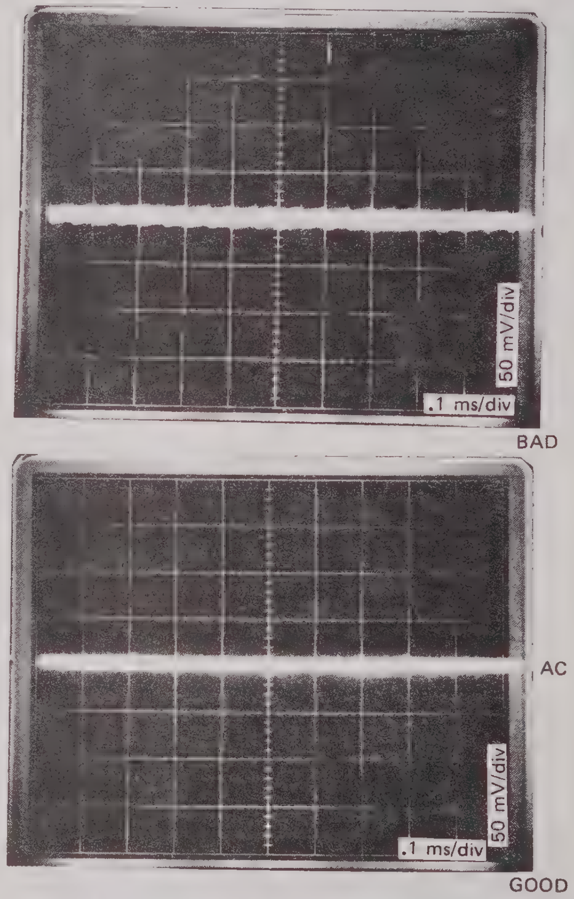


FIGURE 5-23 A15-9 VCO CONTROL RAMP WAVEFORM

#### 5.4.6.3 A17 Lock IF Sensitivity Final Adjust

1. Place instrument in NORMAL mode. Ground XA15-1 and observe the signal at XA17-J. Connect scope horizontal to XA15-9.

2. Readjust Lock Sensitivity A17-R20 as necessary to produce lock beats ⩾200 mV with inputs from 0.5 GHz to 24 GHz at specification input sensitivity -3 dBm.

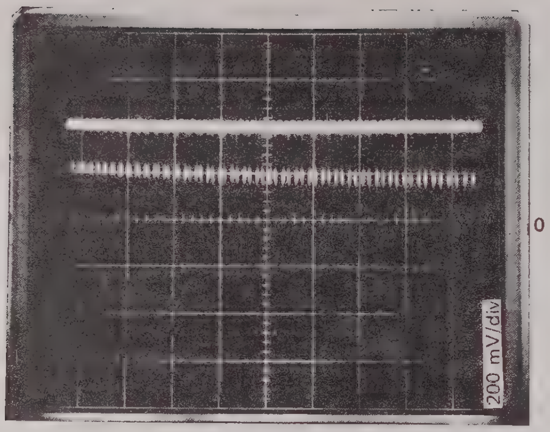
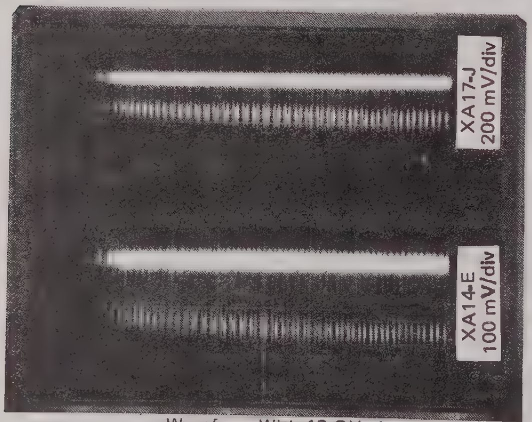


FIGURE 5-24 A17-R20 LOCK SENSITIVITY WAVEFORM

### 5.4.6.4 A17, A14 Lock IF And N IF Final Adjust

1. Place instrument in TEST mode. Ground XA15-1 and compare N IF and Lock IF beats at XA14-E and XA17-J. Connect scope horizontal to XA15-9.

2. Apply an input signal and vary the frequency from 0.5 MHz to 24 GHz and adjust the input level to maintain 200 mV lock beats at XA17-J. N beats at XA14-E must be ≥100 mV when compared with XA17-J through the frequency range 0.5 MHz to 24 GHz.



Waveform With 18 GHz Input

FIGURE 5-25 N IF AND LOCK IF BEATS COMPARISON

### 5.4.6.5 Leveler Final Adjust

1. Place the instrument in NORMAL mode. Ground XA15-1 and observe the signal at XA17-J. Connect scope horizontal to XA15-9.

2. Vary the input frequency from 15 to 24 GHz at high levels (≥0 dBm) and adjust A15-R3 for a base line shift of less than 175 mV at XA17-J.

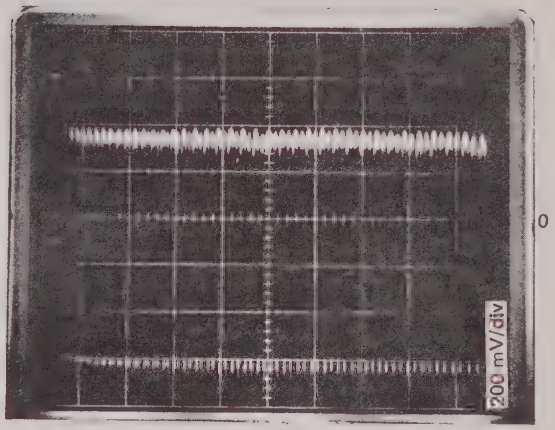


FIGURE 5-26 XA17-J AT 18 GHz LEVELER FINAL ADJUST

3. Input 550 MHz @ 0 dBm and monitor the dc voltage of ≥2 mV at A15-J1. Typical levels are 2 to 4 mV.

### 5.4.6.6 Overload Final Adjust

1. Connect the instrument and Test equipment as outlined in paragraph 5.3.6 Overload and Figure 5-1.

2. Adjust the Signal Generator output for 500 MHz at 0 dBm as read on the power meter.

3. Disconnect the power meter and connect the instrument to the Power Amp. output.

4. Adjust A15-R8 so the front panel OVERLOAD indicator turns on. Once an overload is initiated the least significant digit, the overload and lock indicators will flash on and off.

5. Reduce the Signal Generator output by 1 dBm. The flashing action should stop and only the LOCK indicator stay on.

## 5.5 MAINTENANCE AND REPAIR

### 5.5.1 Digital Plug-in PCB Assemblies (A1 through A13) Removal and Replacement.

When removing PCB Assemblies A1 through A13 for replacement, repair or testing, always remove ac power, and then the top cover of the Counter. To remove these PCB assemblies pull up on the extractor tabs to free the PCB assembly from it's mother board connector, then lift PCB assembly upward until it clears the PCB guides of the card cage assembly.

If a Digital Plug-in PCB Assembly is to be tested or troubleshooted within the Counter install the PCB assembly with the use of the Digital Extender Assembly #05502901.

When reinstalling a Digital Plug-in PCB assembly insert the PCB assembly into it's card cage guides, lower it into the card cage assembly until it makes contact with the mother board connector, then press firmly to insure it's proper seating into the connector.

### 5.5.2 ACTO Plug-in Module Assemblies (A14 Through A17) Removal and Replacement.

When removing module assemblies A14 through A17 for repair, replacement or testing, always remove ac power, and then the top cover of the Counter. Rotate the two retainer cam lock screws located on the ACTO module mounting rail 1/4 turn CCW to free the ACTO module from the ACTO chassis. Then lift the assembly and slip the coax cable(s) off the series 27 connector(s).

To obtain access to the internal circuitry of the ACTO module, remove the six 4-40 5/8" PHMS machine screws with their lock washers from the circuit side of the module casting (the module mounting rail will also detach when the lower three screws are removed).

Remove the component side of the module casting. The internal PCB will remain attached to the circuit side casting by four 4-40 3/8" PHMS screws (if access to the circuit side of the PCB is required removal of these four screws will allow the PCB to be lifted from the casting).

If an ACTO plug-in module is to be aligned, tested or troubleshooted within the Counter, reinstall the ACTO module with the use of the ACTO Extender Assembly #05502801. The ACTO Extender can be attached to the ACTO chassis by it's two cam lock screws.

When reinstalling an ACTO plug-in module assembly into the counter, first push the coax cable(s) on to the series 27 coax connector(s) insuring that they lock with a snapping action. Then insert the module into it's ACTO chassis connector and rotate the two cam lock screws 1/4 turn CW to secure it to the ACTO chassis.

### 5.5.3 PCB Component Removal and Replacement.

When replacing electronic components soldered to PCB's, the procedures indicated below should be followed to prevent damage to the board.

1. Determine by troubleshooting techniques, which integrated circuit or discrete component(s) has failed.

2. Remove the defective component(s) from the board by cutting the pins or leads with small diagonal pliers.

3. Apply heat (40-50W soldering iron) sparingly to each of the cut pins or leads and remove them from the board; clean the holes with a toothpick or solder suction tool.

4. Form the tinned leads of the replacement part and insert in the printed circuit holes; solder, then trim leads to extend 1/16-inch beyond the back surface of the board. (Use only 63-37 solder with maximum 1/16-inch diameter).

*CAUTION*

*Trim leads only after soldered installation is complete. This procedure greatly lessens the possibility of component failure due to shock-wave damage caused by the trimming tool.*

5. When soldering semiconductor devices and other small components, be sure to use a heat sink tool or long-nosed pliers connected to the component leads while each is being soldered. Allow the soldered connection to cool before removing the heat sink.

6. Clean all dirt and solder-flux from the printed circuit traces by liberal application of isopropyl alcohol or freon-type solvents.

## 5.6 INSTRUMENT TROUBLESHOOTING

If a malfunction is suspected, first perform the performance test procedures located in paragraph 5.3 and the calibration and alignment procedures located in paragraph 5.4, to insure that a malfunction does actually exist, and if so cannot be corrected by adjustment.

The calibration and alignment procedures are so structured that they provide fault isolation of most of the counters functional circuits.

A good understanding of the principles of operation of the counter is essential to efficient troubleshooting techniques. For this reason it is recommended that Chapter 4 be reviewed before attempting to troubleshooting the counter.

Before proceeding with the following troubleshooting procedures, check for obvious troubles such as an open fuse, defective power cord, input line power or out of tolerance line power. Next visually inspect the counter's mechanical integrity for such items as loose plug-in PCB assemblies or ACTO modules, loose or pulled out coax cables, etc. Then check the chassis, plug-in PCB and ACTO modules for mechanical and thermal damage, ie., broken, discolored or charred component parts.

If the source of the trouble cannot be detected by visual inspection or the malfunction corrected by performance of the calibration and alignment procedures, then proceed with the following troubleshooting procedures. Keep in mind that the trouble may be complex in nature, ie., two or more faults being present in the same functional area or in different functional areas causing interaction and thus providing faulty symptoms.

The Model 6054B Counter functions can be broken down into four functional groups;

Power Supply Circuits.
Display Circuits.
Control Group.
Conversion Group.

These four groups interact functionally to provide the different measurement operational modes;

Low Frequency Direct (20 Hz - 20 MHz).
Direct (20 MHz - 500 MHz).
Normal (Narrow) FLACTO (500 MHz - 18/24 GHz).
Wide ACTO (500 MHz - 18/24 GHz).

Furthermore the Counter is physically structured into sub-chassis, modules, and assemblies that relate to the functional groupings and operational mode functions.

By making measurements and noting symptoms, the malfunction(s) can be isolated to a certain functional group and/or operational mode. Then determination can be made as to the module or assembly that is at fault.

The most direct method to isolate any fault is to substitute the suspected module or assembly with a replacement that is known to be good and then perform the alignment procedures that may be required.

In the following troubleshooting procedures digital logic levels are called out as high (1) or low (0). The counter uses two different families of logic TTL and ECL which relate to the +5 $V_{cc}$ and -5.2 $V_{ee}$ ACTO and Counter power supplies. The voltage levels that are associated with these logic families are stated as follows:

| | |
|---|---|
| TTL High (1) | $\geqslant$ +2.4V |
| TTL Low (0) | $\leqslant$ +0.5V |
| ECL High (1) | $\geqslant$ -0.7V |
| ECL Low (0) | $\leqslant$ -1.5V |

### 5.6.1 Power Supply Troubleshooting

Almost any trouble symptom could be caused by an incorrect power supply output voltage, thus it is a good practice to routinely check all of the power supply output voltages before attempting to isolate the problem to a functional circuit. Table 5-7 provides a relatively fast and easy check for troubleshooting the power supply circuits. All of the voltage and resistance measurements are made between the indicated measurement point and the main chassis ground tie point, refer to Figure 5-27 which depicts the power supply output measurement

TABLE 5-7 POWER SUPPLY TROUBLESHOOTING CHART

| Power Supply Output Voltage and Function | Measurement Point | Voltage Check | Resistance Check | Bridge Rectifier | Regulator Transistor | IC Regulator |
|---|---|---|---|---|---|---|
| +9V Indicator Power | Emitter Q1 | +9V ±5% | >20 Ω | Diode Assy 05389001 | None | None |
| +5V Counter Vcc | Emitter U1 | +5V ±3% | 200 Ω | Diode Assy 05389001 | Q1 (MJ2500) | U1 (LM309K) |
| +5V ACTO Vcc | Emitter U6 | +5V ±3% | 400 Ω | Diode Assy 05389001 | Q1 (MJ2500) | U6 (MC7805CP) |
| -5.2V Counter Vee | Emitter U2 | -5.2V ±3% | 130 Ω | Diode Assy 05398001 | Q2 (MJ3000) | U2 (LM320K-5.2) |
| -5.2V ACTO Vee | Emitter U7 | -5.2V ±3% | 75 Ω | Diode Assy 05398001 | Q2 (MJ3000) | U7(MC7905-5.2CP) |
| +15V Counter Power | Emitter U5 | +15V ±3% | >1 kΩ | CR5 - 8 | None | U5 (MC7815CP) |
| +15V ACTO Power | Emitter U8 | +15V ±3% | 100 Ω | CR5 - 8 | Q3 (2N5190) | U8 (MC7815CP) |
| -15V Counter Power | Emitter U4 | -15V ±3% | 600 Ω | CR5 - 8 | None | U4 (MC7915CP) |
| -15V ACTO Power | Emitter U9 | -15V ±3% | 500 Ω | CR5 - 8 | Q4 (2N5139) | U9 (MC7915CP) |
| +28V Opt. Ref. Oscillator Power | Emitter U3 | +28V ±3% | | Counter P.S. Reg. Assy 05394101 | None | U3 (MC7815CP) |

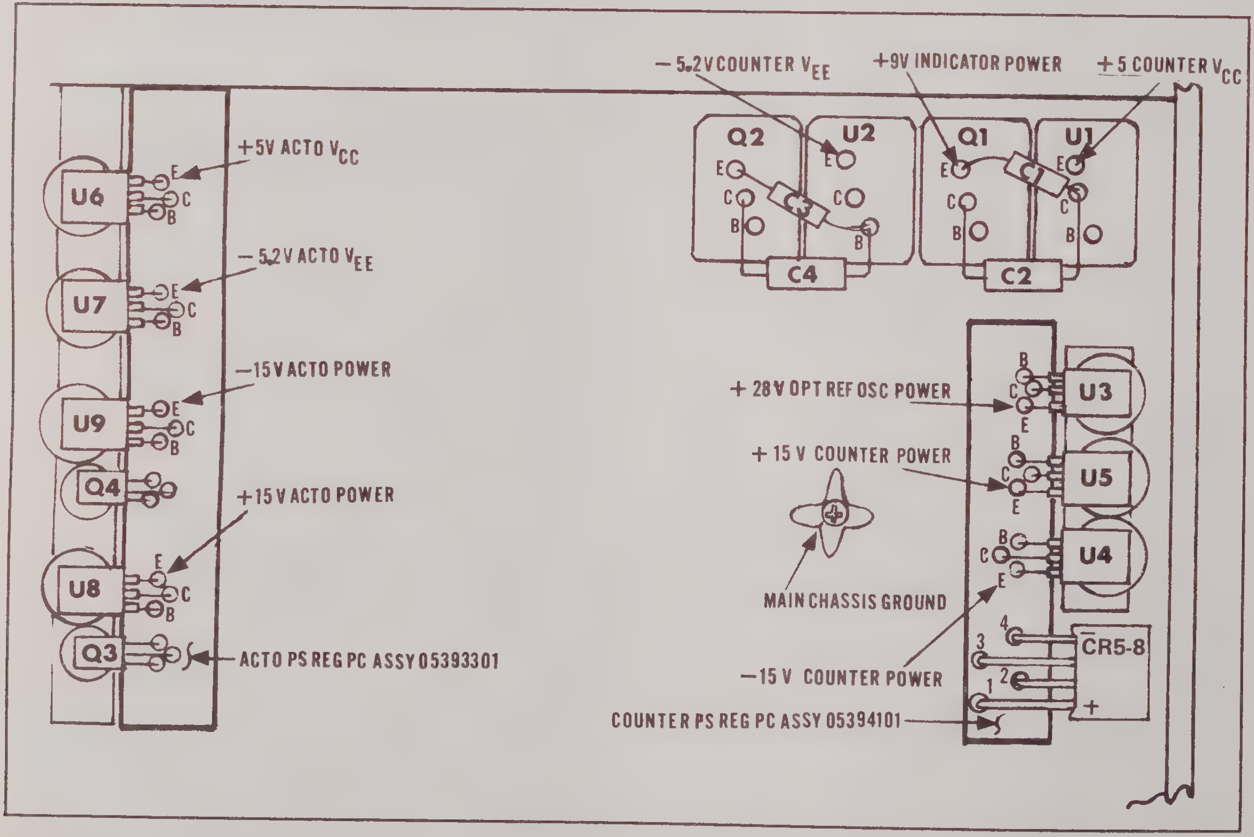

$-5.2$V COUNTER $V_{EE}$
+9V INDICATOR POWER
+5 COUNTER $V_{CC}$
+5V ACTO $V_{CC}$
$-5.2$V ACTO $V_{EE}$
$-15$V ACTO POWER
+15V ACTO POWER
ACTO PS REG PC ASSY 05393301
Q2
U2
Q1
U1
C3
C1
C4
C2
E
C
B
U6
U7
U9
Q4
U8
Q3
U3
U5
U4
CR5-8
1
2
3
4
+
+ 28V OPT REF OSC POWER
+ 15 V COUNTER POWER
MAIN CHASSIS GROUND
$-15$ V COUNTER POWER
COUNTER PS REG PC ASSY 05394101

FIGURE 5-27 POWER SUPPLY TROUBLESHOOTING MEASUREMENT POINT LOCATION

points located on the bottom of the main chassis. All of the voltages should be between the specified range. Should any voltage check out of tolerance, remove power from the Counter and perform the resistance check.

*NOTE*

> *The IC Voltage Regulators used in the power supply circuits (U1 through U9) employ internal thermal overload shutdown and short circuit current limiting functions. Thus a zero or low voltage measurement could be caused by loading effect external to the regulator.*

A lower than normal resistance measurement would indicate either a loading problem external to the effected supply output or a faulty voltage regulator within the effected supply. If the resistance check indicates a lower than normal Counter Power resistance reading(s) remove PCB Assemblies A1 through A13 one at a time to isolate any loading problem to an individual Counter PCB Assembly. If the resistance check indicates a lower than normal ACTO Power Supply resistance reading(s) remove ACTO Modules A14 through A17 one at a time to isolate any loading problem to an individual ACTO Module Assembly.

### 5.6.2 Display Circuitry Troubleshooting

The display circuits are located on Assemblies A1, A2, A3, A4 and A13. The circuitry consists of an 11-digit accumulator/storage chain, and a 40-bit shift register. Also included is signal gating logic which routes the information to the proper accumulator decade for the selected function, visual display and the BCD output data Option 04/05.

Most of the problems that may be encountered with the display circuitry can be isolated relatively fast by the performance of the lamp and instrument front panel pushbutton tests.

### 5.6.2.1 Troubleshooting the A13 Display PCB Assembly

The LAMP TEST will check out all of the visual readout indications of the Counter and allow isolation of the problem to any one of the eleven 7-segment decoder/drivers or digital display elements, or the six LED annunciators. The only function not checked by the LAMP TEST is the generation and display of the decimal point, which is provided by IC A13U12 a BCD-to-decimal decoder SN74145N. Refer to page 5-85 of this manual for information that will allow checking out A13U12 and the decimal point generation and display.

### 5.6.2.2 Troubleshooting the 11-Digit Accumulator /Storage Chain

The INSTR TEST will check out functions relating to the count chain (as well as the time base circuitry which is considered as part of the control group function). When the front panel TEST INSTR switch is pressed and latched the 1 MHz reference oscillator signal is applied to the 500 MHz decade A4U6 ($10^0$ accumulator) via the count gate logic A4U5, which allows the accumulators to count the 1 MHz for the gate times selected by the RESOLUTION switch.

To perform the INST TEST proceed as follows:

Set counter controls as follows:

POWER switch to ON.
Press and latch TEST INSTR switch.
Rotate RECYCLE RATE control fully CW to MAX.
Place rear panel INT/EXT time base switch to INT.

Step the RESOLUTION switch from 1 MHz through 1 Hz and observe the visual display. Table 5-8 provides the normal display readout.

**TABLE 5-8 INSTRUMENT TEST NORMAL DISPLAY INDICATIONS**

| Resolution Switch Setting | 11-Digit Display Readout | Annunciator Indication |
|---|---|---|
| 1 MHz | 1. | MHz |
| 0.1 MHz | 1.0 | MHz |
| 10 kHz | 1.00 | MHz |
| 1 kHz | 1000. | kHz |
| 0.1 kHz | 1000.0 | kHz |
| 10 Hz | 1000.00 | kHz |
| 1 Hz | 1000.000 | kHz |

## TABLE 5-9 RESOLUTION SWITCH INTERFACE

| Reso-lution Switch Setting | A5 ASSEMBLY PIN NUMBER | | | | | | | A8 ASSEMBLY PIN NUMBER | | | | | | A12 ASSEMBLY PIN NUMBER | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Ⓛ | Ⓚ | Ⓙ | Ⓗ | Ⓕ | Ⓔ | Ⓓ | ④ | ⑦ | ⑧ | ⑫ | ⑬ | ⑭ | 4 | C | B | 2 | A | 3 | 1 |
| 1 MHz | L | H | H | H | H | H | H | L | H | H | H | H | H | L | H | H | H | H | H | H |
| 0.1 MHz | H | L | H | H | H | H | H | H | L | H | H | H | H | H | L | H | H | H | H | H |
| 10 kHz | H | H | L | H | H | H | H | H | H | L | H | H | H | H | H | L | H | H | H | H |
| 1 kHz | H | H | H | L | H | H | H | H | H | H | L | H | H | H | H | H | L | H | H | H |
| 0.1 kHz | H | H | H | H | L | H | H | H | H | H | H | L | H | H | H | H | H | L | H | H |
| 10 Hz | H | H | H | H | H | L | H | H | H | H | H | H | L | H | H | H | H | H | L | H |
| 1 Hz | H | H | H | H | H | H | L | H | H | H | H | H | H | H | H | H | H | H | H | L |

H = Logic high (+5V) pulled up by 12k resistor(s) or internal IC pull up.

L = Logic low (OV) resolution switch common, returned to ground via jumper W1.

The 11-digit display readout should be as indicated in Table 5-8 ±1 count on the LSD. If not the problem is either the accumulator/storage chain or the time base circuits. If the annunciator indication or the decimal point location is abnormal the problem is related to the measurement unit (MU) or the decimal point (DP) logic located on the 20 MHz amplifier PCB Assembly A12.

The first step to isolate any problems is to check out the RESOLUTION switch and it's interface with the A5, A8 and A12 Assemblies. Table 5-9 provides the RESOLUTION switch interface data.

If the RESOLUTION switch and it's interface checked out, then check the time base period for each RESOLUTION switch setting. The time base period is measured with an oscilloscope at A8 pin Ⓐ with the Counter operating in the INST TEST function. Table 5-10 provides the time base period for each setting of the RESOLUTION switch.

## TABLE 5-10 TIME BASE PERIOD CHECK

| Resolution Switch Setting | Time Base Period At A8 Pin Ⓐ |
|---|---|
| 1 MHz | 1 μs |
| 0.1 MHz | 10 μs |
| 10 kHz | 100 μs |
| 1 kHz | 1 ms |
| 0.1 kHz | 10 ms |
| 10 Hz | 100 ms |
| 1 Hz | 1 s |

If the time base period check indicated a time base fault, troubleshoot the A8 Time Base PCB Assembly using Figure 7-11, A8 Time Base PC Assembly Schematic Diagram to isolate the problem to the IC component level.

If the time base period check indicated normal time base generation then verify the count gate logic and the $10^0$ accumulator circuitry on A4 PCB Assembly as follows:

1. With an oscilloscope monitor A4 pin V to insure that the time base signal (T.B.) is present as a proper input.

2. Monitor the GATE signal at A4 pin 6 and the $\overline{\text{EOG}}$ signal at A4 pin H for proper period and timing. If abnormal troubleshoot the count gate circuitry consisting of IC's A4U2 through A4U9 and their associated pull-up/pull-down resistors.

3. Monitor the $10^0$ 500 MHz Decade outputs at the following A4 pins.

| | |
|---|---|
| $\overline{\text{BCD 1}}$ | A4 pin B |
| $\overline{\text{BCD 2}}$ | A4 pin C |
| $\overline{\text{BCD 4}}$ | A4 pin D |
| $\overline{\text{BCD 8}}$ | A4 pin E |
| $\overline{\text{CARRY}}$ | A4 pin F |

If not present the problem is A4U6 the SP8635 ECL Decade Counter, refer to it's IC data sheet page 5-101 for troubleshooting information.

If the $10^0$ Decade outputs are normal the problem is then isolated down to the accumulators and storage registers located on Assemblies A3 and A1.

First verify that the $\overline{\text{STORE}}$ signal is present at A3 pin ⑫ and A1 pin Ⓝ. The $\overline{\text{STORE}}$ is required to load the measurement data from the accumulators into the storage registers. Observe the 11-digit display to determine which decade the problem is related to. Table 5-11 provides a trouble shooting chart for the A3 and A1 Assemblies.

**TABLE 5-11 A3 AND A1 FAULT ISOLATION**

| FUNCTION | IC |
|---|---|
| $10^0$ Storage Register | A3U13 |
| $10^1$ Storage Register | A3U14 |
| $10^1$ Accumulator | A3U2 |
| $10^2$ Storage Register | A3U15 |
| $10^2$ Accumulator | A3U3 |
| $10^3$ Storage Register | A3U16 |
| $10^3$ Accumulator | A3U4 |
| $10^4$ Storage Register | A3U17 |
| $10^4$ Accumulator | A3U5 |
| $10^5$ Storage Register | A3U18 |
| $10^5$ Accumulator | A3U6 |
| $10^6$ Storage Register | A1U15 |
| $10^6$ Accumulator | A1U1 |
| $10^7$ Storage Register | A1U16 |
| $10^7$ Accumulator | A1U2 |
| $10^8$ Storage Register | A1U17 |
| $10^8$ Accumulator | A1U3 |
| $10^9$ Storage Register | A1U18 |
| $10^9$ Accumulator | A1U4 |
| $10^{10}$ Storage Register | A1U19 |
| $10^{10}$ Accumulator | A1U5 |
| Resolution Digit Blanking Gate Logic | A1U7, A3U7 |
| $10^1$ through $10^6$ Digit Blanking Gates | A3U1 |
| $10^6$ through $10^{10}$ Digit Blanking Gates | A1U14 |

If a measurement unit (MU) annunciator, a decimal point (DP) or a resolution digit blanking abnormality is indicated, the problem is related to the MU and DP generation logic located on the A12 Assembly. The three 4-Input NAND gates configured by IC's U2 and U3 encodes the one-of-seven RESOLUTION switch settings into a three line 1-2-4 octal code. Using Table 5-12 as a truth table verify the resolution encode logic.

If the resolution encode logic checks out to be normal, the problem is then isolated to the MU and DP PROM A12U4. This 256 Bit PROM can be verified by using truth table 5-13 and measuring the logic levels at the input programming pins and the seven programmed output pins.

**TABLE 5-12 RESOLUTION ENCODE TRUTH TABLE**

| Resolution Switch Setting | Bit 1 A12U3-6 | Bit 2 A12U3-8 | Bit 4 A12U2-6 |
|---|---|---|---|
| 1 MHz | 1 | 1 | 1 |
| 0.1 MHz | 0 | 1 | 1 |
| 10 kHz | 1 | 0 | 1 |
| 1 kHz | 0 | 0 | 1 |
| 0.1 kHz | 1 | 1 | 0 |
| 10 Hz | 0 | 1 | 0 |
| 1 Hz | 1 | 0 | 0 |

**TABLE 5-13 MU AND DP PROM TRUTH TABLE**

| Resolution Switch Setting | PROM INPUTS | | | | | | PROM OUTPUTS | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | A | B | C | D | E | | Y1 | Y2 | Y3 | Y4 | Y5 | Y6 | Y7 |
| | Pin | 10 | 11 | 12 | 13 | 14 | Pin | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| 1 MHz | | 1 | 1 | 1 | 0 | 1 | | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 0.1 MHz | | 0 | 1 | 1 | 0 | 1 | | 1 | 0 | 0 | 0 | 0 | 1 | 0 |
| 10 kHz | | 1 | 0 | 1 | 0 | 1 | | 0 | 1 | 0 | 0 | 0 | 1 | 0 |
| 1 kHz | | 0 | 0 | 1 | 0 | 1 | | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 0.1 kHz | | 1 | 1 | 0 | 0 | 1 | | 1 | 0 | 0 | 0 | 0 | 0 | 1 |
| 10 Hz | | 0 | 1 | 0 | 0 | 1 | | 0 | 1 | 0 | 0 | 0 | 0 | 1 |
| 1 Hz | | 1 | 0 | 0 | 0 | 1 | | 1 | 1 | 0 | 0 | 0 | 0 | 1 |

*NOTE*

*Because the preceding PROM check was performed in the INSTR TEST mode the Y5 output MU Bit 4 (GHz), the Y4 output DP Bit 8 and the Y3 output DP Bit 4 will remain low.*

### 5.6.3 Control Group Troubleshooting

The control group contains the circuitry that performs digital manipulation, event timing and functional control of the counters operation. The circuitry includes the time base selection, time base modification, N computation, 10 kHz generation (LO/M), IF integration N x (IF/N) and various timing, command and flag generation circuits.

The basic function of the control group is to configure the counter into it's four operating modes and provide resolution selection. The following troubleshooting procedures thus are structured to the resolution selection and the four different modes of operation that the counter will operate in.

### 5.6.3.1 A8 Time Base PCB Assembly Troubleshooting Procedure

1. Extend the A8 Assembly using the digital extender assembly #05502901.

2. Set the counter controls as follows:

   POWER switch to ON.
   Press and latch LOW pushbutton switch.
   Rotate RECYCLE RATE control fully CW to MAX.
   Place rear panel INT/EXT switch to INT.

3. Determine if the counter is using the standard 10 MHz T.B. Osc. or the Option 12 or 13 3 MHz T.B. Osc. Insure that 3 MHz/10 MHz jumper is properly installed.

4. With an oscilloscope, verify a 3 or 10 MHz signal at A8 pin $\boxed{D}$, if not present, the problem is in the time base oscillator.

5. With an oscilloscope, verify a 1 MHz TTL clock at U19 pin 8, if not present, the problem is Q1, U15 or U19. If the standard 10 MHz T.B. Osc. is utilized, U4 could also be at fault. If the Option 12 or 13 3 MHz T.B. Osc. is utilized, U5 could also be at fault.

6. Place the rear panel INT/EXT switch to EXT. Jumper A8 pins $\boxed{D}$ and $\boxed{J}$ and verify a 1 MHz TTL clock at U19 pin 8, if not present, the problem is Q2, U15, U20 or U19. Remove the jumper from A8 pin $\boxed{D}$ and $\boxed{J}$ and return the rear panel INT/EXT switch to it's INT position.

7. Verify a 1 MHz TTL clock at A8 pin $\boxed{C}$ (1 MHz OUT) and $\boxed{B}$ (INST 1 MHz), if not present, check U14.

8. Verify a 1 MHz TTL clock at U16 pin 2, if not present problem is U21 or U7-6.

9. Verify a 1 MHz TTL clock at U16 pin 6, then jumper U16 pins 1 and 9 and verify that the 1 MHz clock at U16 pin 6 is disabled. Jumper U16 pins 2 and 4 and verify a 1 MHz clock at U16 pin 6. Remove the jumpers from U16 pins 1 - 9 and 2 - 4 and verify the presence of the 1 MHz clock at U16 pin 6. If any of the above checks proved negative, the problem is U16 or the $\overline{\text{COUNT LO}}$ command at A8 pin② is present as a logic low which relates to an A11 Function PCB Assembly problem.

10. With an Oscilloscope monitor A8 pin① (T.B. OUT) and check the time base period for each RESOLUTION switch setting.

| Resolution Switch Setting | Time Base Period At A8 Pin① |
|---|---|
| 1 MHz | 1 $\mu$s |
| 0.1 MHz | 10 $\mu$s |
| 10 kHz | 100 $\mu$s |
| 1 kHz | 1 ms |
| 0.1 kHz | 10 ms |
| 10 Hz | 100 ms |
| 1 Hz | 1s |

If any of the time base periods are abnormal, the problem is related to the time base decade counter (U8 through U13) or the gating logic comprised of U6, U7, U17 and U18.

### 5.6.3.2 A12 20 MHz Amplifier PCB Assembly Troubleshooting Procedure

1. Extend the A12 Assembly using the digital extender assembly #05502901.

2. Place the POWER switch to ON.

3. Step the RESOLUTION switch through it's seven positions from 1 MHz to 1 Hz while monitoring the logic levels on pins 10, 11 and 12 of U4. Verify the logic levels using the following truth table.

**RESOLUTION SELECT TRUTH TABLE**

| Resolution Switch Setting | Logic Levels A12U4 | | |
|---|---|---|---|
| | A | B | C |
| Pin | 10 | 11 | 12 |
| 1 MHz | 1 | 1 | 1 |
| 0.1 MHz | 0 | 1 | 1 |
| 10 kHz | 1 | 0 | 1 |
| 1 kHz | 0 | 0 | 1 |
| 0.1 kHz | 1 | 1 | 0 |
| 10 Hz | 0 | 1 | 0 |
| 1 Hz | 1 | 0 | 0 |

If the U4 A, B and C input(s) are abnormal, the problem is related to gates U3-6, U3-8 and U2-6.

4. Monitor the logic level at U4 pin 13 (PROM D input). Press and latch the LOW function switch and verify that the logic level switches from TTL high to TTL low. Unlatch the LOW function switch and verify that the logic level switches back to high. If abnormal, the problem is the LOW function switch or gate U2-8.

5. Monitor the logic level at U4 pin 14 (PROM E INPUT), alternately select NORMAL, WIDE and LOW modes of operation, verify that U4 pin 14 goes low when NORMAL or WIDE is selected and goes high when LOW is selected. If it does not, the function switch or gate U7-3 is at fault.

6. Monitor the logic levels at A12 pin $\boxed{13}$ (P.L.) and A12 pin $\boxed{L}$ ($\overline{\text{F.L.}}$) alternately select the NORMAL and WIDE modes of operation, verify that A12 pin $\boxed{13}$ goes low and A12 pin $\boxed{L}$ goes high when NORMAL is selected, and A12 pin $\boxed{13}$ goes high and A12 pin $\boxed{L}$ goes low when WIDE is selected. If abnormal, the problem is related to gating logic consisting of U7-6, U7-8, U7-11, U8-8, U11-11 and U3-11.

7. Monitor A12 pin $\boxed{15}$ ($\overline{\text{CHANGE CLEAR}}$), while stepping through all seven steps of the RESOLUTION switch, on each step change the logic level should go TTL low then return to a logic TTL high. Then alternately select LOW, NORMAL and WIDE functions, and verify that the logic level goes low and returns to a logic high on each mode change. If abnormal, the problem is related to gating logic consisting of U5, U6, U9, U10, U11 and U12.

8. Steps 3, 4 and 5 of this procedure verified the resolution and function mode input select logic which generated the programming inputs for PROM U4. If a problem with the measurement unit or decimal point generation is indicated, PROM U4 is the probable cause. To verify the proper operation and programming of the PROM U4 proceed as follows:

Select NORMAL or WIDE function mode.

Step the RESOLUTION switch through it's seven positions and verify the programmed outputs as related to the programming inputs using the following truth table.

| Resolution Switch Setting | Programming Inputs | | | | | Programmed Outputs | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | A | B | C | D | E | Y1 | Y2 | Y3 | Y4 | Y5 | Y6 | Y7 |
| U4 Pin | 10 | 11 | 12 | 13 | 14 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| .1 MHz | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 |
| 0.1 MHz | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 |
| 10 kHz | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 |
| 1 kHz | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 |
| 0.1 kHz | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 0 |
| 10 Hz | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 |
| 1 Hz | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 |

Select LOW function mode.

Step the RESOLUTION switch through it's seven positions and verify the programmed outputs as related to the programming inputs using the following truth table.

| Resolution Switch Setting | Programming Inputs | | | | | Programmed Outputs | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | A | B | C | D | E | Y1 | Y2 | Y3 | Y4 | Y5 | Y6 | Y7 |
| U4 Pin | 10 | 11 | 12 | 13 | 14 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| 1 MHz | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 0.1 MHz | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 |
| 10 kHz | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 |
| 1 kHz | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 0.1 kHz | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 |
| 10 Hz | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 |
| 1 Hz | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 |

Select NORMAL or WIDE function mode.

Jumper XA12 pin 6 to ground to simulate an auto low function mode (LOW PASS). Step the RESOLUTION switch through it's seven positions and verify the programmed outputs as related to the programming inputs using the following truth table.

| Resolution Switch Setting | Programming Inputs | | | | | | Programmed Outputs | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | U4 Pin | A 10 | B 11 | C 12 | D 13 | E 14 | U4 Pin | Y1 1 | Y2 2 | Y3 3 | Y4 4 | Y5 5 | Y6 6 | Y7 7 |
| 1 MHz | | 1 | 1 | 1 | 1 | 0 | | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 0.1 MHz | | 0 | 1 | 1 | 1 | 0 | | 1 | 0 | 0 | 0 | 0 | 1 | 0 |
| 10 kHz | | 1 | 0 | 1 | 1 | 0 | | 0 | 1 | 0 | 0 | 0 | 1 | 0 |
| 1 kHz | | 0 | 0 | 1 | 1 | 0 | | 1 | 1 | 0 | 0 | 0 | 1 | 0 |
| 0.1 kHz | | 1 | 1 | 0 | 1 | 0 | | 0 | 0 | 1 | 0 | 0 | 1 | 0 |
| 10 Hz | | 0 | 1 | 0 | 1 | 0 | | 1 | 0 | 1 | 0 | 0 | 1 | 0 |
| 1 Hz | | 1 | 0 | 0 | 1 | 0 | | 0 | 1 | 1 | 0 | 0 | 1 | 0 |

9. If the U4 PROM Y5, Y6 and Y7 outputs verify and a problem with the MU Bits 1-2-4 at A12 pins $\boxed{17}$, $\boxed{16}$ and $\boxed{5}$ is indicated, the fault is related to OR gates U13-3 and U13-6.

10. If any of the unit of measurement LED annunciators fail to illuminate when the proper resolution and function mode is selected, the problem is isolated to lamp drivers IC U14 or the LED indicator.

### 5.6.3.3 A11 Function PCB Assembly Troubleshooting Procedure

The A11 Assembly generates commands and flags to control the operation of the control group and the display circuitry. The following troubleshooting procedure is structured to verify the eighteen discreet commands and flags generated by the Function PCB Assembly and isolate any malfunction to it's possible logic component(s) failure.

1. Extend the A11 Assembly using the digital extender assembly #05502901.

2. Place the POWER switch to ON, select NORMAL mode and 1 kHz resolution.

3. Verify that a 1 MHz clock input is present at A11 pin $\boxed{E}$ if not the problem is external to the A11 assembly and related to the A8 time base assembly (refer to paragraph 5.6.3.1).

4. Monitor the $\overline{\text{LOAD SR}}$ at A11 pin $\boxed{T}$ and the CLOCK SR at A11 pin $\boxed{U}$. The $\overline{\text{LOAD SR}}$ command should go low at EOG time, if not, the problem is related to the SR gate counter A11U6 or it's associated gating logic consisting of A11U5 and A11U18.

The SR CLOCK (A11 pin $\boxed{U}$) should be a gated 1 MHz clock which has a gate period determined by the 1 ms to 1s resolution selection applied to A11 pins $\boxed{M}$, $\boxed{K}$, $\boxed{N}$ and $\boxed{L}$, if not, the problem is related to the SR clock counter A11U7 or it's associated gate control logic consisting of A11-U5, A11U8, A11U18 and A11U19.

5. Monitor the $\overline{\text{RESET DECADES}}$ A11 pin $\boxed{S}$, $\overline{\text{PRESET DECADES}}$ A11 pin $\boxed{V}$ and $\overline{\text{INHIBIT END OF COUNT}}$ A11 pin $\boxed{P}$ signals for proper functional sequence timing. The $\overline{\text{RESET DECADES}}$ signal at A11 pin $\boxed{S}$ is sent to the A1 and A3 assemblies to reset the count accumulators to zero when a $\overline{\text{RESET}}$ is applied to A11U9 pin 4 or a logic low is generated by the SR gate counter and applied to A11U9 pin 5, if not the problem relates to A11U9-6 or A11U20-6. The $\overline{\text{PRESET DECADES}}$ signal at A11 pin $\boxed{V}$ provides a command to the A1 and A3 assemblies to load the counters in the shift registers back into the accumulators when a $\overline{\text{RESET}}$ is applied to A11U9 pin 9 or a logic low is generated by the SR gate counter (A11U6 pin 8) and applied to A11U9 pin 10, if not the problem is related to A11U9-8 or A11U20-12. The $\overline{\text{INHIBIT END OF COUNT}}$ signal at A11 pin $\boxed{P}$ is sent to the A6 assembly to inhibit the generation of an EOC, this command is generated when the $\overline{\text{PHASE LOCK}}$ (A11 pin $\boxed{F}$) and the LOAD SR (A11U6-5) are NAND gated by A11U8-11, if not check A11 U8-11.

6. Monitor the $\overline{\text{PHASE LOCK INITIAL}}$ signal at A11 pin $\boxed{5}$ for proper function. This signal is applied to the A8 assembly to allow the time base to be modified to an $N \times 10^{-3}$ period. This signal is generated when the $\overline{\text{PHASE LOCK}}$ (A11 pin $\boxed{F}$) and the RESET DECADES (A11U6-9) are gated by A11U9-3. If not present problem is related to A11U9-3 OR gate or the SR gate counter A11U6.

7. Monitor the $\overline{\text{COUNT IF}}$ command at A11 pin $\boxed{\text{R}}$ for proper function. This command is applied to the A4 assembly to enable the lock IF to be counted by the 500 MHz $10^0$ decade. This command is generated when the $\overline{\text{PHASE LOCK}}$ (A11 pin $\boxed{\text{F}}$ and the RESET DECADES (A11U6 pin 8) are gate by A11U9-11. If not proper in it's function the problem is A11U6 or A11U9-11 OR gate.

8. Monitor the $\overline{\text{COUNT LO}}$ command at A11 pin $\boxed{4}$ for it's proper function. This command is applied to the A4 and A8 assemblies to enable the LO frequency to be counted for a 1 MHz/N period. This command is generated when the $\overline{\text{FREQ LOCK}}$ (A11 pin $\boxed{\text{D}}$) and the $\overline{\text{PHASE LOCK INITIAL}}$ (A11U9-3) are gated by AND gate A11U17-6. If not proper in it's function, the problem is related to A11U17-6, A11U9-3 or A11U6 SR gate counter.

9. Monitor the $\overline{\text{RESET}}$ signal at A11 pin ④ for proper function. This signal is applied to the A4, A6 and A8 assemblies to perform a number of different reset operations. The RESET signal is generated by any one of the following A11 logic operations:

a. Generation of the $\overline{\text{DEMAND CLEAR}}$ at gate A11U16-3.

b. A logic low at A11U2-4 that is generated at the end of the $\overline{\text{CLOCK SR}}$ period (A11 U18-11 gate).

c. End of Display Period. This logic function consists of timer A11U21 which is triggered by the EOC signal applied to A11 pin ③ and timed by the DISPLAY control potentiometer setting at A11 pin Ⓑ.

d. A $\overline{\text{SAMPLE}}$ input at A11 pin Ⓒ.

e. A $\overline{\text{PL RESET}}$ input at A11 pin Ⓕ.

f. A $\overline{\text{CHANGE CLEAR}}$ input at A11 pin Ⓔ.

If the generation of the $\overline{\text{RESET}}$ signal does not function properly to any of the above listed logic operations, refer to Figure 7-17, A11, Function PC Assembly schematic diagram to isolate the problem down to the IC component level.

10. Monitor the $\overline{\text{STORE}}$ command at A11 pin Ⓓ for proper function. This command is applied to the A1 and A3 assemblies to load the storage registers and to the A6 assembly to generate the $\overline{\text{LEAD ZERO DISABLE}}$ signal at A6 pin ④. The $\overline{\text{STORE}}$ command is generated when a STORE is generated by one-shot M.V. A11U12 pin 5, an $\overline{\text{EOG}}$ signal is applied to A11 pin $\boxed{\text{C}}$ or on a DEMAND CLEAR (A11U15-2) generation. If the $\overline{\text{STORE}}$ is not proper in it's functional generation, the problem is related to A11U11-10, A11U19-3, A11U12, A11U1-12 or A11U16-8.

11. Monitor the $\overline{\text{DEMAND CLEAR}}$ command at A11 pin Ⓤ. The $\overline{\text{DEMAND CLEAR}}$ is applied to A1 and A3 assemblies to reset their shift registers. The DEMAND CLEAR is generated by any one of the following A11 logic operations.

a. A $\overline{\text{LOW PASS}}$ input at A11 pin $\boxed{\text{B}}$ which will trigger one-shot M.V. A11U22-5.

b. A manual momentary closure of the front panel RESET switch thus generating a $\overline{\text{RESET PUSH-BUTTON}}$ input at A11 pin ⑰ .

c. A momentary loss of +5V $V_{CC}$ detected by the "power glitch detector" A11Q2 and it's associated RC components.

d. An $\overline{\text{ACTO}}$ command input at A11 pin ⑫ .

e. The dropping of the MODIFIED SQUELCH signal applied to A11 pin Ⓜ while the ACTO input is active.

If the $\overline{\text{DEMAND CLEAR}}$ command fails to generate in response to any of the above logic operations check the following circuit components: A11U3-10, A11U15, A11R14, A11R15, A11C6, A11CR1, A11U16-3, A11U13-8, A11U3-12, A11U22-5 and it's associated RC timing components, A11U20-8, A11Q2, A11R28, A11R29 and A11C11.

12. Monitor the $\overline{\text{RESET N}}$ signal at A11 pin $\boxed{2}$ for proper logic generation. This signal is applied to A10 assembly to aid in the generation of the $\overline{\text{RESET ACTO}}$ signal. The $\overline{\text{RESET N}}$ is generated when the $\overline{\text{RESET PUSH-BUTTON}}$ or $\overline{\text{LOW PASS}}$ signals are applied to A11 pin ⑰ or A11 pin $\boxed{\text{B}}$

respectively. If the $\overline{\text{RESET N}}$ fails to generate the problem is related to the following components: A11U16-6, A11U13-1, or the circuits related to the LOW PASS logic functions that was checked in the preceding step.

13. Monitor the $\overline{\text{GATE LAMP}}$ drive at A11 pin $\boxed{14}$ . This signal is applied to the A13 assembly as a ground return to illuminate the GATE LED indicator A13DS4. The $\overline{\text{GATE LAMP}}$ drive is generated when the GATE signal is applied to A11 pin Ⓛ. If not functional, check one-shot MV A11U2-5, A11R2, A11C3 and gate A11U13-6 or inverter A11U3-2.

14. Monitor the $\overline{\text{OVERLOAD LAMP}}$ A11 pin Ⓝ, the OVERLOAD A11 pin Ⓟ and the BLINK A11 pin Ⓣ. These three signals are generated when an analog OVERLOAD signal from assembly A15 is applied to A11 pin $\boxed{17}$ . If all three of these signals fail to generate the problem is related to A11-Q1, A11U15-4, or A11R8 through A11R10. If the $\overline{\text{BLINK}}$ and $\overline{\text{OVERLOAD LAMP}}$ drives fail to generate the problem is related to timer/flasher A11U14 and it's associated RC components or the inverter drivers A11U3-8 and A11U3-6 respectively.

15. Monitor the $\overline{\text{LOCK LAMP}}$ A11 pin Ⓢ and the $\overline{\text{LOCK}}$ A11 pin $\boxed{J}$ . These signals are generated when the $\overline{\text{LOW PASS}}$ at A11 pin $\boxed{B}$ or the N COMPUTED at A11 pin Ⓙ and the MODIFIED SQUELCH at A11 pin Ⓜ are applied to the A11 assembly. The $\overline{\text{LOCK}}$ will "flash" alternately with the $\overline{\text{OVERLOAD LAMP}}$ signal at A11 pin Ⓝ when an overload is detected by A11Q1. If the $\overline{\text{LOCK LAMP}}$ or $\overline{\text{LOCK}}$ signals fail to generate properly, the problem is related to A11U4-8, A11U4-6, A11U3-4 or the circuitry relating to the OVERLOAD and $\overline{\text{BLINK}}$ functions checked in step 14 of this procedure.

### 5.6.3.4 A10 N Computer PCB Assembly Troubleshooting Procedure

The N Computer Assembly determines the harmonic number (N) and generates control, command and flag signals required for the ACTO and FLACTO conversion operations. The N Computer provides five different subfunctions which are listed as follows:

a. Harmonic Number (N) Determination.

b. 1 MHz/N Signal Generation.

c. IF/N Signal Generation.

d. 10 kHz Reference and 10 kHz Gate Signal Generation.

e. Squelch and N Inhibit Signal Generation.

The following procedure is structured to the five subfunctions listed above.

1. Extend the A10 Assembly using the digital extender assembly #05502901.

2. Place the POWER switch to ON, and apply a 1 GHz -20 dBm signal to the counter.

3. Select WIDE or NORMAL function as appropriate for the following procedural steps.

4. Troubleshoot the Harmonic number (N) determination circuitry as follows:

    a. Select NORMAL mode and verify that the LOCK illuminates.

    b. Verify that the 1 kHz x N clock is being inputted at A10 pin Ⓢ.

    c. Verify that the 1 kHz clock is being applied at A10 pin ⑩ .

    d. Monitor A10U18 pin 1 to verify that a $\overline{\text{LOAD}}$ command is being applied to counter A10U18 during the N determination cycle. If the $\overline{\text{LOAD}}$ command is not present the problem is related to A10U7, A10U2-9, A10U1-8 or A10U16-11.

    e. Verify the N number generated as a 8-bit binary format on A10U4 Q1 through Q8 outputs. If the N number 8-bit binary is not present at A10U4 outputs or it is determined that an incorrect N number is being computed, the problem is related to A10U18, A10U4, A10Q3 or A10Q4.

5. Troubleshoot the 1 MHz/N signal generation circuitry as follows:

    a. Select WIDE mode, 1 kHz resolution and verify the LOCK illuminates.

b. Verify that the 1 MHz clock is being applied at A10 pin ⑰.

c. Verify that an ECL level 1 MHz clock is present at A10U9 pin 6, if not the problem is related to A10Q2 or it's associated resistors.

d. Monitor the 1 MHz/N output signal at A10 pin $\boxed{A}$ if not present the problem is the programmable ÷N binary counters A10U9 and A10U14 or the line driver A10U23-6.

e. Monitor the N COMPUTED flag at A10 pin Ⓐ, it should go to a logic TTL high at the conclusion of an N determination cycle. If not, the problem is related to A10U16-3, A10U11-8, A10Q6 or diodes A10CR2 and A10CR3.

6. Troubleshoot the IF/N signal generation circuitry as follows:

a. Select WIDE mode, 1 kHz resolution and verify that LOCK illuminate.

b. Verify that the IF signal is being applied via it's shielded pair cable at A10 pin $\boxed{R}$ and $\boxed{P}$.

c. Check the ECL IF differential output at A10U28 pins 10 and 14, if not present, replace IC A10U28.

d. Verify the presence of the $\overline{\text{FREQUENCY LOCK}}$ and GATE at A10 pins $\boxed{V}$ and $\boxed{U}$ respectively.

e. Check out the gating and TTL-to-ECL logic translation of the GATE performed by gates A10U28-13 and -15, if not proper, replace A10U28.

f. Monitor the IF/N output signal at A10 pin $\boxed{T}$, if not present, the problem is related to A11U23-13, A10U27, or A10U22.

7. Troubleshoot the 10 kHz reference and 10 kHz GATE signal generation circuitry as follows:

a. Select NORMAL mode 1 kHz resolution.

b. Verify that the 1 MHz reference clock is being applied to A10 pin ⑰.

c. Monitor the 10 kHz reference output at A10 pin ⑨, if not present, the problem is related to A10U12 or A10U17.

d. Verify that the $\overline{\text{PHASE LOCK}}$ flag is being applied to A10 pin ①.

e. Monitor the 10 kHz GATE output and it's associated output flags as indicated below:

10 kHz GATE A10 pin ⑯
$\overline{\text{10 kHz COMPUTED}}$ flag A10 pin ⑤
$\overline{\text{PHASE LOCK RESET}}$ flag A10 pin Ⓔ
$\overline{\text{CLEAR 10 kHz}}$ flag A10 pin Ⓒ

If the 10 kHz GATE or any of the flags are not being properly generated, the problem is related to A10U10, A10U15, A10U3, or A10U5-4.

8. Troubleshoot the Squelch and N Inhibit signal generation circuitry as follows:

a. Verify that the SQUELCH (COUNTER RESET) at A10 pin ⑬, the $\overline{\text{SQUELCH}}$ (IF LOCK) at A10 pin ④ and the $\overline{\text{TEST}}$ at A10 pin Ⓤ are applied and are in the proper operational mode sequence.

b. Monitor the MODIFIED SQUELCH output signal at A10 pin ⑧, if it is not being generated properly, the problem is related to A10U10.

c. Monitor the N INHIBIT output signal at A10 pin $\boxed{5}$, if it is not being generated properly, the problem is related to A10U28-4, A10U13, A10U16-6, A10U11-6, A10U6 or A10Q1.

d. Verify that the RAMP signal at A10 pins $\boxed{2}$ and $\boxed{B}$ is properly applied.

e. Monitor the SQUELCH output signal at A10 pin ⑥, if it is not being generated properly, the problem is related to A10U19-7, A10U23-4 and -12, A10U20-6, A10U20 or A10U24-8 and -11.

### 5.6.3.5 A9 10 kHz Generator PCB Assembly Troubleshooting Procedure

The A9 assembly contains the "M" counter logic which divides the LO signal from the A16 assembly to 10 kHz as the VCO/N signal which is applied to the A15 search oscillator circuit. Two control signals are applied to the 10 kHz Generator PCB Assembly, the 10 kHz GATE at A9 pin Ⓡ which will set the "M" divider chain and lock up the loop, and the $\overline{\text{CLEAR 10 kHz}}$ at A9 pin Ⓒ which will reset the "M" divider when phase lock is dropped, thus allowing the search oscillator to sweep and rephase-lock the L.O.

1. Extend the A9 Assembly using the digital extender assembly #05502901.

2. Place the POWER switch to ON.

3. Select the NORMAL mode, 1 kHz resolution.

4. Apply a 1 GHz signal to the 20 MHz - 24 GHz input connector.

5. Verify that a L.O. signal is applied across A9 pins $\boxed{K}$ and $\boxed{J}$.

6. Verify that the L.O. signal is present as an output across A9 pins $\boxed{L}$ and $\boxed{M}$, if not check A9U17.

7. Monitor A9 pin ⑯ and verify a proper 10 kHz VCO/N output, if not present or if it is not a 10 kHz increment of the N number troubleshoot the "M" divider counter circuitry.

8. Verify a logic high at the 10 kHz GATE input at A9 pin Ⓡ and check that the "M" counter sets and locks up the loop, if not, troubleshoot the M counter set gating logic.

9. Momentarily press RESET pushbutton to generate a $\overline{\text{CLEAR 10 kHz}}$ reset and verify that the M divider resets, thus allowing the search oscillator to sweep and rephase-lock. If the "M" divider does not reset check A9U2 and A9U3.

### 5.6.4 Conversion Group Troubleshooting

The conversion group consists of the ACTO Module Assemblies A14 through A17, the 500 MHz Pre Amplifier PC Assembly, the PIN Leveler U1, the Power Divider/Detector U2 and the Mixer/Sampler U3 and U4.

U1 through U4 are not field repairable and must be replaced if they are determined to be faulty.

The ACTO plug-in Modules A14 through A17 consists of PCB's mounted inside of RFI enclosures, and will not function properly if the RFI integrity of the external enclosure or the interstage shielding is compromised.

Figure 5-28 provides a functional diagram of the conversion group circuitry which will aid in the fault isolation to any of the non-repairable U1 through U4 components or to a functional circuitry group within any ACTO module assembly.

#### 5.6.4.1 PIN Attenuator U1 Troubleshooting

The PIN Attenuator is a non-repairable solid state control device that functions as an input coupler and a variable attenuator. It consists of a straight through transmission line using PIN diodes in shunt for level control attenuation of the input signal. The impedance of the device is controlled by the AGC signal from assembly A15-J2 which is applied to it's control port. An input signal within the power range of the device will develop little or no AGC feedback and the PIN diodes will appear as a high impedance across the line providing an insertion loss of less than 3 dB. As the input signal level increases, the AGC signal will increase thereby turning on the PIN diodes which will adversely affect the line impedance. The resulting discontinuity will reflect most of the incident power and provide >40 dB of attenuation.

If the PIN attenuator is suspected of attenuating the input signal adversely or not coupling the input signal to the Power Divider/Detector U2, perform the following procedure.

1. Configure test set-up depicted in Figure 5-29.

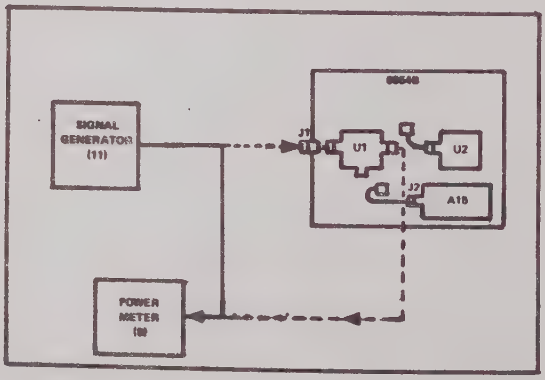


FIGURE 5-29 PIN ATTENUATOR U1 VERIFICATION TEST SETUP

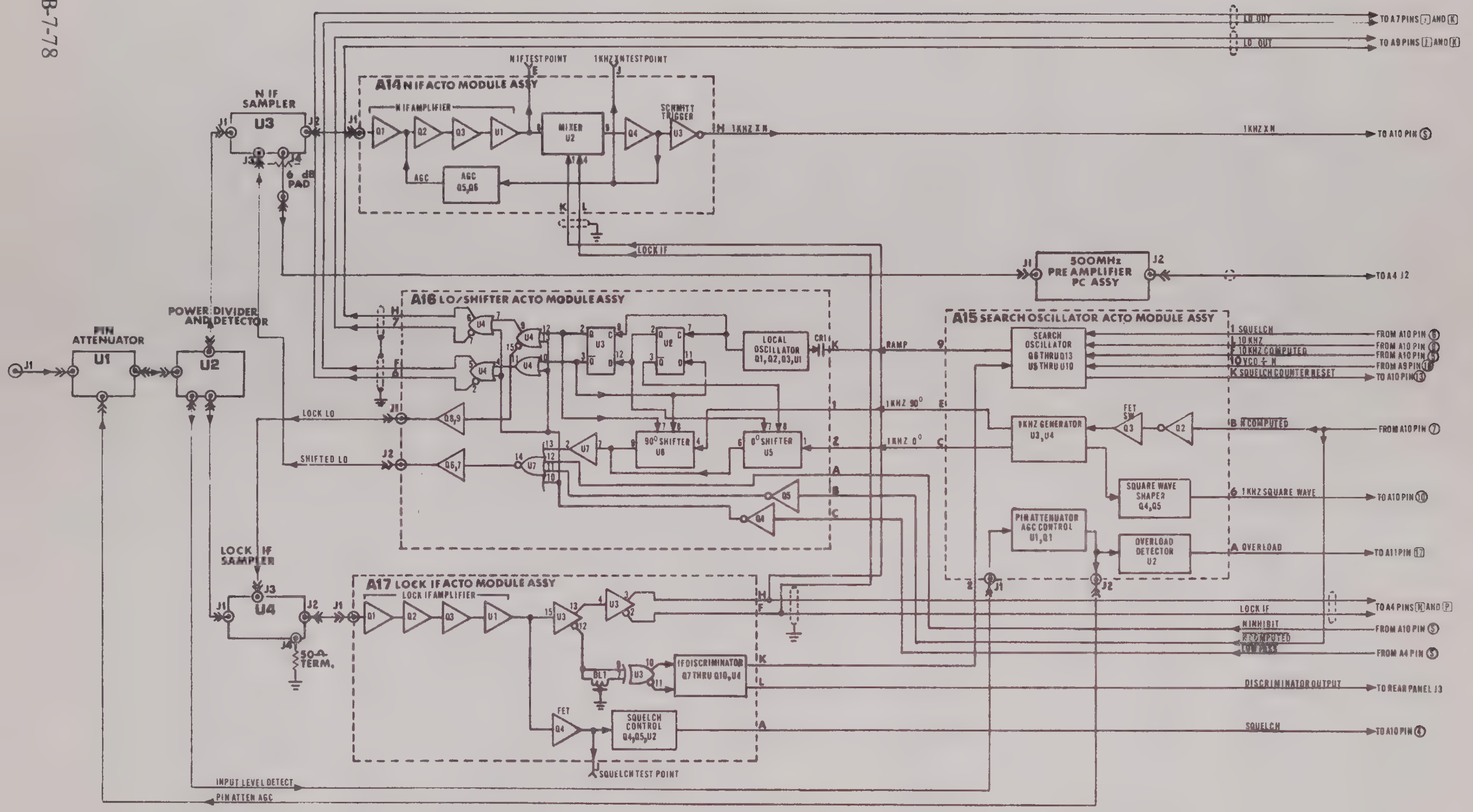

J1
PIN ATTENUATOR
U1
POWER DIVIDER AND DETECTOR
U2
N IF SAMPLER
U3
J1
J2
J3
J4
6 dB PAD
LOCK IF SAMPLER
U4
50Ω TERM.
N IF TEST POINT
1KHZ x N TEST POINT
A14 N IF ACTO MODULE ASSY
N IF AMPLIFIER
Q1
Q2
Q3
U1
AGC
AGC Q5,Q6
MIXER U2
Q4
SCHMITT TRIGGER
U3
1KHZ X N
LOCK IF
500MHz PRE AMPLIFIER PC ASSY
TO A4 J2
A16 LO/SHIFTER ACTO MODULE ASSY
U4
U3
U2
LOCAL OSCILLATOR Q1, Q2, Q3, U1
CR1
90° SHIFTER U6
0° SHIFTER U5
U7
Q8,9
Q6,7
Q5
Q4
LOCK LO
SHIFTED LO
RAMP
1KHZ 90°
1KHZ 0°
A15 SEARCH OSCILLATOR ACTO MODULE ASSY
SEARCH OSCILLATOR Q6 THRU Q13 U5 THRU U10
9KHZ GENERATOR U3, U4
FET SW
Q3
Q2
SQUARE WAVE SHAPER Q4, Q5
PIN ATTENUATOR AGC CONTROL U1, Q1
OVERLOAD DETECTOR U2
1 SQUELCH
L 10 KHZ
F 10 KHZ COMPUTED
10 VCO ÷ N
K SQUELCH COUNTER RESET
B N COMPUTED
6 1KHZ SQUARE WAVE
A OVERLOAD
A17 LOCK IF ACTO MODULE ASSY
LOCK IF AMPLIFIER
Q1
Q2
Q3
U1
U3
U3
DL1
IF DISCRIMINATOR Q7 THRU Q10, U4
FET
Q4
SQUELCH CONTROL Q4, Q5, U2
SQUELCH TEST POINT
INPUT LEVEL DETECT
PIN ATTEN AGC
LO OUT
LO OUT
TO A7 PINS J AND K
TO A9 PINS J AND K
TO A10 PIN S
FROM A10 PIN 6
FROM A10 PIN 8
FROM A10 PIN 5
FROM A9 PIN 14
TO A10 PIN 13
FROM A10 PIN 7
TO A10 PIN 10
TO A11 PIN 17
LOCK IF
N INHIBIT
N COMPUTED
LOW PASS
TO A4 PINS N AND P
FROM A10 PIN 5
FROM A4 PIN 5
DISCRIMINATOR OUTPUT
TO REAR PANEL J3
SQUELCH
TO A10 PIN 4

FIGURE 5-28 CONVERSION GROUP TROUBLESHOOTING SCHEMATIC DIAGRAM

2. Adjust signal generator for a +0 dBm on the power meter at 550 MHz, or frequency of difficulty.

3. Disconnect coax cable supplying the AGC signal to U1, disconnect coax cable from U1 output connector.

4. Disconnect power meter from the signal generator and connect it to the U1 output connector.

5. Connect the signal generator to the counters 20 MHz - 24 GHz input connector (J1)

6. Observe the reading on the power meter, it should be > -3 dBm.

If the PIN Attenuator is suspected of not leveling high level (≥0 dBm) input signals properly, perform the Leveler Final Adjust procedure paragraph 5.4.6.5.

### 5.6.4.2 Power Divider/Detector U2 Troubleshooting

The power divider/detector U2 is a non-repairable solid state device. It consists of a balance T and an RF detector. It accepts RF input from the PIN Attenuator U1, and splits it for distribution to the samplers U3 and U4. The loss between it's input port and it's two output ports should be 6 dB ±2 dB from dc to 500 MHz and 8 dB ±3 dB from 500 MHz to 24 GHz. The detector output should generate ≈5 mV detector level for a -20 dB signal at it's output ports.

If the power divider/detector is suspected to be faulty, perform the following procedure.

1. Disconnect all the coax cables from the power divider/detector. Remove U2 from the counter.

2. Configure test set up depicted in Figure 5-30.

3. Connect the signal generator (11) to the power meter (9). Adjust the signal generator for a -10 dBm reading on the power meter at 500 MHz.

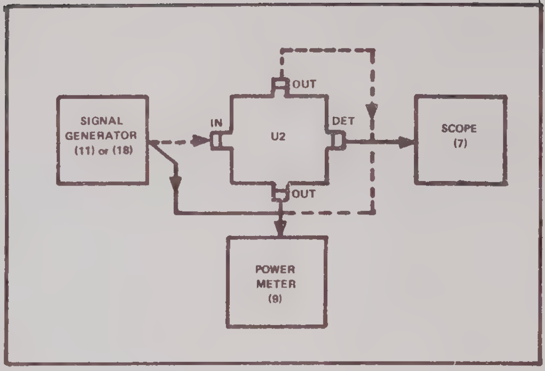


FIGURE 5-30 POWER DIVIDER/DETECTOR U2 VERIFICATION TEST SETUP

4. Connect the signal generator to the IN port of U2. Connect the power meter to one of the U2 OUT ports and terminate the other U2 OUT port with a 50Ω terminator and note the power meter reading. It should be 6 dB ±2 dB less than the -10 dBm level applied to the IN port.

5. Connect the power meter to the other OUT port and terminate the OUT port that was output level measured in step 5 with a 50Ω terminator, and note the power meter reading. It should be 6 dB ±2 dB less than the level applied to the IN port.

6. Decrease the output level of the signal genertor until the power meter indicates -20 dBm at the OUT port. With the oscilloscope, measure the DET output level, it should be ≥5 mV.

7. Connect the signal generator (18) to the power meter (9). Adjust the signal generator for a -10 dBm reading on the power meter at 24 GHz.

8. Connect the signal generator to the IN port of U2. Connect the power meter to one of the U2 OUT Ports and terminate the other U2 OUT port with a 50Ω terminator. Tune the frequency of the signal generator from 18 GHz to 24 GHz, and note the power meter reading. It should be 8 dB ±3 dB less than the -10 dBm level applied to the IN port.

9. Connect the power meter to the other OUT port and terminate the OUT port that was output level measured in step 8 with a 50Ω terminator. Tune the frequency of the signal generator from 18 GHz to 24 GHz, and note the power meter reading. It should be 8 dB ±3 dB less than the -10 dBm level applied to the IN port.

### 5.6.4.3 N IF Mixer U3 And Lock IF Mixer U4 Troubleshooting

The mixers U3 and U4 are identical non-repairable microwave mixer circuits employing conventional sampling techniques to reduce the RF input to an IF that may be counted using direct counting techniques.

If a problem relating to U3 or U4 is indicated, the first step is to verify that the proper L.O. signal is being applied. The LOCK L.O. signal applied to U4-J3 can be checked with an oscilloscope at A16-J1 and the SHIFTED L.O. signal applied to U3-J3 can be checked with an oscilloscope at A16-J2.

If the U3 or U4 mixer is suspected to be faulty they may be cross substituted, since they are identical, then verified by performing the A17 Lock IF Sensitivity Final Adjust procedure in paragraph 5.4.6.3.

### 5.6.4.4 Lock IF ACTO Module Assembly A17 Troubleshooting

The lock IF ACTO module contains three functional circuit elements.

1. A three stage staggered tuned 30 MHz IF amplifier having a band-pass of 10 MHz.

2. The squelch detector and control circuit.

3. The IF discriminator circuit.

The A17 module can be troubleshooted by performing the following step procedure.

1. Place the 6054B counter in the TEST mode and ground XA15 pin 1 to disable the SQUELCH signal to the search oscillator circuit.

2. Connect the horizontal input of an oscilloscope (7) to the RAMP signal at XA15 pin 9. Connect the vertical input of the oscilloscope to XA17 pin J (SQUELCH TEST POINT).

3. Apply a 520 - 550 MHz at -40 dBm from a sweep generator (19) to the front panel input connector J1.

4. A waveform representing the lock IF bandpass as depicted in Figure 5-31 should be observed on the oscilloscope. It indicates an envelop of the 30 MHz IF having a band-pass of 10 MHz and a amplitude of ⩾200 mV.

5. If the lock IF waveform is not present or abnormal the problem is related to A17Q1, A17Q2, A17Q3, A17U1 or A17Q4. First re-perform the A17 Lock IF Initial Alignment described in paragraph 5.4.5.2, if abnormal. If alignment does not correct the problem, then troubleshoot the lock IF amplifier circuit.

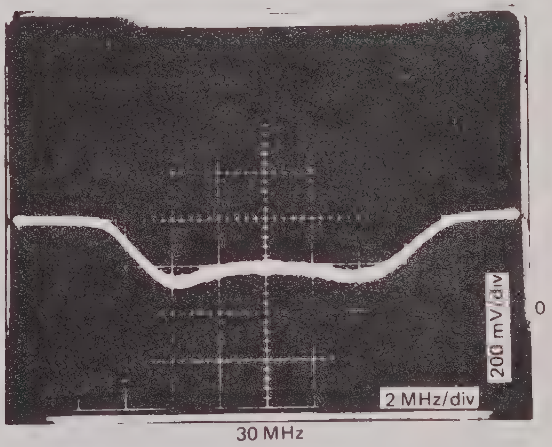


FIGURE 5-31 A17 PIN J TEST POINT, LOCK IF BAND-PASS WAVEFORM

6. Maintain the test configuration setup in steps 1 and 2, and relocate the oscilloscope vertical input to XA17 pin A to observe the SQUELCH waveform. Figure 5-32 depicts the proper waveform.

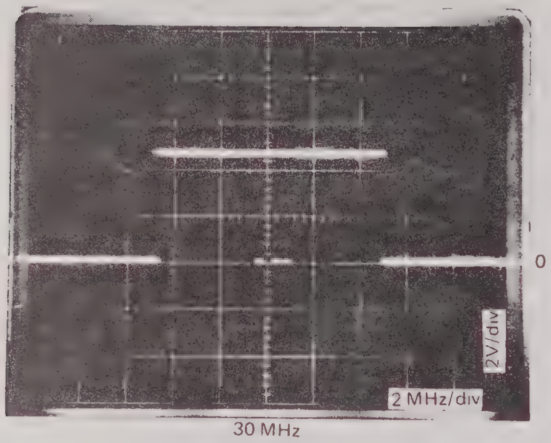


FIGURE 5-32 A17 PIN A, SQUELCH WAVEFORM

If the SQUELCH waveform is not present or abnormal, the problem is related to A17Q5, A17Q6 or A17U2. Adjustment of A17R27 (SQUELCH THRESHOLD) potentiometer may correct the problem, if it does not, troubleshoot the squelch detector control circuit.

7. Remove the vertical input connection of the oscilloscope from XA17 pin J and connect it to XA17 pin L to observe the discriminator output "S" curve. Figure 5-33 depicts the proper waveshape.

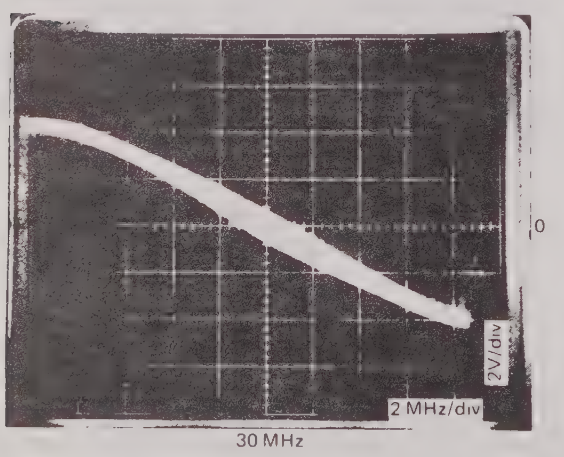


FIGURE 5-33 A17 PIN L, DISCRIMINATOR "S" CURVE WAVESHAPE

8. If the discriminator "S" curve is not present or is abnormal the problem is related to A17U3 or A17Q7 through A17Q10. Adjustment of potentiometers A17R35 and A17R49 may correct the abnormality of the discriminator "S" curve, if it does not, troubleshoot the discriminator circuit.

9. Remove the ground connected to XA15 pin 1. Place the 6054B counter in the NORMAL mode, and apply a 500 MHz -15 dBm signal to the front panel input connector J1.

10. With an oscilloscope monitor XA17 pin K, which is the discriminator output to the search oscillator. It should be a dc level after the counter locks up it's IF loop. If it is not present check A17U4 for possible failure.

11. Monitor the Lock IF output across XA17 pins H and F, if not present the problem is related to A17U3.

### 5.6.4.5 N IF ACTO Module Assembly A14 Troubleshooting

The N IF ACTO module provides for the generations of the 1 kHz x N signal by mixing the IF output from the N IF Sampler U3 with the LOCK IF signal from the ACTO module A17.

The A14 N IF ACTO module can be troubleshooted by performing the following step procedure.

1. Place the 6054B counter in it's TEST mode and ground XA15 pin 1 to disable the SQUELCH signal applied to the search oscillator.

2. Connect the horizontal input of the oscilloscope (7) to the RAMP signal at XA15 pin 9.

3. Apply a 520 - 500 MHz at -40 dBm from the sweep generator (19) to the front panel input connector J1.

4. A waveform representing the N IF band-pass as depicted in Figure 5-34 should be observed on the oscilloscope. The oscilloscope display is an envelop of the 30 MHz N IF having a 10 MHz bandpass and an amplitude of $\geqslant$200 mV.

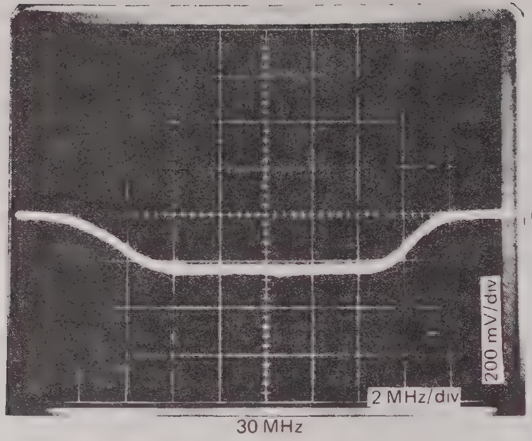


FIGURE 5-34 A14 PIN E TEST POINT, N IF BAND-PASS WAVEFORM

5. If the N IF waveform is not present or is abnormal, the problem is related to A14Q1 through A14Q3 or A14U1. If abnormal, first re-perform the A17 N IF Initial Alignment, steps 1 through 4 of paragraph 5.4.5.3. If alignment does not correct the problem, then troubleshoot the N IF amplifier circuit.

6. With an oscilloscope verify that a proper Lock IF signal is being applied to XA14 pins K and L.

7. Monitor XA14 pin J (1 kHz x N TEST POINT) with an oscilloscope, a 2V p - p sinewave as depicted in Figure 5-35 should be present.

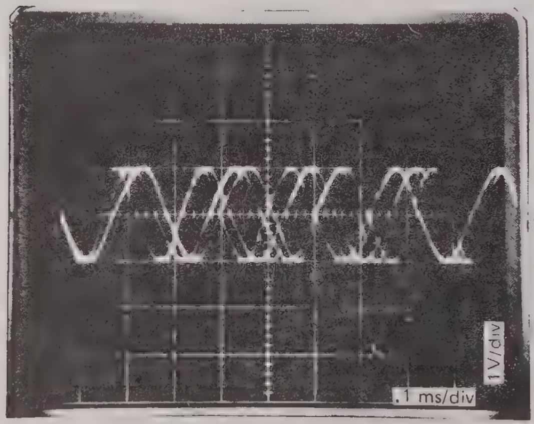


FIGURE 5-35 A14 PIN J, 1 kHz x N TEST POINT WAVESHAPE

If not present or is abnormal the problem is related to the N Mixer A14U2 or transistors A14Q4 through A14Q6.

### 5.6.4.6 LO/Shifter ACTO Module Assembly A16 Troubleshooting

The local oscillator/shifter module A16 contains the VCO local oscillator and the 1 kHz shifter SSB generator circuits. It supplies the shifted LO signal to the N IF Sampler U4. It also supplies the lock L.O. via shielded pairs to the 10 kHz Generator Assembly A10 and the 500 MHz Decade Assembly A4 which are part of the Control Group.

If the LO/Shifter module is suspected of being faulty, the first step is to perform the A16 LO and 0 shifter alignment procedure in paragraph 5.4.5.4. If alignment does not clear the problem or alignment cannot be completed due to a circuit fault then proceed with the following step procedure.

1. Place the 6054B counter in TEST mode and ground XA16 pins B and C to prevent the inhibiting of the Lock LO and Shifted LO outputs on a Low Pass flag or the inhibiting of the Shifted LO on an N Computed flag.

2. Apply 550 MHz at -15 dBm to the front panel input connector J1.

3. With a counter (6) measure the Lock LO output at XA16 pin F and note it's frequency. If the Lock LO output is not present the problem is related to the local oscillator circuit comprised of A16Q1 through A16Q3 and A16U1 through A16-U4, or the Lock LO driver A16Q6 and A16Q7.

4. With counter (6) measure the Shifted LO output at A16J2, a signal 1 kHz higher in frequency than the Lock LO signal measured in step 3 should be present. If the shifted LO output is not present or abnormal the problem is related to the SSB generator (shifter) IC A16U6, gate A16U7 or the shifted LO driver circuit A16Q8 and A16Q9.

### 5.6.4.7 Search Oscillator ACTO Module Assembly A15 Troubleshooting

The search oscillator module A15 contains four functional circuits:

1) PIN Level Detector
2) 1 kHz Generator
3) Phase Detector
4) Search Oscillator

The PIN level detector circuit provides AGC feedback to the PIN Attenuator U1 to level the input signal, and generates the OVERLOAD flag when an input of >+20 dBm is applied to the front panel J1 connector. If the level detector circuit is suspected of being faulty the first step is to perform the Leveler Final Adjust and/or the Overload Final Adjust procedures paragraphs 5.4.6.5 and 5.4.6.6. If alignment does not clear the problem, then troubleshoot the circuit consisting of A15U1, A15Q1 and A15Q2.

The 1 kHz generator circuit is comprised of A15U3 and U4 configured as a 1 kHz oscillator, the oscillator gate circuit A15Q2 and Q3 and the square wave shaper circuit A15Q4 and Q5. To troubleshoot the 1 kHz generator verify 1 kHz sinewaves displaced 90° in phase at XA15 pins C and E with the use of an oscilloscope. If they are not present or abnormal, the problem is related to the gate circuit comprised of transistor A15Q2 and FET switch A15Q1 or the 1 kHz oscillator comprised of A15U1 and U2. Next verify a 1 kHz TTL squarewave at XA15 pin 6, if not present or abnormal, the problem is related to the squarewave shaper circuit comprised of A15Q4 and A15Q5.

When the counter is operating in the NORMAL mode (FLACTO) the search oscillator is inhibited and the LO will lock up on a 10 kHz increment. If the counter will not phase lock the problem is related to the phase detector circuit. Troubleshoot the phase detector circuit as follows:

1) Place the counter in the NORMAL mode.

2) Observe the VCO signal at XA15 pin 9. If the VCO signal is abnormal or phase lock cannot be obtained the probelm is thus isolated to the phase detector A15U5, the lead-lag RC filter (A15-C23 and C24 and R33 through R40), or differential amplifier A15U6, Q6, Q7, Q10 or Q12.

When the counter is operating in the WIDE Mode (ACTO) the search oscillator circuit is enabled and will provide the VCO control of the L.O. If proper WIDE (ACTO) Mode of operation cannot be obtained, a problem with the search oscillator circuitry is indicated. Before troubleshooting the circuitry perform the Search Oscillator A15 Initial Alignment, paragraph 5.4.5.1, the A15 Lock IF Final Adjust paragraph 5.4.6.1 and the A15 Search Oscillator Final Adjust paragraph 5.4.6.2 procedures. If adjustment will not correct the probelm or adjustment procedures cannot be completed due to abnormal indications, then troubleshoot the search oscillator circuitry referring to Figure 7-27 schematic diagram and the following circuit analysis.

When the counter is not locked and LO is searching, the search oscillator circuit (A15U7, U8 and U9) should generate a ramp signal. This ramp signal is amplified by A15U10 and applied to the LO via A15 pin 9. Two potentiometers adjustments A15R44 (SWEEP LIMIT) and A15R57 (DC LEVEL SHIFT) provides for the ramp alignment. The counter should frequency lock up on the LOCK IF DISCRIMINATOR signal applied to A15 pin 2 when the SQUELCH signal is applied as a gate enable at A15 pin 1.

Potentiometer A15R30 provides for the adjustment of the Lock IF discriminator level to the source of FET A15Q9. The above described function should allow an AFC voltage to be applied LO via A15 pin 9 to effect a high gain AFC loop which will maintain the IF at 30 MHz.

### 5.6.4.8 Data Interface Group Troubleshooting

The IEEE data interface group consists of assemblies A2, A5, A7, A20 and A21. These assemblies are so interrelated that the data interface circuits must be troubleshot as a subsystem after it has been ascertained that the counter operates properly when used as a stand-alone instrument.

Troubleshoot the data interface circuits using the following procedure.

1. Place the Counter in its wake-up condition performing the data interface test outlined in 5.3.8, steps a through c.

2. If all wake-up conditions are absent or incorrect, check A20U8, A20U13, A20U14 and A20U15.

If the resolution is incorrect check A5U8, A5U2 and A5U3, and associated buffers.

If the mode selection is not set to NORMAL, check A5U12, A5U9, A5U11 and A20U1 and A20U2.

If the HOLD function is incorrect, check A5U2.

3. Verify the operation of the remaining functions by performing the procedures outlined in 3.7.3 for all functions listed in Troubleshooting Table 5-14. Enter the appropriate ASCII Character on the programmable calculator (21) and observe the Counter response.

4. If the Counter does not respond to any of the function commands, the handshake circuits may be faulty. Check A7U7, A7U8, A7U9 and A7U10.

5. If the Counter does not respond to one or more commands refer to the Troubleshooting Table 5-14. This Table lists each function, the program bit pattern on the data lines, the ASCII character of the function, and the components which should be checked for the specific command fault. When checking any circuit, note the state in which the program bits should be and check the circuits involved with any state changes.

6. After completing a function check, address the Counter to talk. This allows the Counter to send measurement data to the calculator (or line printer) one digit at a time over the data lines. Compare the Counter readout with that received at the calculator, refer to Table 3-7. If one or more digits are incorrect or missing, check A2U1 through A2U7 as appropriate.

## 5.7 INTEGRATED CIRCUITS DATA

The Model 6054B-6068 contains three IC Programmed Read Only Memory (PROM) components that are unique and must be ordered by Systron-Donner part number. Figures 5-36, 5-37 and 5-38 provide pinning information and programming data on these PROM's. All other IC components are standard and are referenced to manufacturers part numbers on the schematic diagrams. If more significant data is required, refer to the appropriate manufacturers specification sheet and/or catalog.

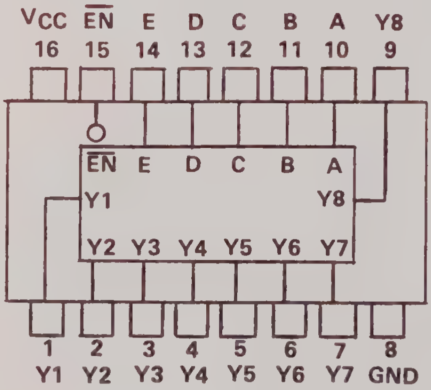
### TABLE 5-14 DATA INTERFACE TROUBLESHOOTING

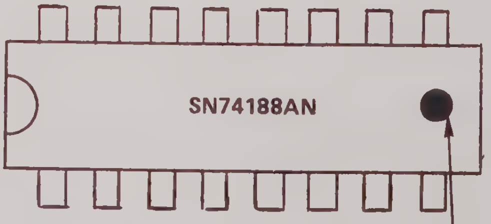
| Function | Program Bits | | | | | | | ASCII Character | Possible Cause Of Error |
|---|---|---|---|---|---|---|---|---|---|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | | |
| 1 MHz | 1 | 0 | 0 | 0 | 0 | 0 | 0 | @ | A5U8, U2, U3; A20U6, U14, U1. |
| 1 MHz | 1 | 0 | 0 | 0 | 0 | 0 | 1 | A | A5U8, U2, U3; A20U6, U14, U1. |
| 100 kHz | 1 | 0 | 0 | 0 | 0 | 1 | 0 | B | A5U8, U3; A20U1. |
| 10 kHz | 1 | 0 | 0 | 0 | 0 | 1 | 1 | C | A5U8, U3; A20U1. |
| 1 kHz | 1 | 0 | 0 | 0 | 1 | 0 | 0 | D | A5U8, U2; A20U2. |
| 100 Hz | 1 | 0 | 0 | 0 | 1 | 0 | 1 | E | A5U8, U2, U3; A20U2. |
| 10 Hz | 1 | 0 | 0 | 0 | 1 | 1 | 0 | F | A5U8, U3; A20U1, U2. |
| 1 Hz | 1 | 0 | 0 | 0 | 1 | 1 | 1 | G | A5U8, U2, U3; A20U1. |
| WIDE | 1 | 0 | 0 | 1 | 0 | 0 | 0 | H | A5U12, U5, U9, U11; A20U2. |
| NORMAL | 1 | 0 | 0 | 1 | 0 | 0 | 1 | I | A5U12, U5, U9, U11; A20U1, U2. |
| LOW | 1 | 0 | 0 | 1 | 0 | 1 | 0 | J | A5U12, U5, U9, U11; A20U1, U2. |
| TEST | 1 | 0 | 0 | 1 | 0 | 1 | 1 | K | A5U12, U5, U9, U11; A20U1, U2. |
| HOLD | 1 | 0 | 0 | 1 | 1 | 0 | 0 | L | A7U8, U2, U3. |
| RECYCLE | 1 | 0 | 0 | 1 | 1 | 0 | 1 | M | A5U2, U5, U13; A20U1, U2;<br>A21U1, U2, U3, U4, Q1, Q2. |
| SAMPLE | 1 | 0 | 0 | 1 | 1 | 1 | 0 | N | A5U10, U13; A20U1, U2;<br>A21U1, U2, U3, U4, Q1, Q2. |
| RESET | 1 | 0 | 0 | 1 | 1 | 1 | 1 | O | A5U10, U13; A20U1, U2. |

SD 055123

SD P/N 055123

| PROGRAMMED INPUTS | | | | | PROGRAMMED OUTPUTS | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| E | D | C | B | A | Y8 | Y7 | Y6 | Y5 | Y4 | Y3 | Y2 | Y1 |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 |
| 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 |
| 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 |
| 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 |
| 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 |
| 0 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 |
| 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 |
| 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |


VCC 16
EN 15
E 14
D 13
C 12
B 11
A 10
Y8 9
EN
E
D
C
B
A
Y1
Y8
Y2
Y3
Y4
Y5
Y6
Y7
1 Y1
2 Y2
3 Y3
4 Y4
5 Y5
6 Y6
7 Y7
8 GND



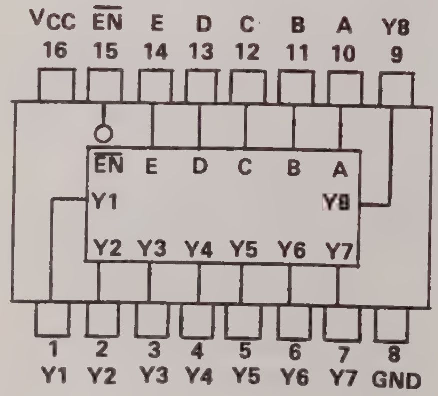
1/8 Dia. minimum yellow paint dot to indicate programmed IC to this specification.

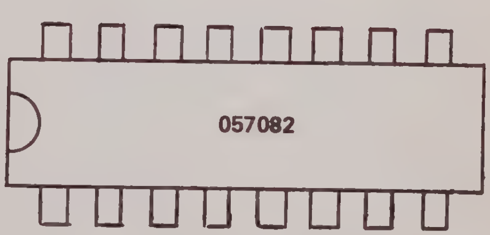
FIGURE 5-36 PROGRAMMED READ ONLY MEMORY (A12U4)

SD 057082

SD P/N 057082

| PROGRAMMED INPUTS | | | | | PROGRAMMED OUTPUTS | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| E | D | C | B | A | Y8 | Y7 | Y6 | Y5 | Y4 | Y3 | Y2 | Y1 |
| 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |


VCC 16
EN 15
E 14
D 13
C 12
B 11
A 10
Y8 9
EN
E
D
C
B
A
Y1
Y8
Y2
Y3
Y4
Y5
Y6
Y7
1 Y1
2 Y2
3 Y3
4 Y4
5 Y5
6 Y6
7 Y7
8 GND



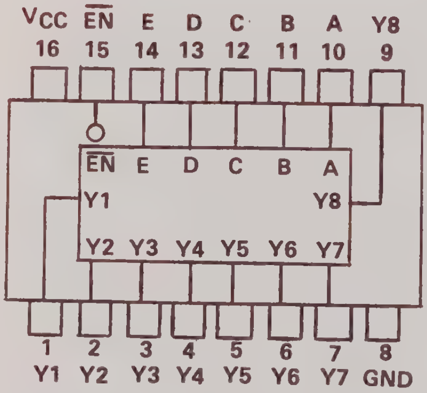
#057082 marked in white ink to indicate programmed IC to this specifications.

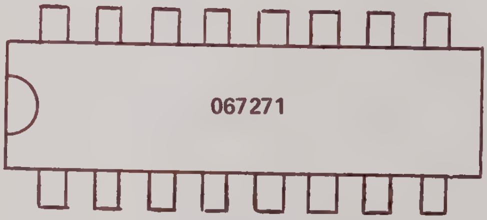
FIGURE 5-37 PROGRAMMED READ ONLY MEMORY (A2U2)

SD 067271

SD P/N 067271

| PROGRAMMED INPUTS | | | | | PROGRAMMED OUTPUTS | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| E | D | C | B | A | Y8 | Y7 | Y6 | Y5 | Y4 | Y3 | Y2 | Y1 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 |


VCC 16
$\overline{EN}$ 15
E 14
D 13
C 12
B 11
A 10
Y8 9
$\overline{EN}$ E D C B A
Y1
Y8
Y2 Y3 Y4 Y5 Y6 Y7
1 Y1
2 Y2
3 Y3
4 Y4
5 Y5
6 Y6
7 Y7
8 GND



#067271 marked in white ink to indicate programmed IC to this specification.

FIGURE 5-38 PROGRAMMED READ ONLY MEMORY (A12U7)

**LM301AH** **S-D P/N 025745**

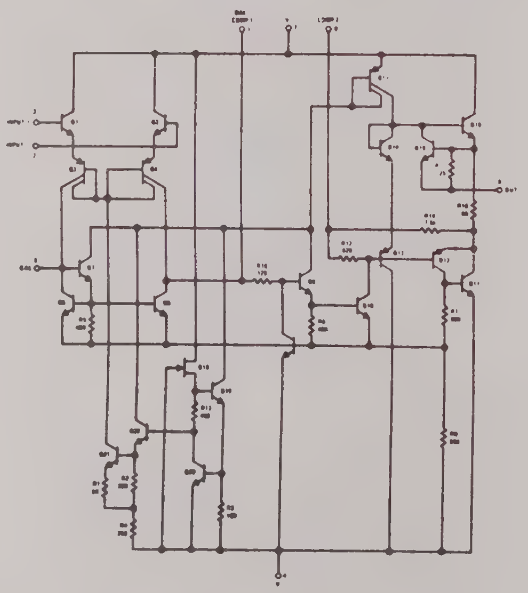
## general description

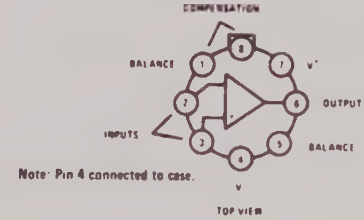
The LM301A is a general-purpose operational amplifier which features improved performance over the 709C and other popular amplifiers. Advanced processing techniques make possible an order of magnitude reduction in input currents, and a redesign of the biasing circuitry reduces the temperature drift of input current.

This amplifier offers many features which make its application nearly foolproof: overload protection on the input and output, no latch-up when the common mode range is exceeded, freedom from oscillations and compensation with a single 30 pF capacitor. It has advantages over internally compensated amplifiers in that the compensation can be tailored to the particular application. For example, as a summing amplifier, slew rates of 10 V/μs and bandwidths of 10 MHz can be realized. In addition, the circuit can be used as a comparator with differential inputs up to ±30V; and the output can be clamped at any desired level to make it compatible with logic circuits.

The LM301A provides better accuracy and lower noise than its predecessors in high impedance circuitry. The low input currents also make it particularly well suited for long interval integrators or timers, sample and hold circuits and low frequency waveform generators. Further, replacing circuits where matched transistor pairs buffer the inputs of conventional IC op amps, it can give lower offset voltage and drift at reduced cost.

## schematic** and connection diagrams





Note: Pin 4 connected to case.

**LM302H**

**S-D P/N 025721**

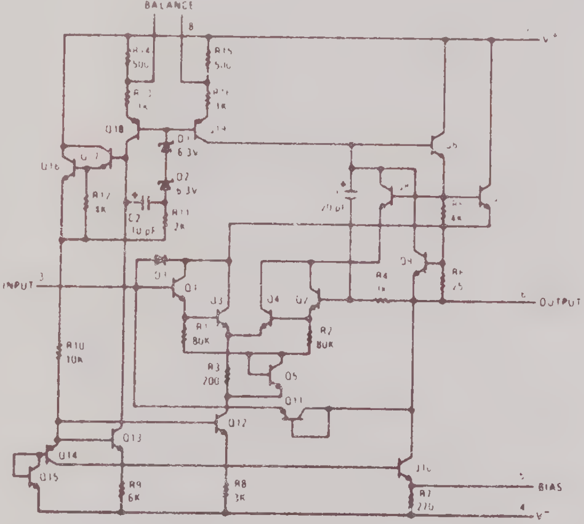
## general description

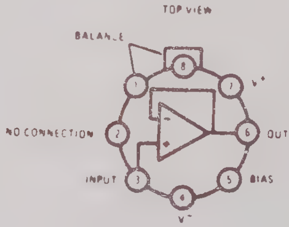
The LM302 is a high gain operational amplifier designed specifically for unity-gain voltage follower applications. Built on a single silicon chip, the device incorporates advanced processing techniques to obtain very low input current and high input impedance. Further, the input transistors are operated at zero collector-base voltage to virtually eliminate high temperature leakage currents. It can therefore be operated in a temperature stabilized component over to get extremely low input currents and low offset voltage drift. Other outstanding characteristics of the device include:

- Fast Slewing – 10V/μs
- Low input current – 30 nA (max)
- High input resistance – 1,000 MΩ
- No external frequency compensation required
- Simple offset balancing with optional 1K potentiometer
- Specified for operation from 0°C to 70°C
- Plug-in replacement for both the LM201 and LM709C in voltage follower applications.

The LM302, which is designed to operate with supply voltages between ±12V and ±15V, also features low input capacitance as well as excellent small signal and large signal frequency response – all of which minimize high frequency gain error. Because of the low wiring capacitances inherent in monolithic construction, this fast operation can be realized without increasing power consumption.

## schematic and connection diagrams


BALANCE
8
V+
R14 500
R15 500
R12 1K
R11 1K
Q18
Q16
Q17
D1 6.3V
D2 6.3V
R17 3K
C2 10 pF
R13 2K
30 pF
R5 4K
R6 25
R4 1k
INPUT
3
OUTPUT
6
R1 80K
R2 80K
R3 200
R10 10K
Q13
Q14
Q15
Q12
Q11
R9 6K
R8 3K
R7 270
BIAS
5
4
V−


TOP VIEW
BALANCE
1
8
7
V+
NO CONNECTION
2
6
OUTPUT
INPUT
3
5
BIAS
4
V−

Note: Pin 4 connected to case.

**LM309K** **S-D P/N 025787**

## general description

The LM309 is a complete 5V regulator fabricated on a single silicon chip. It is designed for local regulation on digital logic cards, eliminating the distribution problems associated with single-point regulation. The device is available in two common transistor packages. In the solid-kovar TO-5 header, it can deliver output currents in excess of 200 mA, if adequate heat sinking is provided. With the TO-3 power package, the available output current is greater than 1A.

The regulator is essentially blow-out proof. Current limiting is included to limit the peak output current to a safe value. In addition, thermal shutdown is provided to keep the IC from overheating. If internal dissipation becomes too great, the regulator will shut down to prevent excessive heating.

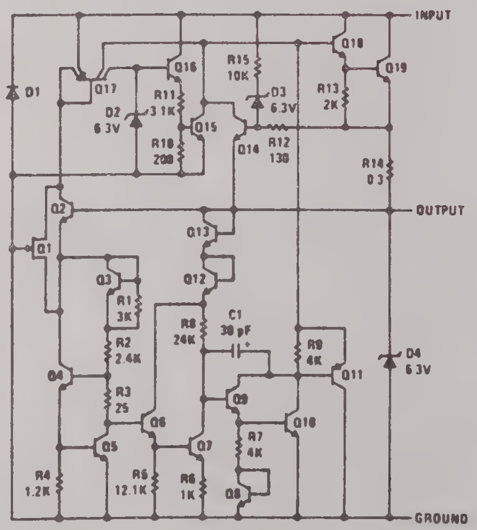
Considerable effort was expended to make the LM309 easy to use and minimize the number of external components. It is not necessary to bypass the output, although this does improve transient response somewhat. Input bypassing is needed, however, if the regulator is located very far from the filter capacitor of the power supply. Stability is also achieved by methods that provide very good rejection of load or line transients as are usually seen with TTL logic.

Although designed primarily as a fixed-voltage regulator, the output of the LM309 can be set to voltages above 5V, as shown below. It is also possible to use the circuit as the control element in precision regulators, taking advantage of the good current-handling capability and the thermal overload protection.

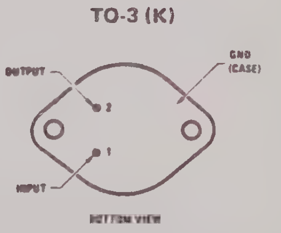
To summarize, outstanding features of the regulator are:

- Specified to be compatible, worst case, with TTL and DTL
- Output current in excess of 1A
- Internal thermal overload protection
- No external components required

## schematic diagram


INPUT
OUTPUT
GROUND
D1
Q17
D2
6.3V
R11
3.1K
Q16
R10
200
Q15
R15
10K
D3
6.3V
Q14
R12
130
R13
2K
Q18
Q19
R14
0.3
Q2
Q1
Q13
Q12
Q3
R1
3K
R2
2.4K
Q4
R3
25
Q5
Q6
Q7
R4
1.2K
R5
12.1K
R6
1K
R8
24K
C1
30 pF
Q9
Q10
R7
4K
Q8
R9
4K
Q11
D4
6.3V

## connection diagram


TO-3 (K)
OUTPUT
GND
(CASE)
2
1
INPUT
BOTTOM VIEW

**LM320K5.2** **S-D P/N 103064**

## general description

The LM120 Series are three-terminal negative regulators with a fixed output voltage of –5V, –5.2V, –12V, and –15V and up to 1.5A load current capability. These devices need only one external component – a compensation capacitor at the output, making them easy to apply. Worst case guarantees on output voltage deviation due to any combination of line, load or temperature variation assure satisfactory system operation.

Exceptional effort has been made to make the LM120 Series immune to overload conditions. The regulators have current limiting which is independent of temperature, combined with thermal overload protection. Internal current limiting protects against momentary faults while thermal shutdown prevents junction temperatures from exceeding safe limits during prolonged overloads.

Although primarily intended for fixed output voltage applications, the LM120 Series may be programmed for higher output voltages with a simple resistive divider. The low quiescent drain current of the devices allows this technique to be used with good regulation.

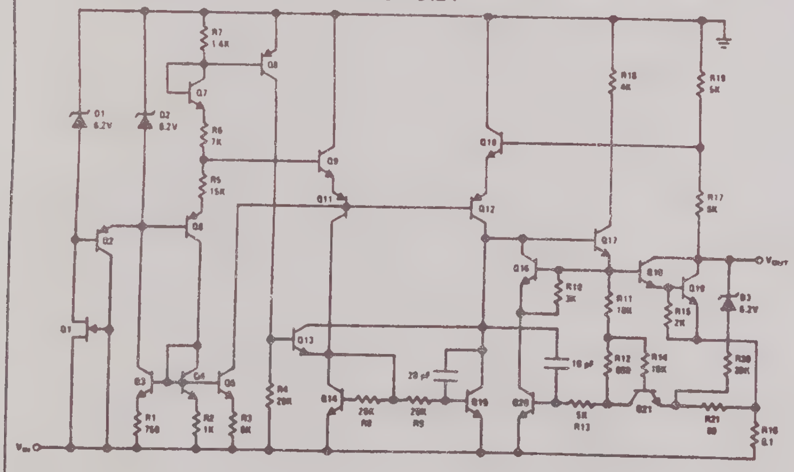
The LM120 Series is available in TO-5 and TO-3 packages. The TO-5 is rated at 200 mA and 2W; the TO-3 at 1A and 20W.

## features

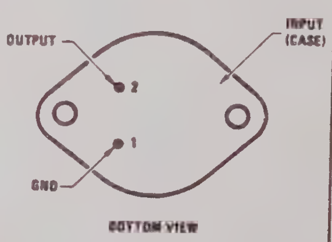
- Preset output voltage error less than ±3%
- Preset current limit
- Internal thermal shutdown
- Operates with input-output voltage differential down to 1V
- Excellent ripple rejection
- 50 mV load regulation

## schematic and connection diagrams

–5V & –5.2V


R7 1.4K
Q8
Q7
D1 6.2V
D2 6.2V
R6 7K
Q9
R5 15K
Q11
Q10
Q12
R18 4K
R19 5K
R17 5K
Q6
Q2
Q17
Q16
Q18
Q19
VOUT
R10 3K
R11 10K
R15 2K
D3 6.2V
Q1
Q13
Q3
Q4
Q5
R4 20K
Q14
20K R8
20K R9
20 pF
Q15
Q20
10 pF
5K R13
R12
R14
Q21
R20
R21
R16 0.1
R1 750
R2 1K
R3 6K
VIN

TO-3 (K)


OUTPUT
INPUT (CASE)
2
1
GND
BOTTOM VIEW

# LINEAR BALANCED MODULATOR/DEMODULATOR

MC1495L

S-D P/N 106624

# MC1595L
# MC1495L

## WIDEBAND MONOLITHIC FOUR-QUADRANT MULTIPLIER

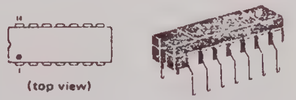
. . . designed for uses where the output is a linear product of two input voltages. Maximum versatility is assured by allowing the user to select the level shift method. Typical applications include: multiply, divide*, square root*, mean square*, phase detector, frequency doubler, balanced modulator/demodulator, electronic gain-control.

*When used with an operational amplifier.

- Wide Bandwidth
- Excellent Linearity – 1% max Error on X-Input, 2% max Error on Y-Input – MC1595L
- Excellent Linearity – 2% max Error on X-Input, 4% max Error on Y-Input – MC1495L
- Adjustable Scale Factor, K
- Excellent Temperature Stability
- Wide Input Voltage Range – ± 10 Volts
- ± 15 Volt Operation

**LINEAR FOUR-QUADRANT MULTIPLIER INTEGRATED CIRCUIT**

**MONOLITHIC SILICON EPITAXIAL PASSIVATED**


14
1
(top view)

CERAMIC PACKAGE
CASE 632
TO-116

FIGURE 1 – FOUR-QUADRANT MULTIPLIER TRANSFER CHARACTERISTIC

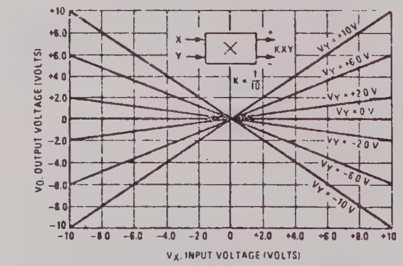


FIGURE 2 – TRANSCONDUCTANCE BANDWIDTH

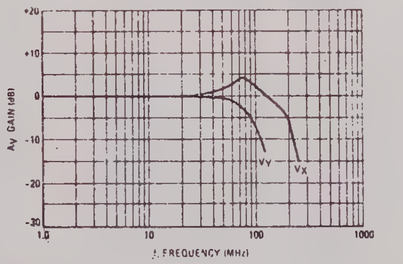
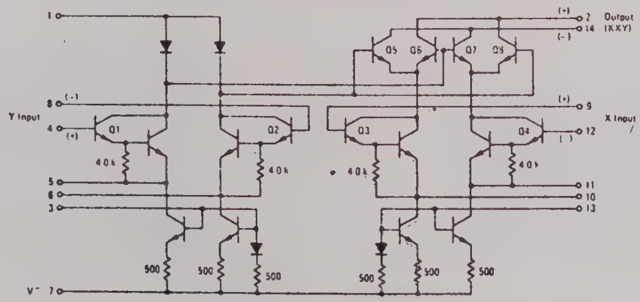


FIGURE 3 – CIRCUIT SCHEMATIC


1
(+)
2 Output
14 (KXY)
(-)
Q5 Q6 Q7 Q8
8 (-)
Y Input
4 (+)
Q1
Q2
Q3
Q4
(+) 9
X Input
12 (-)
40 k
40 k
40 k
40 k
5
6
3
11
10
13
500
500
500
500
500
500
V- 7

# LINEAR BALANCED MODULATOR/DEMODULATOR

# MC1596
# MC1496

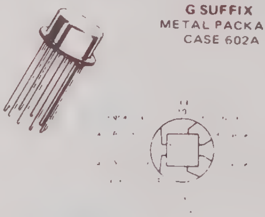
## BALANCED MODULATOR – DEMODULATOR

. . . designed for use where the output voltage is a product of an input voltage (signal) and a switching function (carrier). Typical applications include suppressed carrier and amplitude modulation, synchronous detection, FM detection, phase detection, and chopper applications. See Motorola Application Note AN-531 for additional design information.

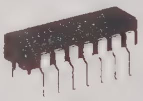
- Excellent Carrier Suppression – 65 dB typ @ 0.5 MHz
  - 50 dB typ @ 10 MHz
- Adjustable Gain and Signal Handling
- Balanced Inputs and Outputs
- High Common-Mode Rejection – 85 dB typ

**BALANCED MODULATOR – DEMODULATOR**

**SILICON MONOLITHIC INTEGRATED CIRCUIT**

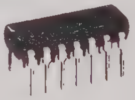


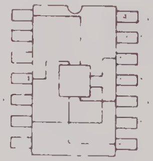
**G SUFFIX**
METAL PACKAGE
CASE 602A



**L SUFFIX**
CERAMIC PACKAGE
CASE 632
TO 116

**P SUFFIX**
PLASTIC PACKAGE
CASE 646
(MC1496 only)





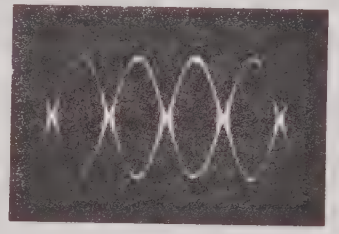


FIGURE 1
SUPPRESSED CARRIER
OUTPUT WAVEFORM

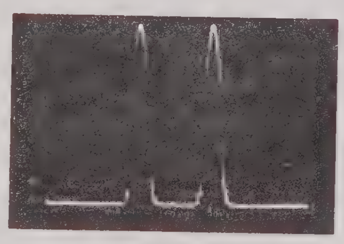


FIGURE 2
SUPPRESSED-CARRIER
SPECTRUM

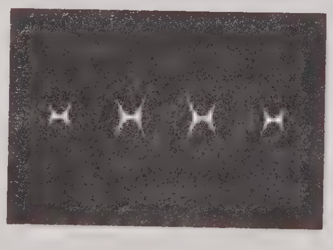
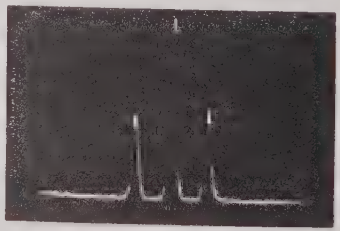


FIGURE 3 –
AMPLITUDE-MODULATION
OUTPUT WAVEFORM

FIGURE 4   AMPLITUDE MODULATION SPECTRUM



# MC1590G

## RF/IF/AUDIO AMPLIFIER

. . . an integrated circuit featuring wide-range AGC for use in RF/IF amplifiers and audio amplifiers over the temperature range, -55 to +125°C. See Motorola Application Note AN-513 for design details.

- High Power Gain – 50 dB typ at 10 MHz
  45 dB typ at 60 MHz
  35 dB typ at 100 MHz
- Wide-Range AGC – 60 dB min, dc to 60 MHz
- Low Reverse Transfer Admittance – <10 μmhos typ at 60 MHz
- 6.0 to 15-Volt Operation, Single-Polarity Power Supply

## WIDEBAND AMPLIFIER WITH AGC

SILICON MONOLITHIC
INTEGRATED CIRCUIT

METAL PACKAGE
CASE 601

PIN CONNECTIONS

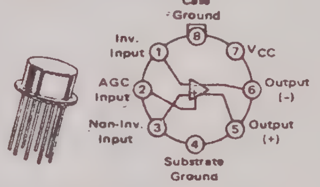

Case Ground
8
Inv. Input
1
7
VCC
AGC Input
2
6
Output (-)
Non-Inv. Input
3
5
Output (+)
4
Substrate Ground

FIGURE 1 – UNNEUTRALIZED POWER GAIN versus FREQUENCY
(Tuned Amplifier, see Figure 16)

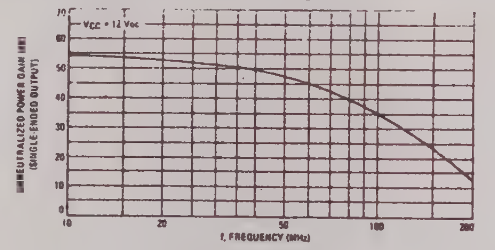
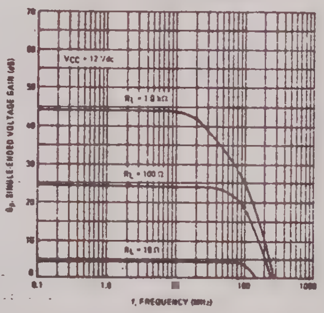
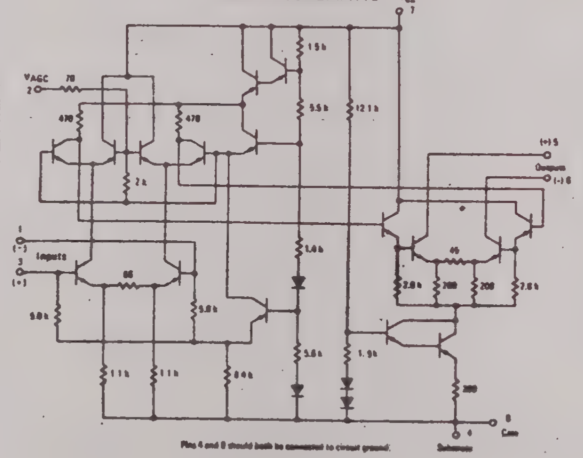


FIGURE 2 – VOLTAGE GAIN versus FREQUENCY
(Video Amplifier, see Figure 17)

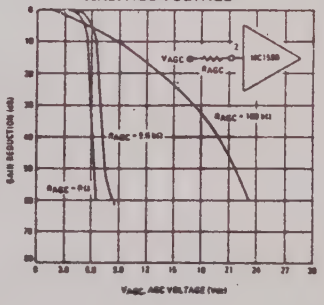


CIRCUIT SCHEMATIC


VCC
7
VAGC
2
70
470
470
1.5 k
5.5 k
12 k
2 k
(+) 5
Outputs
(-) 6
1
(-)
Inputs
3
(+)
68
9.8 k
9.8 k
1.6 k
46
2.8 k
200
200
2.8 k
5.6 k
1.9 k
1.1 k
1.1 k
8.4 k
200
8
Case
4
Substrate

Pins 4 and 8 should both be connected to circuit ground.

FIGURE 3 – TYPICAL GAIN REDUCTION versus AGC VOLTAGE



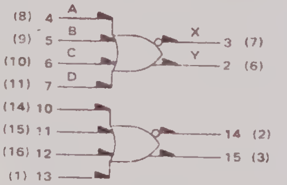
# ECL DUAL 4-INPUT OR/NOR OR AND/NAND GATE

MC1660L

S-D P/N 025777

MC1660 provides simultaneous OR-NOR or AND-NAND output functions with the capability of driving 50-ohm lines. These devices contain an internal bias reference voltage insuring that the threshold point is always in the center of the transition region over the temperature range (-30° to +85°C). The input pulldown resistors eliminate the need to tie unused inputs to $V_{EE}$.

POSITIVE LOGIC

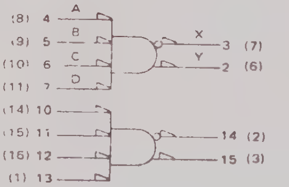


(8) 4
(9) 5
(10) 6
(11) 7
A
B
C
D
X
Y
3 (7)
2 (6)
(14) 10
(15) 11
(16) 12
(1) 13
14 (2)
15 (3)

$X = \overline{A + B + C + D}$

$Y = A + B + C + D$

NEGATIVE LOGIC



(8) 4
(9) 5
(10) 6
(11) 7
A
B
C
D
X
Y
3 (7)
2 (6)
(14) 10
(15) 11
(16) 12
(1) 13
14 (2)
15 (3)

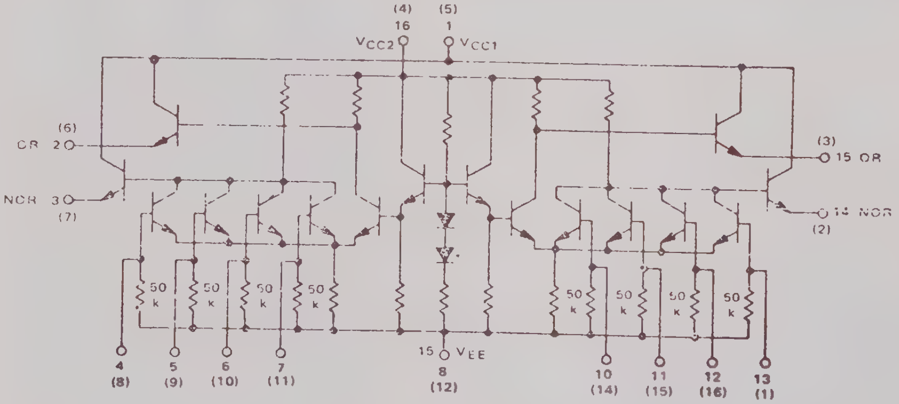
$X = \overline{A} \bullet \overline{B} \bullet \overline{C} \bullet \overline{D}$

$Y = A \bullet B \bullet C \bullet D$

$t_{pd}$ = 0.9 ns typ (510-ohm load)
= 1.1 ns typ ( 50 ohm load)
$P_D$ = 120 mW typ/pkg (No load)
Full Load Current, $I_L$ = -25 mAdc max

Numbers at ends of terminals denote pin numbers for L package (Case 620).
Numbers in parenthesis denote pin numbers for F package (Case 650).

CIRCUIT SCHEMATIC



(4)
16
VCC2
(5)
1
VCC1
(6)
OR 2
NOR 3
(7)
(3)
15 OR
14 NOR
(2)
50 k
50 k
50 k
50 k
50 k
50 k
50 k
50 k
15 VEE
8
(12)
4
(8)
5
(9)
6
(10)
7
(11)
10
(14)
11
(15)
12
(16)
13
(1)

Numbers at ends of terminals denote pin numbers for L package (Case 620).
Numbers in parenthesis denote pin numbers for F package (Case 650).

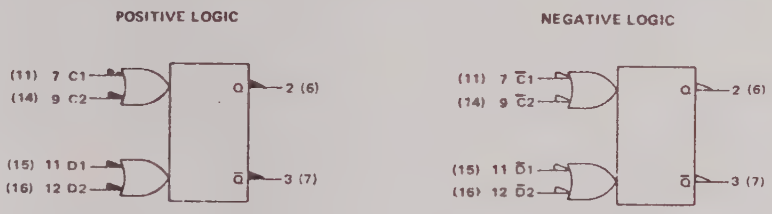
# ECL UHF PRESCALER TYPE D FLIP-FLOP

**MC1690L** S-D P/N 103182

$P_D$ = 200 mW typ/pkg (No Load)
$f_{tog}$ = 500 MHz min

The MC1690 is a high speed D master-slave flip-flop capable of toggle rates over 500 MHz. Designed primarily for high speed prescaling applications in communications and instrumentation, this device employs two data inputs, two clock inputs and complementary Q and Q̄ outputs. It is a higher frequency replacement for the MC1670 (350 MHz) D flip-flop. There are no set or reset inputs and an extra data input is provided.

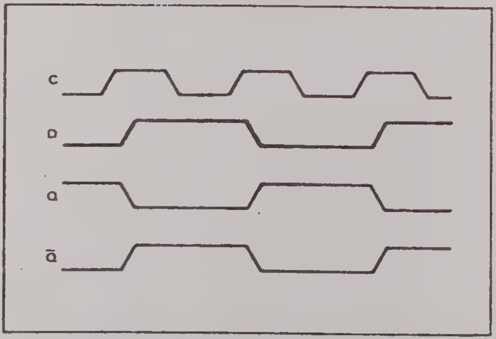
When used with the MC1678, the MC1690 provides a decade counter capable of 500 MHz operation.


POSITIVE LOGIC
(11) 7 C1
(14) 9 C2
(15) 11 D1
(16) 12 D2
Q
Q̄
2 (6)
3 (7)
NEGATIVE LOGIC
(11) 7 C̄1
(14) 9 C̄2
(15) 11 D̄1
(16) 12 D̄2
Q
Q̄
2 (6)
3 (7)

$V_{CC1}$ = Pin 1 (5)
$V_{CC2}$ = Pin 16 (4)
$V_{EE}$ = Pin 8 (12)

Numbers at ends of terminals denote pin numbers for L package (Case 620).
Numbers in parenthesis denote pin numbers for F package (Case 650).

TIMING DIAGRAM



**TRUTH TABLE**

| C | D | $Q_{n+1}$ |
|---|---|---|
| L | φ | $Q_n$ |
| H | φ | $Q_n$ |
| ↑ | L | L |
| ↑ | H | H |

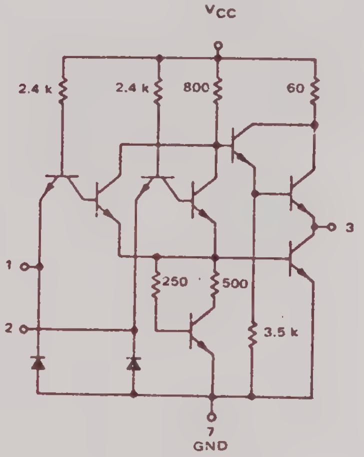
C = C1 + C2
D = D1 + D2
φ = Don't Care

## TTL QUAD 2-INPUT NOR GATE

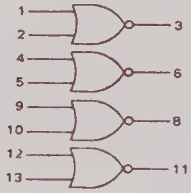
MC3002P

S-D P/N 025739

1/4 OF CIRCUIT SHOWN


VCC
2.4 k
2.4 k
800
60
3
1
2
250
500
3.5 k
7
GND

This device consists of four 2-input NOR gates. Each gate may be used as an inverter, or two gates may be cross-coupled to form bistable circuits.


1
2
3
4
5
6
9
10
8
12
13
11

Positive Logic: $3 = \overline{1 + 2}$

Negative Logic: $3 = \overline{1 \bullet 2}$

Input Loading Factor = 1

Output Loading Factor = 10

Total Power Dissipation = 122 mW typ/pkg

Propagation Delay Time = 5.0 ns typ

## TTL QUAD 2-INPUT OR GATE

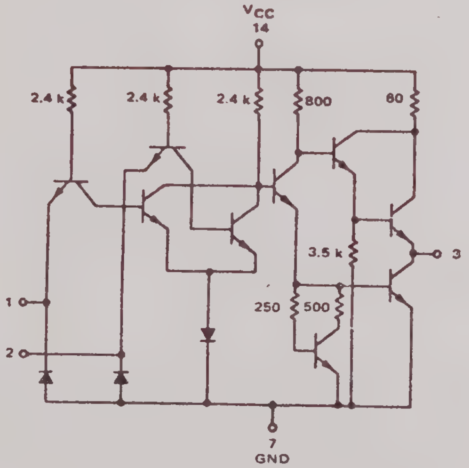
MC3003P

S-D P/N 025767

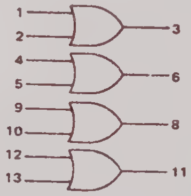
**MC3103F • MC3003F**

**MC3103L • MC3003L,P**

1/4 OF CIRCUIT SHOWN


VCC
14
2.4 k
2.4 k
2.4 k
800
60
3.5 k
3
1
2
250
500
7
GND

This device consists of four 2-input OR gates. This non-inverting function is useful for optimizing logic design, or for direct implementation of standard logic equations.


1
2
3
4
5
6
9
10
8
12
13
11

Positive Logic: $3 = 1 + 2$

Negative Logic: $3 = 1 \cdot 2$

Input Loading Factor = 1

Output Loading Factor = 10

Total Power Dissipation = 150 mW typ/pkg

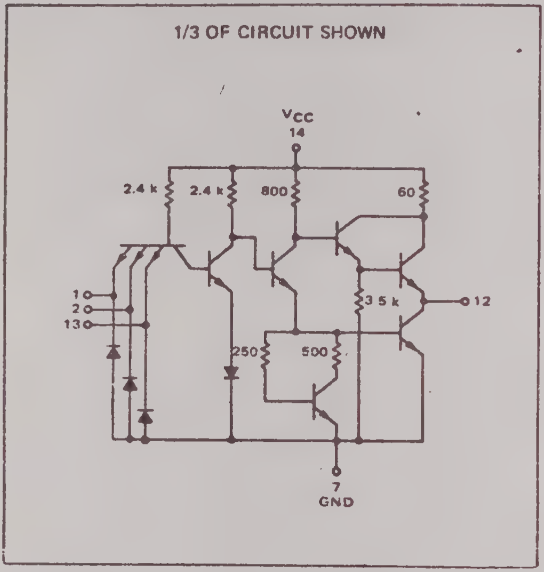
Propagation Delay Time = 9.0 ns typ

## TTL TRIPLE 3-INPUT AND GATE

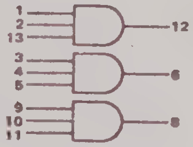
MC3006P

S-D P/N 045219

**MC3106F • MC3006F**
**MC3106L • MC3006L,P**
**(54H11J) (74H11J,N)**


1/3 OF CIRCUIT SHOWN
VCC
14
2.4 k
2.4 k
800
60
3.5 k
250
500
1
2
13
12
7
GND

This device consists of three 3-input AND gates. This non-inverting function is useful for optimizing logic design, or for direct implementation of standard logic equations.


1
2
13
12
3
4
5
6
9
10
11
8

Positive Logic: $12 = 1 \cdot 2 \cdot 13$
Negative Logic: $12 = 1 + 2 + 13$

Input Loading Factor = 1
Output Loading Factor = 10

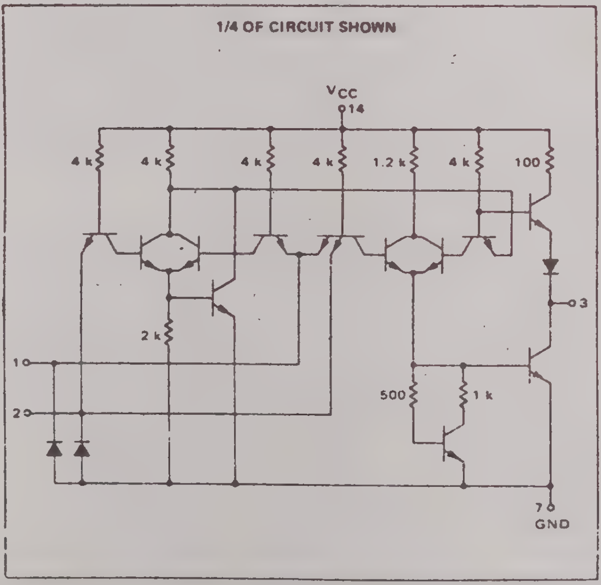
Total Power Dissipation = 84 mW typ/pkg
Propagation Delay Time = 9.0 ns typ

## TTL QUAD 2-INPUT EXCLUSIVE OR GATE

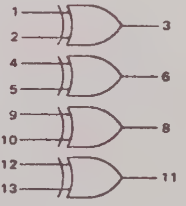
MC3021P

S-D P/N 025789

**MC3121F • MC3021F**
**MC3121L • MC3021L,P**


1/4 OF CIRCUIT SHOWN
VCC
14
4 k
4 k
4 k
4 k
1.2 k
4 k
100
2 k
500
1 k
1
2
3
7
GND

This device consists of four 2-input Exclusive OR gates. They can be used to build parity checking/generating functions. Up/down counters can be built using these gates and J-K flip-flops.


1
2
3
4
5
6
9
10
8
12
13
11

Positive Logic: $3 = 1 \bullet \overline{2} + \overline{1} \bullet 2$

Input Loading Factor = 1.6
Output Loading Factor = 8
Total Power Dissipation = 100 mW typ/pkg
Propagation Delay Time = 14 ns typ

# TTL QUAD INTERFACE BUS TRANSCEIVER

MC3446P

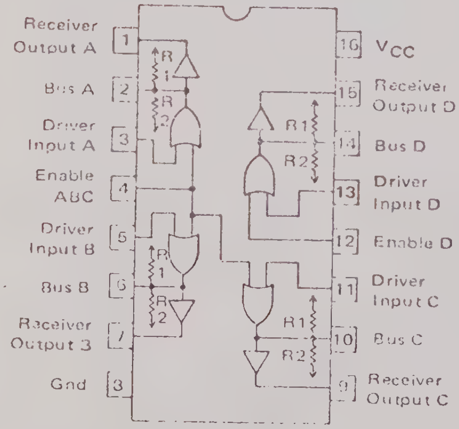
S-D P/N 117021

## QUAD GENERAL PURPOSE INTERFACE BUS (G.P.I.B.) TRANSCEIVER

The MC3446 is a quad bus transceiver intended for usage in instruments and programmable calculators equipped for interconnection into complete measurement systems. This transceiver allows the bidirectional flow of digital data and commands between the various instruments. The transceiver provides four open-collector drivers and four receivers featuring hysteresis.

- Tailored to Meet the IEEE Standard 488-1975 (Digital Interface for Programmable Instrumentation) and the Proposed IEC Standard on Instrument Interface
- Provides Electrical Compatibility with Hewlett Packard Interface Bus. (HPIB)
- MOS Compatible with High Impedance Inputs
- Driver Output Guaranteed Off During Power Up/Power Down
- Low Power – Average Power Supply Current = 12 mA
- Termination Resistors Provided

PIN CONNECTIONS

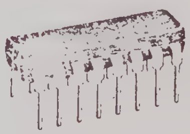


Receiver Output A 1
Bus A 2
Driver Input A 3
Enable ABC 4
Driver Input B 5
Bus B 6
Receiver Output B 7
Gnd 8
16 VCC
15 Receiver Output D
14 Bus D
13 Driver Input D
12 Enable D
11 Driver Input C
10 Bus C
9 Receiver Output C
R1
R2

R1 = 2.4 k
R2 = 5.0 k

### QUAD INTERFACE BUS TRANSCEIVER

SILICON MONOLITHIC INTEGRATED CIRCUIT



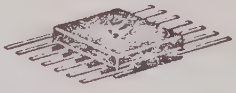
P SUFFIX
PLASTIC PACKAGE
CASE 648

# TTL PHASE/FREQUENCY DETECTOR

MC4044P

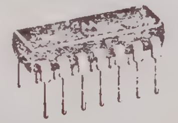
S-D P/N 045238

The MC4344/4044 consists of two digital phase detectors, a charge pump, and an amplifier. In combination with a voltage controlled multivibrator (such as the MC4324/4024 or MC1648), it is useful in a broad range of phase-locked loop applications. The circuit accepts MTTL waveforms at the R and V inputs and generates an error voltage that is proportional to the frequency and/or phase difference of the input signals. Phase detector #1 is intended for use in systems requiring zero frequency and phase difference at lock. Phase detector #2 is used if quadrature lock is desired. Phase detector #2 can also be used to indicate that the main loop, utilizing phase detector #1, is out of lock.

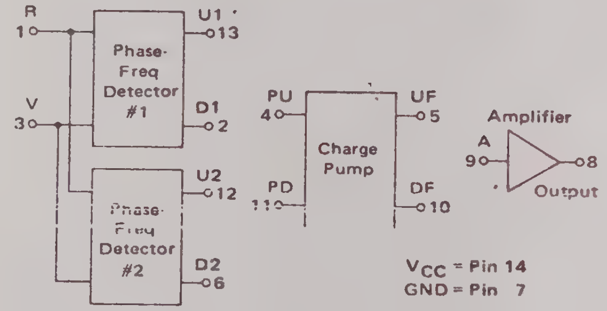


F SUFFIX
CERAMIC PACKAGE
CASE 607
(TO 86)

L SUFFIX
CERAMIC PACKAGE
CASE 632
(TO-116)



P SUFFIX
PLASTIC PACKAGE
CASE 646
(TO-116)
MC4044 only


R
1
U1
13
Phase-Freq Detector #1
V
3
D1
2
U2
12
Phase-Freq Detector #2
D2
6
PU
4
UF
5
Charge Pump
PD
11
DF
10
Amplifier
A
9
8
Output

VCC = Pin 14
GND = Pin 7

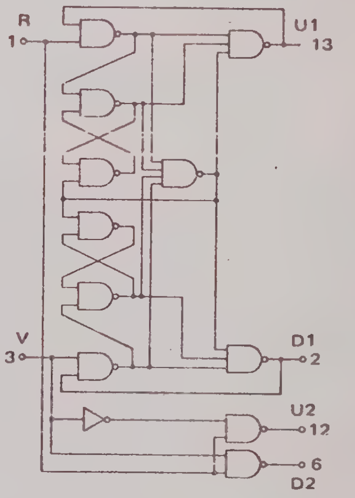
Input Loading Factor: R, V = 3

Output Loading Factor (Pin 8) = 10

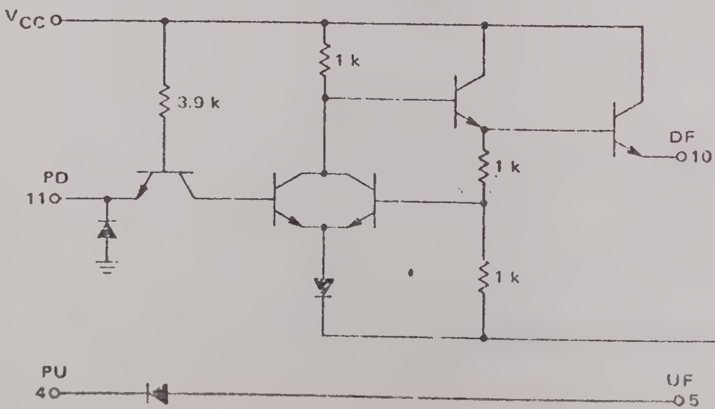
Total Power Dissipation = 85 mW typ/pkg

Propagation Delay Time = 9.0 ns typ
(thru phase detector)

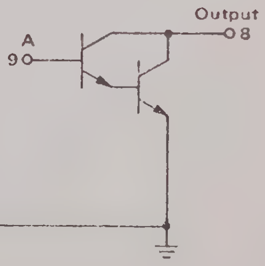
## PHASE DETECTOR


R
1
U1
13
V
3
D1
2
U2
12
6
D2

## CHARGE PUMP


VCC
3.9 k
1 k
1 k
1 k
PD
11
DF
10
PU
4
UF
5

## AMPLIFIER



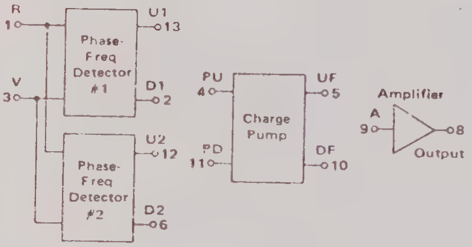
| INPUT STATE | INPUT | | OUTPUT | | | |
|---|---|---|---|---|---|---|
| | RI | VI | U1 | D1 | U2 | D2 |
| 1 | 0 | 0 | X | X | 1 | 1 |
| 2 | 1 | 0 | X | X | 0 | 1 |
| 3 | 1 | 1 | X | X | 1 | 0 |
| 4 | 1 | 0 | X | X | 0 | 1 |
| 5 | 0 | 0 | X | X | 1 | 1 |
| 6 | 1 | 0 | X | X | 0 | 1 |
| 7 | 0 | 0 | X | X | 1 | 1 |
| 8 | 1 | 0 | X | X | 0 | 1 |
| 9 | 0 | 0 | 0 | 1 | 1 | 1 |
| 10 | 0 | 1 | 0 | 1 | 1 | 1 |
| 11 | 0 | 0 | 1 | 1 | 1 | 1 |
| 12 | 0 | 1 | ✓1 | 1 | 1 | 1 |
| 13 | 0 | 0 | 1 | 0 | 1 | 1 |
| 14 | 0 | 1 | 1 | 0 | 1 | 1 |
| 15 | 0 | 0 | 1 | 0 | 1 | 1 |
| 16 | 1 | 0 | 1 | 0 | 0 | 1 |
| 17 | 0 | 0 | ✓1 | 1 | 1 | 1 |

### TRUTH TABLE

This is not strictly a functional truth table; i.e., it does not show all possible modes of operation. It is useful for dc testing.

1. X indicates output state unknown.
2. U1 and D1 outputs are sequential; i.e., they must be sequenced in order shown.
3. U2 and D2 outputs are combinational; i.e., they need only inputs shown to obtain outputs.

## ELECTRICAL CHARACTERISTICS

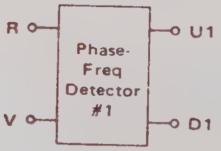


## OPERATING CHARACTERISTICS

Operation of the MC4344/4044 is best explained by initially considering each section separately. If phase detector #1 is used, loop lockup occurs when both outputs U1 and D1 remain high. This occurs only when all the negative transitions on R, the reference input, and V, the variable or feedback input, coincide. The circuit responds only to transitions, hence phase error is independent of input waveform duty cycle or amplitude variation. Phase detector #1 consists of sequential logic circuitry, therefore operation prior to lockup is determined by initial conditions.

When operation is initiated, by either applying power to the circuit or active input signals to R and V, the circuitry can be in one of several states. Given any particular starting conditions, the flow table of Figure 1 can be used to determine subsequent operation. The flow table indicates the status of U1 and D1 as the R and V inputs are varied. The numbers in the table which are in parentheses are arbitrarily assigned labels that correspond to stable states that can result for each input combination. The numbers without parentheses refer to unstable conditions. Input changes are traced by horizontal movement in the table; after each input change, circuit operation will settle in the numbered state indicated by moving horizontally to the appropriate R-V column. If the number at that

FIGURE 1 – PHASE DETECTOR #1 FLOW TABLE



| R-V | R-V | R-V | R-V | U1 | D1 |
|---|---|---|---|---|---|
| 0-0 | 0-1 | 1-1 | 1-0 | | |
| (1) | 2 | 3 | (4) | 0 | 1 |
| 5 | (2) | (3) | 8 | 0 | 1 |
| (5) | 6 | 7 | 8 | 1 | 1 |
| 9 | (6) | 7 | 12 | 1 | 1 |
| 5 | 2 | (7) | 12 | 1 | 1 |
| 1 | 2 | 7 | (8) | 1 | 1 |
| (9) | (10) | 11 | 12 | 1 | 0 |
| 5 | 6 | (11) | (12) | 1 | 0 |

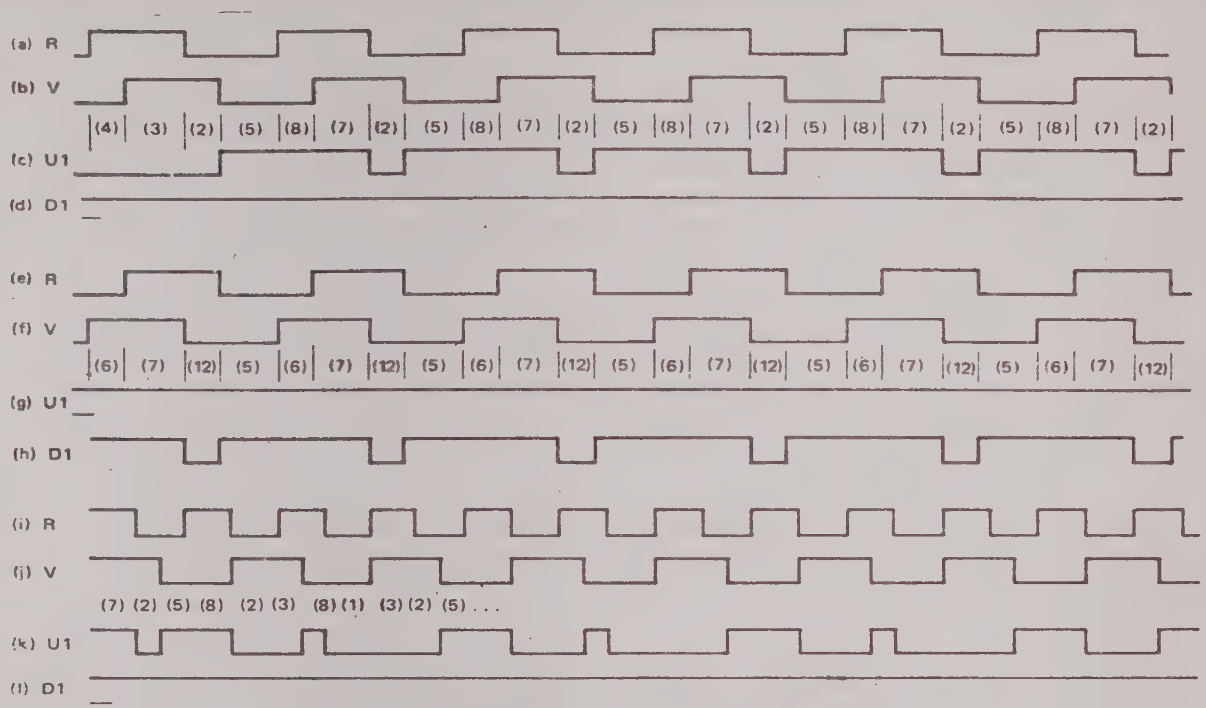


FIGURE 2 – PHASE DETECTOR #1 TIMING DIAGRAM

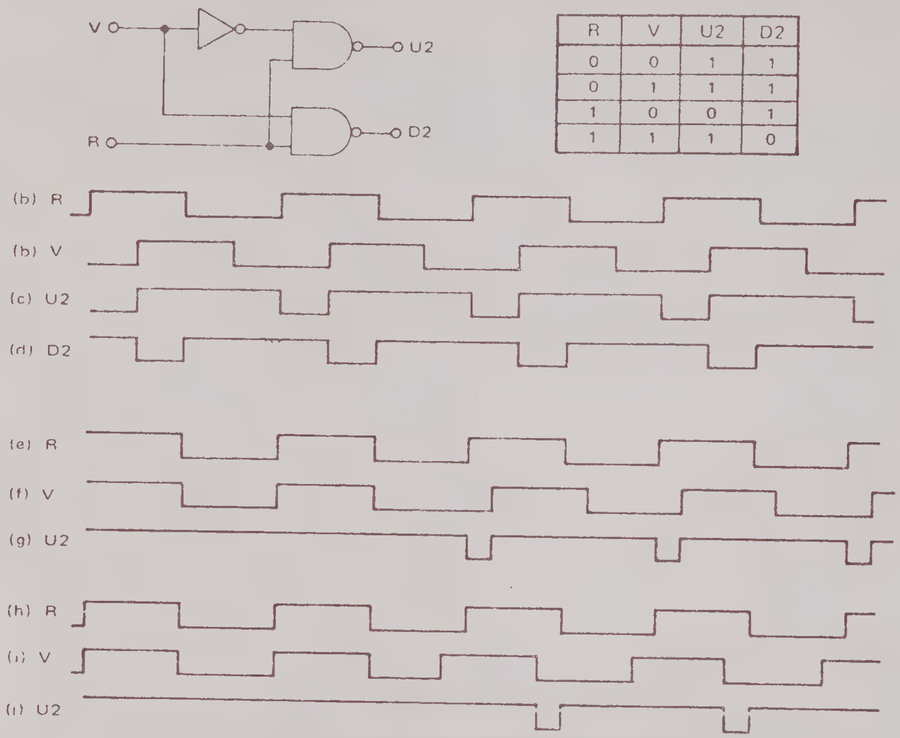
location is not in parentheses, move vertically to the number of the same value that is in parentheses. For a given input pair, any one of three stable states can exist. As an example, if R = 1 and V = 0, the circuit will be in one of the stable states (4), (8), or (12).

Use of the table in determining circuit operation is illustrated in Figure 2. In the timing diagram, the input to R is the reference frequency; the input to V is the same frequency but lags in phase. Stable state (4) is arbitrarily assumed as the initial condition. From the timing diagram and flow table, when the circuit is in stable state (4), outputs U1 and D1 are "0" and "1" respectively. The next input state is R-V = 1-1; moving horizontally from stable state (4) under R-V = 1-0 to the R-V = 1-1 column, state 3 is indicated. However, this is an unstable condition and the circuit will assume the state indicated by moving vertically in the R-V = 1-1 column to stable state (3). In this instance, outputs U1 and D1 remain unchanged. The input states next become R-V = 0-1; moving horizontally to the R-V = 0-1 column, stable state (2) is indicated. At this point there is still no change in U1 or D1. The next input change shifts operation to the R-V = 0-0 column where unstable state 5 is indicated. Moving vertically to stable state (5), the outputs now change state to U1-D1 = 1-1. The next input change, R-V = 1-0, drives the circuitry to stable state (8), with no change in U1 or D1. The next input, R-V = 1-1, leads to stable state (7) with no change in the outputs. The next two input state changes cause U1 to go low between the negative transitions of R and V. As the inputs continue to change, the circuitry moves repeatedly through stable states (2), (5), (8), (7), (2), etc. as shown, and a periodic waveform is obtained on the U1 terminal while D1 remains high.

A similar result is obtained if V is leading with respect to R, except that the periodic waveform now appears on D1 as shown in rows e-h of the timing diagram of Figure 2. In each case, the average value of the resulting waveform is proportional to the phase difference between the two inputs. In a closed loop application, the error signal for controlling the VCO is derived by translating and filtering these waveforms.

The results obtained when R and V are separated by a fixed frequency difference are indicated in rows i-l of the timing system. For this case, the U1 output goes low when R goes low and stays in that state until a negative transition on V occurs. The resulting waveform is similar to the fixed phase difference case, but now the duty cycle of the U1 waveform varies at a rate proportional to the difference frequency of the two inputs, R and V. It is this characteristic that permits the MC4344/4044 to be used as a frequency discriminator; if the signal on R has been frequency modulated and if the loop bandwidth is selected to pass the deviation frequency but reject R and V, the resulting error voltage applied to the VCO will be the recovered modulation signal.

Phase detector #2 consists only of combinatorial logic, therefore its characteristics can be determined from the



| R | V | U2 | D2 |
|---|---|---|---|
| 0 | 0 | 1 | 1 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 0 |

FIGURE 3 – PHASE DETECTOR #2 OPERATION

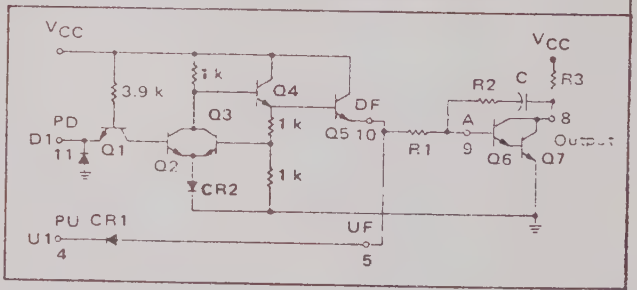
simple truth table of Figure 3. Since circuit operation requires that both inputs to the charge pump either be high or have the same duty cycle when lock occurs, using this phase detector leads to a quadrature relationship between R and V. This is illustrated in rows a-d of the timing diagram of Figure 3. Note that any deviation from a fifty percent duty cycle on the inputs would appear as phase error.

Waveforms showing the operation of phase detector #2 when phase detector #1 is being used in a closed loop are indicated in rows e-j. When the main loop is locked, U2 remains high. If the loop drifts out of lock in either direction a negative pulse whose width is proportional to the amount of drift appears on U2. This can be used to generate a simple loss-of-lock indicator.

Operation of the charge pump is best explained by considering it in conjunction with the Darlington amplifier included in the package (see Figure 4). There will be a pulsed waveform on either PD or PU, depending on the phase-frequency relationship of R and V. The charge pump serves to invert one of the input waveforms (D1) and translates the voltage levels before they are applied to the loop filter. When PD is low and PU is high, Q1 will be conducting in the normal direction and Q2 will be off. Current will be flowing through Q3 and CR2; the base of Q3 will be two $V_{BE}$ drops above ground or approximately 1.5 volts. Since both of the resistors connected to the base of Q3 are equal, the emitter of Q4 (base of Q5) will be approximately 3.0 volts. For this condition, the emitter of Q5 (DF) will be one $V_{BE}$ below this voltage, or about 2.25 volts. The PU input to the charge pump is high (> 2.4 volts) and CR1 will be reverse biased. Therefore Q5 will be supplying current to Q6. This will tend to lower the voltage at the collector of Q7, resulting in an error signal that lowers the VCO frequency as required by a "pump down" signal.

When PU is low and PD is high, CR1 is forward biased and UF will be approximately one $V_{BE}$ above ground (neglecting the $V_{CE(sat)}$ of the driving gate). With PD high, Q1 conducts in the reverse direction, supplying base current for Q2. While Q2 is conducting, Q4 is prevented from supplying base drive to Q5; with Q5 cut off and UF low there is no base current for Q6 and the voltage at the

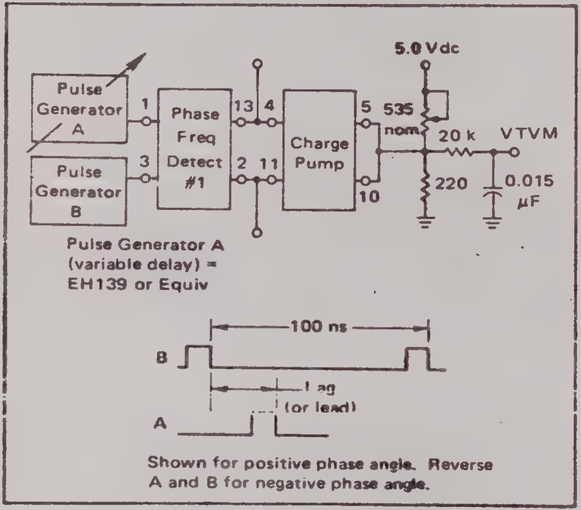
FIGURE 4 – CHARGE PUMP OPERATION



collector of Q7 moves up, resulting in an increase in the VCO operating frequency as required by a "pump up" signal.

If both inputs to the charge pump are high (zero phase difference), both CR1 and the base-emitter junction of Q5 are reverse biased and there is no tendency for the error voltage to change. The output of the charge pump varies between one $V_{BE}$ and three $V_{BE}$ as the phase difference of R and V varies from minus $2\pi$ to plus $2\pi$. If this signal is filtered to remove the high-frequency components, the phase detector transfer function, $K_\phi$, of approximately 0.12 volt/radian is obtained (see Figure 5).

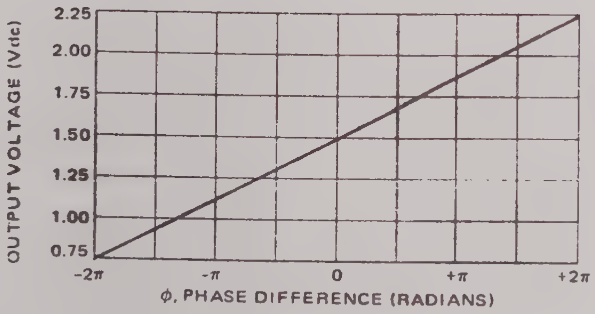
FIGURE 5 – PHASE DETECTOR TEST



Pulse Generator A (variable delay) = EH139 or Equiv

Shown for positive phase angle. Reverse A and B for negative phase angle.

The specified gain constant of 0.12 volt/radian may not be obtained if the amplifier/filter combination is improperly designed. As indicated previously, the charge pump delivers pump commands of about 2.25 volts on the positive swings and 0.75 volt on the negative swings for a mean no-pump value of 1.5 volts. If the filter amplifier is biased to threshold "on" at 1.5 volts, then the pump up and down voltages have equal effects. The pump signals are established by $V_{BE}$'s of transistors with milliamperes of current flowing. On the other hand, the transistors included for use as a filter amplifier will have very small currents flowing and will have correspondingly lower $V_{BE}$'s – on the order of 0.6 volt each for a threshold of 1.2 volts. Any displacement of the threshold from 1.5 volts causes an increase in gain in one direction and a reduction in the other. The transistor configuration provided is hence not optimum but does allow for the use of an additional transistor to improve filter response. This addition also results in a non-symmetrical response since the threshold is now approximately 1.8 volts. The effective positive swing is limited to 0.45 volt while the negative swing below threshold can be greater than 1.0 volt. This means that the loop gain when changing from a high frequency to a lower frequency is less than when changing in the opposite direction. For type two loops this tends to increase overshoot when going from low to high and increases damping in the other direction. These problems and the selection of external filter components are intimately related to system requirements and are discussed in detail in the filter design section.



MC7805CT
& MC7815CT

**+5 VOLT REGULATOR**
**+15 VOLT REGULATOR**

S-D P/N 045256
S-D P/N 103039

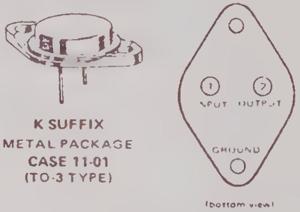
# MC7800C Series

## MC7800C SERIES THREE-TERMINAL POSITIVE VOLTAGE REGULATORS

The MC7800C Series of three-terminal positive voltage regulators are monolithic integrated circuits designed as fixed-voltage regulators for a wide variety of applications including local, on-card regulation. Available in seven fixed output voltage options from 5.0-to-24 volts, these regulators employ internal current limiting, thermal shutdown, and safe area compensation — making them essentially blow-out proof. With adequate heatsinking they can deliver output currents in excess of 1.0 ampere. The last two digits of the part number indicate nominal output voltage.

- Output Current in Excess of 1.0 Ampere
- No External Components Required
- Internal Thermal Overload Protection
- Internal Short-Circuit Current Limiting
- Output Transistor Safe-Area Compensation
- Packaged in the Plastic Case 313 and Case 11 (TO-220 and Hermetic TO 3)

## THREE-TERMINAL POSITIVE FIXED VOLTAGE REGULATORS



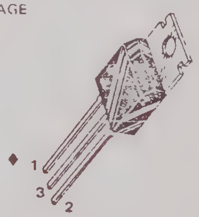
K SUFFIX
METAL PACKAGE
CASE 11-01
(TO-3 TYPE)

(bottom view)

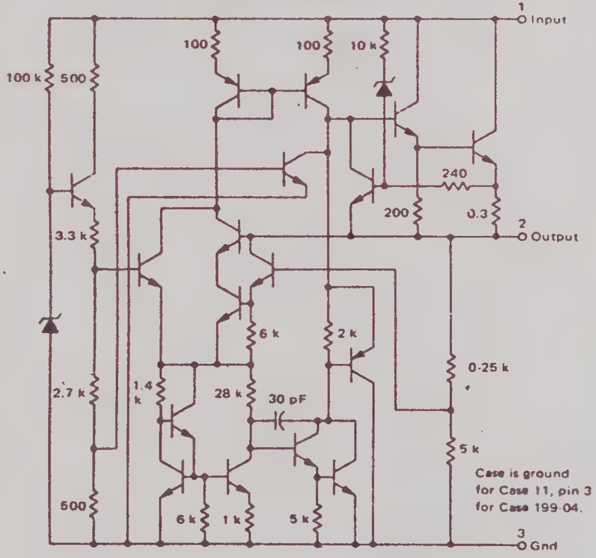
Pins 1 and 2 electrically isolated from case. Case is third electrical connection

T SUFFIX
PLASTIC PACKAGE
CASE 313
TO-220

1 Input
2 Output
3 Ground

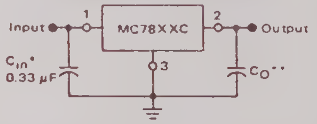


### SCHEMATIC DIAGRAM



Case is ground for Case 11, pin 3 for Case 199-04.

### ◆ STANDARD APPLICATION



A common ground is required between the input and the output voltages. The input voltage must remain typically 2.0 V above the output voltage even during the low point on the input ripple voltage.

XX = these two digits of the type number indicate voltage.

* = $C_{in}$ is required if regulator is located an appreciable distance from power supply filter.

** = $C_O$ is not needed for stability; however, it does improve transient response.

XX indicates nominal voltage

### TYPE NO./VOLTAGE

| | |
|---|---|
| MC7805C | 5.0 Volts |
| MC7806C | 6.0 Volts |
| MC7808C | 8.0 Volts |
| MC7812C | 12 Volts |
| MC7815C | 15 Volts |
| MC7818C | 18 Volts |
| MC7824C | 24 Volts |

ORDERING INFORMATION

| DEVICE | TEMPERATURE RANGE | PACKAGE |
|---|---|---|
| MC78XXCK | $T_J$ = 0° C to +150° C | Metal Power |
| MC78XXCT | $T_J$ = 0° C to +150° C | Plastic Power |

# +12 VOLT REGULATOR

MC78L12ACP | S-D P/N 117013

## THREE-TERMINAL POSITIVE VOLTAGE REGULATORS

The MC78L00 Series of positive voltage regulators are inexpensive, easy-to-use devices suitable for a multitude of applications that require a regulated supply of up to 100 mA. Like their higher powered MC7800 and MC78M00 Series cousins, these regulators feature internal current limiting and thermal shutdown making them remarkably rugged. No external components are required with the MC78L00 devices in many applications.

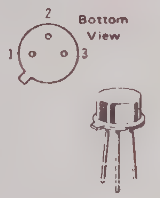
These devices offer a substantial performance advantage over the traditional zener diode-resistor combination. Output impedance is greatly reduced and quiescent current is substantially reduced.

- Wide Range of Available, Fixed Output Voltages
- Low Cost
- Internal Short-Circuit Current Limiting
- Internal Thermal Overload Protection
- No External Components Required
- Complementary Negative Regulators Offered (MC79L00 Series)
- Available in Either ±5% (AC) or ±10% (C) Selections

## THREE-TERMINAL POSITIVE FIXED VOLTAGE REGULATORS

**P SUFFIX**
CASE 29
TO-92

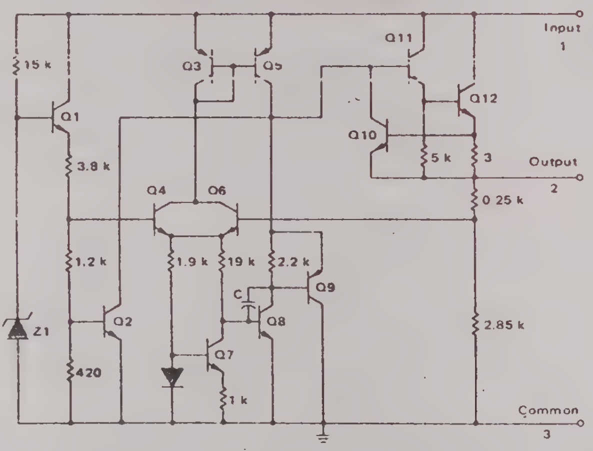
1. INPUT ◆
2. OUTPUT
3. GROUND



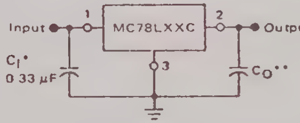
**G SUFFIX**
CASE 79
TO-39

1. INPUT ◆
2. OUTPUT
3. GROUND

### REPRESENTATIVE CIRCUIT SCHEMATIC



### ◆ STANDARD APPLICATION



A common ground is required between the input and the output voltages. The input voltage must remain typically 2.0 V above the output voltage even during the low point on the input ripple voltage.

* = $C_I$ is required if regulator is located an appreciable distance from power supply filter.

** = $C_O$ is not needed for stability; however, it does improve transient response.

| Device No. ±10% | Device No. ±5% | Nominal Voltage |
|---|---|---|
| — | MC78L02AC | 2.6 |
| MC78L05C | MC78L05AC | 5.0 |
| MC78L08C | MC78L08AC | 8.0 |
| MC78L12C | MC78L12AC | 12 |
| MC78L15C | MC78L15AC | 15 |
| MC78L18C | MC78L18AC | 18 |
| MC78L24C | MC78L24AC | 24 |

ORDERING INFORMATION

| Device | Temperature Range | Package |
|---|---|---|
| MC78LXXACG | $T_J$ = 0°C to +150°C | Metal Can |
| MC78LXXACP | $T_J$ = 0°C to +150°C | Plastic Transistor |
| MC78LXXCG | $T_J$ = 0°C to +150°C | Metal Can |
| MC78LXXCP | $T_J$ = 0°C to +150°C | Plastic Transistor |

XX indicates nominal voltage

MC7905.2CT
& MC7915CT

# -5.2 VOLT REGULATOR
# -15 VOLT REGULATOR

S-D P/N 103033
S-D P/N 103040

## MC7900C SERIES THREE-TERMINAL NEGATIVE VOLTAGE REGULATORS

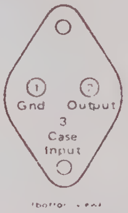
The MC7900C Series of fixed output negative voltage regulators are intended as complements to the popular MC7800C Series devices. These negative regulators are available in the same seven voltage options as the MC7800C devices. In addition, two extra voltage options commonly employed in MECL systems are also available in the negative MC7900C Series.

Available in fixed output voltage options from -2.0 to -24 volts, these regulators employ current limiting, thermal shutdown, and safe-area compensation – making them remarkably rugged under most operating conditions. With adequate heat-sinking they can deliver output currents in excess of 1.0 ampere.

- No External Components Required
- Internal Thermal Overload Protection
- Internal Short Circuit Current Limiting
- Output Transistor Safe-Area Compensation
- Packaged in the Plastic Case 313 and Case 11 (TO 220 and Hermetic TO 3)

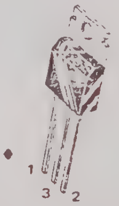
## THREE-TERMINAL NEGATIVE FIXED VOLTAGE REGULATORS

K SUFFIX
METAL PACKAGE
CASE 11-01
(TO 3 TYPE)

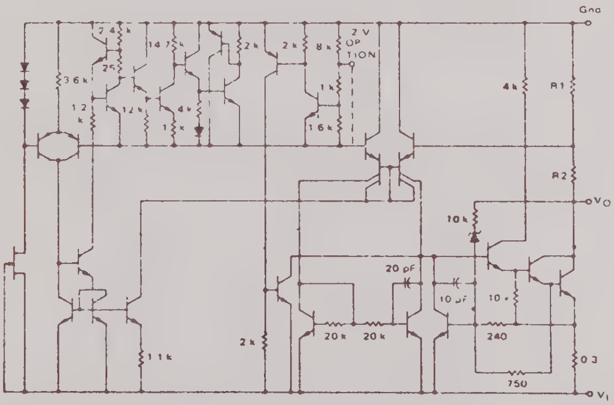


T SUFFIX
PLASTIC PACKAGE
CASE 313

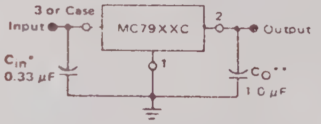
1 Gnd
2 Output
3 Input



### SCHEMATIC DIAGRAM



### ◆ STANDARD APPLICATION



A common ground is required between the input and the output voltages. The input voltage must remain typically 2.0 V more negative even during the high point on the input ripple voltage.

XX = these two digits of the type number indicate voltage

* = $C_{in}$ is required if regulator is located an appreciable distance from power supply filter.

** = $C_O$ improves stability and transient response

### DEVICE TYPE/NOMINAL OUTPUT VOLTAGE

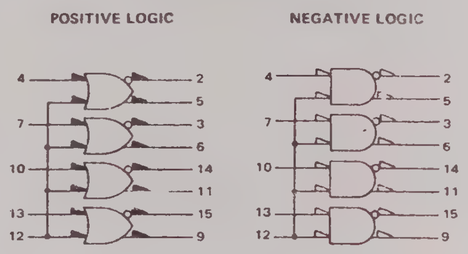
MC7902C - 2.0 Volts
MC7905C - 5.0 Volts
MC7905.2C - 5.2 Volts
MC7906C - 6.0 Volts
MC7908C - 8.0 Volts
MC7912C - 12 Volts
MC7915C - 15 Volts
MC7918C - 18 Volts
MC7924C - 24 Volts

| ORDERING INFORMATION | | |
|---|---|---|
| DEVICE | TEMPERATURE RANGE | PACKAGE |
| MC79XXCK | $T_J$ = 0° C to +150° C | Metal Power |
| MD79XXCT | $T_J$ - 0° C to +150° C | Plastic Power |
| XX indicates nominal voltage | | |

## ECL QUAD OR/NOR GATE

**MC10101L** S-D P/N 025791

The MC10101 is a quad 2-input OR/NOR gate with one input from each gate common to pin 12. Input pulldown resistors eliminate the need to tie unused inputs to an external supply.


POSITIVE LOGIC
NEGATIVE LOGIC
4
7
10
13
12
2
5
3
6
14
11
15
9

$V_{CC1}$ = Pin 1
$V_{CC2}$ = Pin 16
$V_{EE}$ = Pin 8

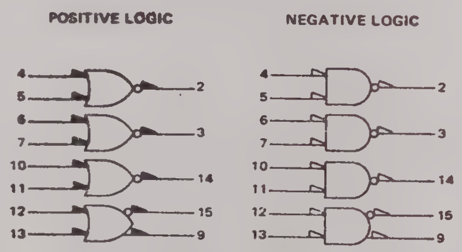
$P_D$ = 25 mW typ/gate (No Load)
$t_{pd}$ = 2.0 ns typ
Output Rise and Fall Time:
= 3.5 ns typ (10% - 90%)
= 2.0 ns typ (20% - 80%)

---

## ECL QUAD 2-INPUT NOR GATE

**MC10102P** S-D P/N 103025

The MC10102 is a quad 2-input NOR gate. Input pulldown resistors eliminate the need to tie unused inputs to an external supply.


POSITIVE LOGIC
NEGATIVE LOGIC
4
5
6
7
10
11
12
13
2
3
14
15
9

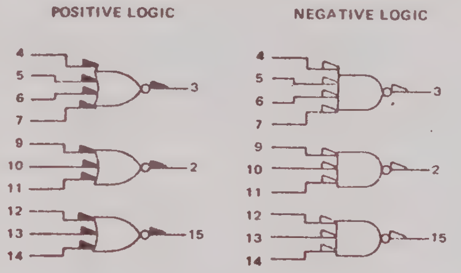
$V_{CC1}$ = Pin 1
$V_{CC2}$ = Pin 16
$V_{EE}$ = Pin 8

$P_D$ = 25 mW typ/gate (No Load)
$t_{pd}$ = 2.0 ns typ
Output Rise and Fall Time:
= 3.5 ns typ (10% - 90%)
= 2.0 ns typ (20% - 80%)

## ECL TRIPLE 4-3-3 INPUT NOR GATE

MC10106P

S-D P/N 103168


POSITIVE LOGIC

NEGATIVE LOGIC

$V_{CC1}$ = Pin 1
$V_{CC2}$ = Pin 16
$V_{EE}$ = Pin 8

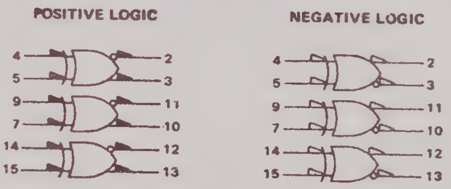
The MC10106 is a triple 4-3-3 input NOR gate. Input pulldown resistors eliminate the need to tie unused inputs to an external supply.

$P_D$ = 30 mW typ/gate (No Load)
$t_{pd}$ = 2.0 ns typ
Output Rise and Fall Time
= 3.5 ns typ (10% - 90%)
= 2.0 ns typ (20% - 80%)

## ECL TRIPLE 2-INPUT EXCLUSIVE OR/NOR GATE

MC10107P

S-D P/N 103179


POSITIVE LOGIC

NEGATIVE LOGIC

Positive logic:
$3 = (4 \bullet \overline{5}) + (\overline{4} \bullet 5)$
$2 = (\overline{4} \bullet \overline{5}) + (4 \bullet 5)$

$V_{CC1}$ = Pin 1
$V_{CC2}$ = Pin 16
$V_{EE}$ = Pin 8

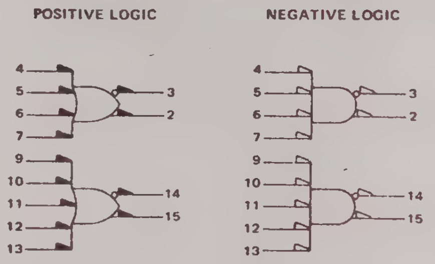
Negative logic:
$3 = (\overline{4} \bullet \overline{5}) + (4 \bullet 5)$
$2 = (4 \bullet \overline{5}) + (\overline{4} \bullet 5)$

This three gate array is designed to provide the positive logic Exclusive OR and Exclusive NOR functions in high speed applications. Input pulldown resistors eliminate the need to tie unused inputs to $V_{EE}$.

$P_D$ = 40 mW typ/gate (No Load)
$t_{pd}$ = 2.5 ns typ
Output Rise and Fall Times
= 2.5 ns typ (20% to 80%)
= 3.5 ns typ (10% to 90%)

## ECL DUAL 4-5 INPUT OR/NOR GATE

**MC10109P** S-D P/N 103026



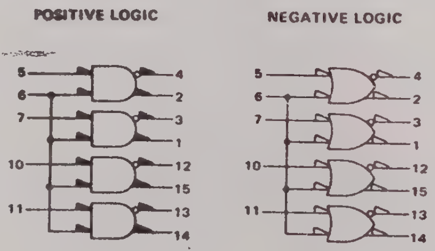
$V_{CC1} = 1$
$V_{CC2} = 16$
$V_{EE} = 8$

The MC10109 is a dual 4-5 input OR-NOR gate which is pin compatible with the MECL III MC1660L dual OR-NOR gate. All inputs are terminated by a 50 k ohm resistor to $V_{EE}$ eliminating the need to tie unused inputs low.

$t_{pd}$ = 2.0 ns typ
$P_D$ = 30 mW typ/gate (No Load)
Output Rise and Fall Times
(10% to 90%) 3.5 ns
(20% to 80%) 2.0 ns

## ECL QUAD TTL TO ECL TRANSLATOR

**MC10124L** S-D P/N 045228



Gnd = Pin 16
$V_{CC}$ (+5.0 Vdc) = Pin 9
$V_{EE}$ (-5.2 Vdc) = Pin 8

The MC10124 is a quad translator for interfacing data and control signals between a saturated logic section and the MECL section of digital systems. The MC10124 has MTTL compatible inputs, and MECL complementary open-emitter outputs that allow use as an inverting/non-inverting translator or as a differential line driver. When the common strobe input is at the low logic level, it forces all true outputs to a MECL low logic state and all inverting outputs to a MECL high logic state.

Power supply requirements are ground, +5.0 Volts, and -5.2 Volts. Propagation delay of the MC10124 is typically 3.5 ns. The dc levels are standard or Schottky TTL in, MECL 10,000 out.

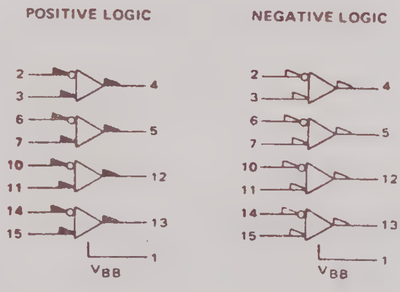
An advantage of this device is that MTTL level information can be transmitted differentially, via balanced twisted pair lines, to the MECL equipment, where the signal can be received by the MC10115 or MC10116 differential line receivers. The MC10124 is useful in computers, instrumentation, peripheral controllers, test equipment, and digital communications systems.

$P_D$ = 380 mW typ/pkg (No Load)
$t_{pd}$ = 3.5 ns typ (+1.5 Vdc in to 50% out)
Output Rise, Fall Times;
2.5 ns typ (20% to 80%)

# ECL QUAD ECL TO TTL TRANSLATOR

MC10125L

S-D P/N 045226



Gnd = Pin 16
$V_{CC}$ (+5 0 Vdc) - Pin 9
$V_{EE}$ (-5.2 Vdc) = Pin 8

The MC10125 is a quad translator for interfacing data and control signals between the MECL section and saturated logic sections of digital systems. The MC10125 incorporates differential inputs and Schottky MTTL "totem pole" outputs. Differential inputs allow for use as an inverting/non-inverting translator or as a differential line receiver. The $V_{BB}$ reference voltage is available on pin 1 for use in single-ended input biasing. The outputs of the MC10125 go to a low logic level whenever the inputs are left floating.

Power supply requirements are ground, **+5.0 Volts** and -5.2 Volts. Propagation delay of the **MC10125** is typically 4.5 ns. The MC10125 has fanout of 10 MTTL loads. The dc levels are MECL 10,000 in and Schottky TTL, or MTTL out. This device has an input common mode noise rejection of ±1.0 Volt.

An advantage of this device is that MECL level information can be received, via balanced twisted pair lines, in the MTTL equipment. This isolates the MECL logic from the noisy MTTL environment. This device is useful in computers, instrumentation, peripheral controllers, test equipment and digital communications systems.

$P_D$ = 380 mW typ/pkg (No Load)
$t_{pd}$ = 4.5 ns typ (50% to +1.5 Vdc out)
Output Rise, Fall Times,
2 5 ns typ (20% to 80%)
$V_{CCmax}$ = +7.00 Vdc

# ECL DUAL TYPE D MASTER-SLAVE FLIP-FLOP

MC10131L

S-D P/N 045239

The MC10131 is a dual master-slave type D flip-flop. Asynchronous Set (S) and Reset (R) override Clock ($C_C$) and Clock Enable ($\bar{C}_E$) inputs. Each flip-flop may be clocked separately by holding the common clock in the low state and using the enable inputs for the clocking function. If the common clock is to be used to clock the flip-flop, the Clock Enable inputs must be in the low state. In this case, the enable inputs perform the function of controlling the common clock.

The output states of the flip-flop change on the positive transition of the clock. A change in the information present at the data (D) input will not affect the output information at any other time due to master slave construction.

Input pulldown resistors eliminate the need to tie unused inputs to $V_{EE}$. Output rise and fall times have been optimized to provide relaxation of system design and layout criteria.

**R-S TRUTH TABLE**

| R | S | $Q_{n+1}$ |
|---|---|---|
| L | L | $Q_n$ |
| L | H | H |
| H | L | L |
| H | H | N.D. |

N.D. = Not Defined

**CLOCKED TRUTH TABLE**

| C | D | $Q_{n+1}$ |
|---|---|---|
| L | $\phi$ | $Q_n$ |
| H | L | L |
| H | H | H |

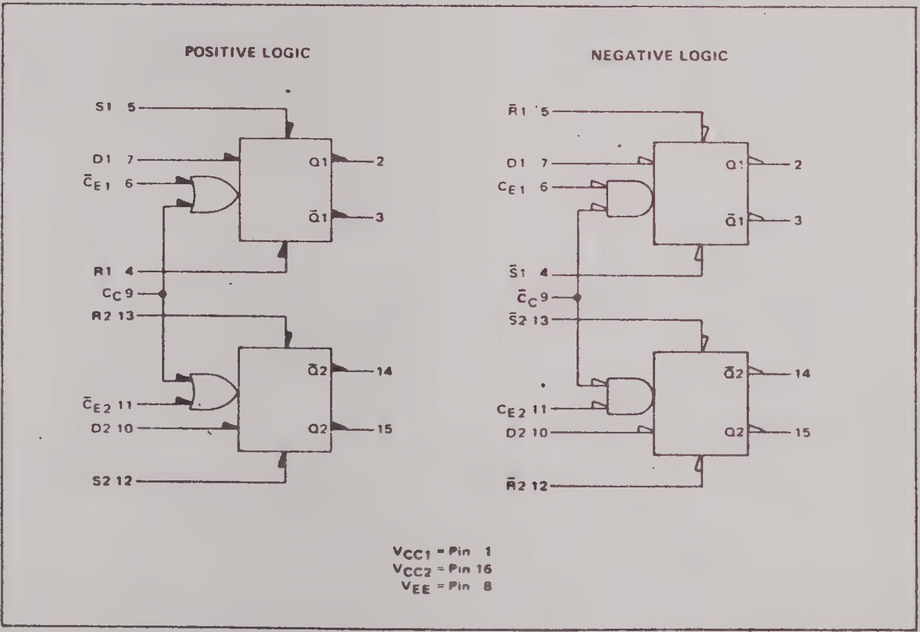
$\phi$ = Don't Care

$C = \bar{C}_E + C_C$.

A clock H is a clock transition from a low to a high state.

$P_D$ = 235 mW typ/pkg (No Load)

$f_{Tog}$ = 160 MHz typ


POSITIVE LOGIC
NEGATIVE LOGIC
S1 5
D1 7
$\bar{C}_{E1}$ 6
R1 4
$C_C$ 9
R2 13
$\bar{C}_{E2}$ 11
D2 10
S2 12
Q1 2
$\bar{Q}1$ 3
$\bar{Q}2$ 14
Q2 15
$\bar{R}1$ 5
D1 7
$C_{E1}$ 6
$\bar{S}1$ 4
$\bar{C}_C$ 9
$\bar{S}2$ 13
$C_{E2}$ 11
D2 10
$\bar{R}2$ 12
Q1 2
$\bar{Q}1$ 3
$\bar{Q}2$ 14
Q2 15

$V_{CC1}$ = Pin 1
$V_{CC2}$ = Pin 16
$V_{EE}$ = Pin 8

# ECL UNIVERSAL HEXADECIMAL COUNTER

MC10136L

S-D P/N 103169

**SEQUENTIAL TRUTH TABLE***

| INPUTS | | | | | | | | OUTPUTS | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| S1 | S2 | D0 | D1 | D2 | D3 | $\overline{\text{Carry In}}$ | Clock ** | Q0 | Q1 | Q2 | Q3 | $\overline{\text{Carry Out}}$ |
| L | L | L | L | H | H | φ | H | L | L | H | H | L |
| L | H | φ | φ | φ | φ | L | H | H | L | H | H | H |
| L | H | φ | φ | φ | φ | L | H | L | H | H | H | H |
| L | H | φ | φ | φ | φ | L | H | H | H | H | H | L |
| L | H | φ | φ | φ | φ | H | L | H | H | H | H | H |
| L | H | φ | φ | φ | φ | H | H | H | H | H | H | H |
| H | H | φ | φ | φ | φ | φ | H | H | H | H | H | H |
| L | L | H | H | L | L | φ | H | H | H | L | L | L |
| H | L | φ | φ | φ | φ | L | H | L | H | L | L | H |
| H | L | φ | φ | φ | φ | L | H | H | L | L | L | H |
| H | L | φ | φ | φ | φ | L | H | L | L | L | L | L |
| H | L | φ | φ | φ | φ | L | H | H | H | H | H | H |

φ = Don't care.

* Truth table shows logic states assuming inputs vary in sequence shown from top to bottom.

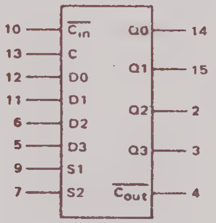
** A clock H is defined as a clock input transition from a low to a high logic level.

The MC10136 is a high speed synchronous counter that can count up, count down, preset, or stop count at frequencies exceeding 100 MHz. This binary counter is useful in high speed central processors and peripheral controllers, minicomputers, high speed digital communications equipment and instrumentation. The flexibility of this device allows the designer to use one basic counter for most applications, and the synchronous count feature makes the **MC10136** suitable for either computers or instrumentation.

Three control lines (S1, S2, and $\overline{\text{Carry In}}$) determine the operation mode of the counter. Lines S1 and S2 determine one of four operations, preset (program), increment (count up), decrement (count down), or hold (stop count). Note that in the preset mode a clock pulse is necessary to load the counter, and the information present on the data inputs (D0, D1, D2, and D3) will be entered into the counter. $\overline{\text{Carry Out}}$ goes low on the terminal count, or when the counter is being preset.

This device is not designed for use with gated clocks. Control is via S1 and S2.

A prescaler can be constructed using the MC10136 in conjunction with the MC10231 which will operate at over 200 MHz input frequency. A 500 MHz prescaler is possible using an MC1690 500 MHz D Flip-Flop, an MC1670 300 MHz D Flip-Flop, and the MC10136.



$V_{CC1}$ = Pin 1
$V_{CC2}$ = Pin 16
$V_{EE}$ = Pin 8

**FUNCTION SELECT TABLE**

| S1 | S2 | Operating Mode |
|---|---|---|
| L | L | Preset (Program) |
| L | H | Increment (Count Up) |
| H | L | Decrement (Count Down) |
| H | H | Hold (Stop Count) |

$P_D$ = 625 mW typ/pkg (No Load)
$f_{count}$ = 150 MHz typ

# ECL BINARY COUNTER

**MC10178P** S-D P/N 103273

The MC10178 is a four-bit counter capable of divide-by-two, divide-by-four, divide-by-eight or a divide-by-sixteen function.

Clock inputs trigger on the positive going edge of the clock pulse. Set and Reset inputs override the clock, allowing asynchronous "set" or "clear". Individual Set and common Reset inputs are provided, as well as complementary outputs for the first and fourth bits. True outputs are available at all bits.

$P_D$ = 370 mW typ/pkg (No Load)
$f_{toggle}$ 150 MHz (typ)

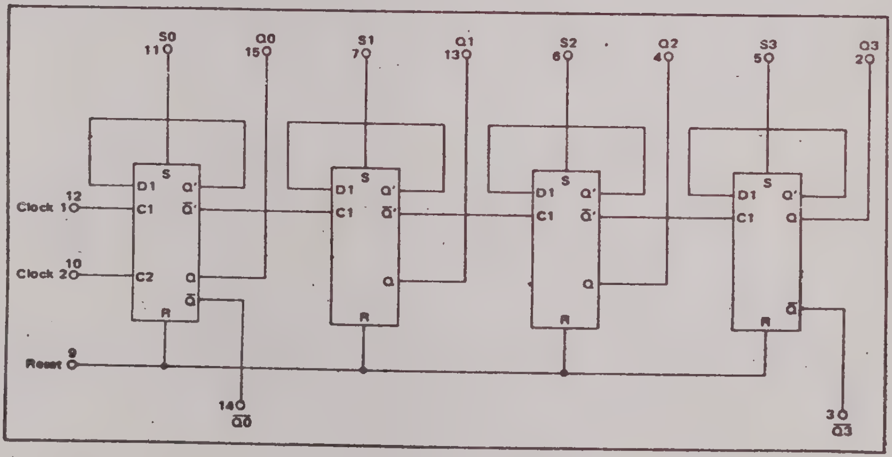
TRUTH TABLE

| INPUTS | | | | | | | OUTPUTS | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| R | S0 | S1 | S2 | S3 | C1 | C2 | Q0 | Q1 | Q2 | Q3 |
| H | L | L | L | L | ϕ | ϕ | L | L | L | L |
| L | H | H | H | H | ϕ | ϕ | H | H | H | H |
| L | L | L | L | L | H | ϕ | No Count | | | |
| L | L | L | L | L | ϕ | H | No Count | | | |
| L | L | L | L | L | •• | | L | L | L | L |
| L | L | L | L | L | •• | | H | L | L | L |
| L | L | L | L | L | •• | | L | H | L | L |
| L | L | L | L | L | •• | | H | H | L | L |
| L | L | L | L | L | •• | | L | L | H | L |
| L | L | L | L | L | •• | | H | L | H | L |
| L | L | L | L | L | •• | | L | H | H | L |
| L | L | L | L | L | •• | | H | H | H | L |
| L | L | L | L | L | •• | | L | L | L | H |
| L | L | L | L | L | •• | | H | L | L | H |
| L | L | L | L | L | •• | | L | H | L | H |
| L | L | L | L | L | •• | | H | H | L | H |
| L | L | L | L | L | •• | | L | L | H | H |
| L | L | L | L | L | •• | | H | L | H | H |
| L | L | L | L | L | •• | | L | H | H | H |
| L | L | L | L | L | •• | | H | H | H | H |

ϕ = Don't Care

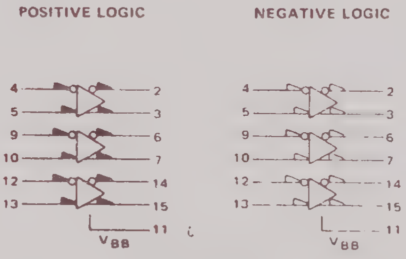
•• $V_{IL}$ ⟋ $V_{IH}$ Clock transition from $V_{IL}$ to $V_{IH}$ may be applied to C1 or C2 or both for same effect.

$V_{CC1}$ = Pin 1
$V_{CC2}$ = Pin 16
$V_{EE}$ = Pin 8



# ECL HIGH SPEED TRIPLE LINE RECEIVER

MC10216L S-D P/N 045276



$V_{CC1}$ = Pin 1
$V_{CC2}$ = Pin 16
$V_{EE}$ = Pin 8

The MC10216 is a high speed triple differential amplifier designed for use in sensing differential signals over long lines. The base bias supply ($V_{BB}$) is made available at pin 11 to make the device useful as a Schmitt trigger, or in other applications where a stable reference voltage is necessary.

Active current sources provide the MC10216 with excellent common mode noise rejection. If any amplifier in a package is not used, one input of that amplifier must be connected to $V_{BB}$ (pin 11) to prevent upsetting the current source bias network.

Complementary outputs are provided to allow driving twisted pair lines, to enable cascading of several amplifiers in a chain, or simply to provide complement outputs of the input logic function.

**$P_D$ = 100 mW typ/pkg (No Load)**
**$t_{pd}$ = 1.8 ns typ (Single ended)**
**= 1.5 ns typ (Differential)**

# ECL HIGH SPEED DUAL TYPE D MASTER-SLAVE FLIP-FLOP

MC10231L S-D P/N 045227

The MC10231 is a dual master-slave type D flip-flop. Asynchronous Set (S) and Reset (R) override Clock($C_C$) and Clock Enable ($\bar{C}_E$) inputs. Each flip-flop may be clocked separately by holding the common clock in the low state and using the enable inputs for the clocking function. If the common clock is to be used to clock the flip-flop, the Clock Enable inputs must be in the low state. In this case, the enable inputs perform the function of controlling the common clock.

The output states of the flip-flop change on the positive transition of the clock. A change in the information present at the data (D) input will not affect the output information at any other time due to master slave construction.

Input pulldown resistors eliminate the need to tie unused inputs to $V_{EE}$. Output rise and fall times allow high frequency operation over 200 MHz.

**R-S TRUTH TABLE**

| R | S | $Q_{n+1}$ |
|---|---|---|
| L | L | $Q_n$ |
| L | H | H |
| H | L | L |
| H | H | N.D. |

N.D. = Not Defined

**CLOCKED TRUTH TABLE**

| C | D | $Q_{n+1}$ |
|---|---|---|
| L | ϕ | $Q_n$ |
| H | L | L |
| H | H | H |

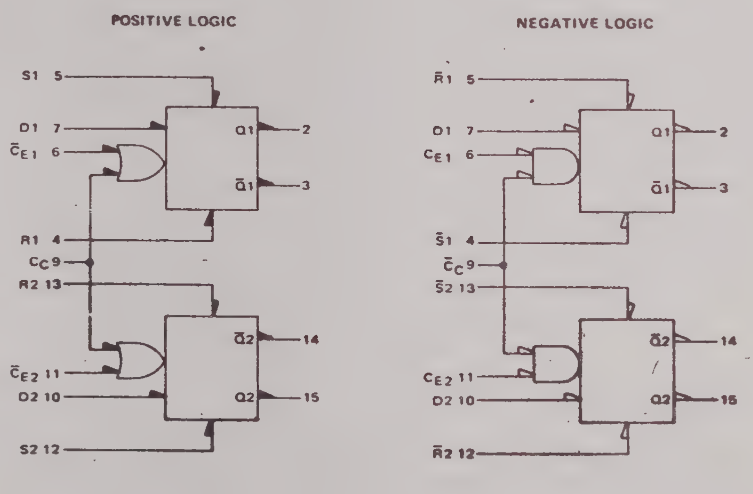
ϕ = Don't Care

$C = \bar{C}_E + C_C$.

A clock H is a clock transition from a low to a high state.

$P_D$ = 270 mW typ/pkg (No Load)

$f_{Tog}$ = 225 MHz typ


POSITIVE LOGIC
NEGATIVE LOGIC
S1 5
D1 7
C̄E1 6
Q1 2
Q̄1 3
R1 4
CC 9
R2 13
Q̄2 14
Q2 15
C̄E2 11
D2 10
S2 12
R̄1 5
D1 7
CE1 6
Q1 2
Q̄1 3
S̄1 4
C̄C 9
S̄2 13
Q̄2 14
CE2 11
D2 10
Q2 15
R̄2 12

$V_{CC1}$ = Pin 1
$V_{CC2}$ = Pin 16
$V_{EE}$ = Pin 8

# CMOS 12-BIT BINARY COUNTER

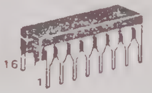
MC14040BCP

S-D P/N 117143

## 12-BIT BINARY COUNTER

The MC14040 12-stage binary counter is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. This part is designed with an input wave shaping circuit and 12 stages of ripple-carry binary counter. The device advances the count on the negative-going edge of the clock pulse. Applications include time delay circuits, counter controls, and frequency-driving circuits.

- Fully Static Operation
- Quiescent Power Dissipation = 50 nW/package typical @ $V_{DD}$ = 5.0 V
- Noise Immunity = 45% of $V_{DD}$ typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc (MC14040AL)
  = 3.0 Vdc to 16 Vdc (MC14040CL/CP)
- Low Input Capacitance = 5.0 pF typical
- All 12 Buffered Outputs Available
- Common Reset Line
- 13 MHz Typical Counting Rate @ $V_{DD}$ = 15 V
- Pin-for-Pin Replacement for CD4040A



**L SUFFIX**
CERAMIC PACKAGE
CASE 620

**P SUFFIX**
PLASTIC PACKAGE
CASE 648

### TRUTH TABLE

| CLOCK | RESET | OUTPUT STATE |
|---|---|---|
| _/‾ | 0 | No Change |
| ‾_ | 0 | Advance to next state |
| X | 1 | All Outputs are low |

X = Don't Care

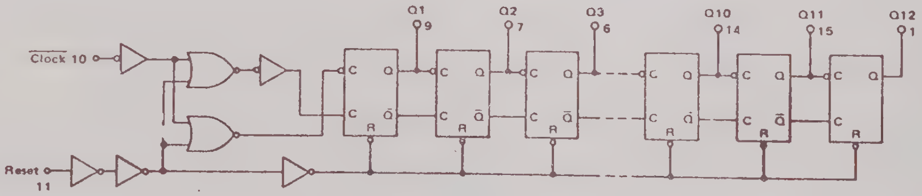
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that $V_{in}$ and $V_{out}$ be constrained to the range $V_{SS} \leqslant (V_{in}$ or $V_{out} \leqslant V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either $V_{SS}$ or $V_{DD}$).

### MAXIMUM RATINGS (Voltages referenced to $V_{SS}$, Pin 8)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| DC Supply Voltage MC14040AL<br>MC14040CL/CP | $V_{DD}$ | +18 to -0.5<br>+16 to -0.5 | Vdc |
| Input Voltage, All Inputs | $V_{in}$ | $V_{DD}$ to -0.5 | Vdc |
| DC Current Drain per Pin | I | 10 | mAdc |
| Operating Temperature Range – MC14040AL<br>– MC14040CL/CP | $T_A$ | -55 to +125<br>-40 to +85 | °C |
| Storage Temperature Range | $T_{stg}$ | -65 to +150 | °C |

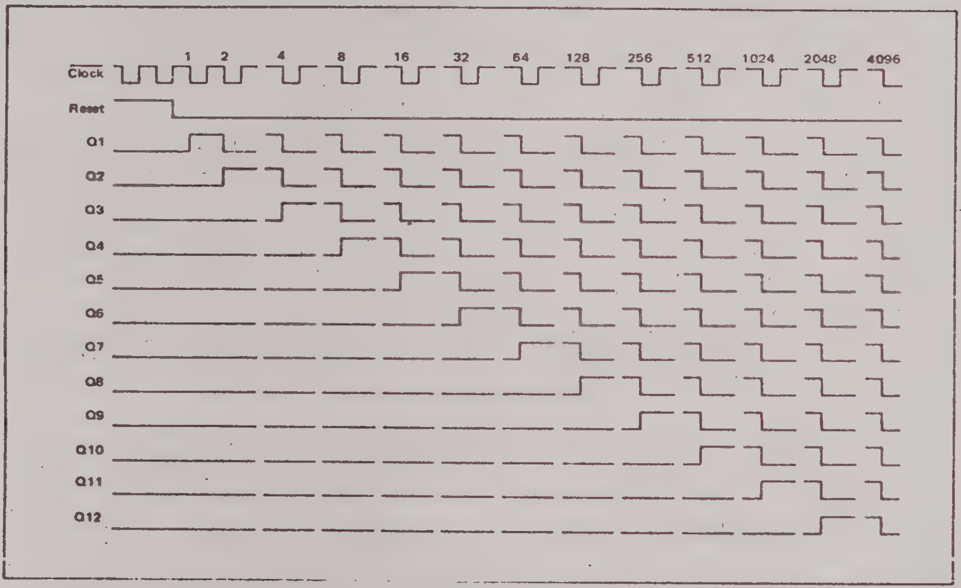
### LOGIC DIAGRAM



Q4 = Pin 5
Q5 = Pin 3
Q6 = Pin 2
Q7 = Pin 4
Q8 = Pin 13
Q9 = Pin 12

$V_{DD}$ = Pin 16
$V_{SS}$ = Pin 8

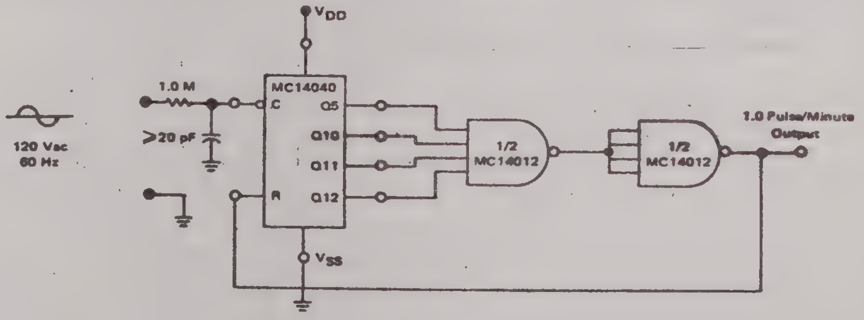
FIGURE 3 – TIMING DIAGRAM


Clock
1
2
4
8
16
32
64
128
256
512
1024
2048
4096
Reset
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
Q10
Q11
Q12

## APPLICATIONS INFORMATION

### TIME-BASE GENERATOR

A 60 Hz sinewave obtained through a 1.0 Megohm resistor connected directly to a standard 120 Vac power line is applied to the clock input of the MC14040. By selecting outputs Q5, Q10, Q11, and Q12 division by 3600 is accomplished. The MC14040 decodes the counter outputs, produces a single output pulse, and resets the binary counter. The resulting output frequency is 1.0 pulse/minute.


VDD
1.0 M
MC14040
C
Q5
Q10
Q11
Q12
R
>20 pF
120 Vac
60 Hz
1/2
MC14012
1/2
MC14012
1.0 Pulse/Minute
Output
VSS

# CMOS PROGRAMMABLE 4-BIT BINARY COUNTER

MC14526BCP S-D P/N 117144

**MC14522AL**
**MC14522CL**
**MC14522CP**
**MC14526AL**
**MC14526CL**
**MC14526CP**

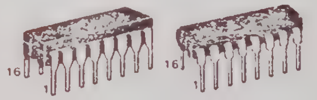
## PROGRAMMABLE DIVIDE-BY-N 4-BIT COUNTERS

The MC14522 BCD counter and the MC14526 binary counter are constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure.

These devices are programmable, cascadable down counters with a decoded "0" state output for divide-by-N applications. In single stage applications the "0" output is applied to the Preset Enable input. The Cascade Feedback input allows cascade divide-by-N operation with no additional gates required. The Master Reset function provides synchronous initiation of divide-by-N cycles. The Clock Inhibit input allows disabling of the pulse counting function.

These complementary MOS counters can be used in frequency synthesizers, phase-locked loops, and other frequency division applications requiring low power dissipation and/or high noise immunity.

- Quiescent Power Dissipation = 250 nW/package typical @ 5 Vdc
- Supply Voltage Range = 3.0 Vdc to 18 Vdc (AL Version)
  = 3.0 Vdc to 16 Vdc (CL, CP Version)
- Internally Synchronous for High Internal and External Speeds.
- Logic Edge-Clocked Design — Incremented on Positive Transition of Clock or Negative Transition of Clock Inhibit
- 5.0 MHz Counting Rate
- Asynchronous Preset Enable



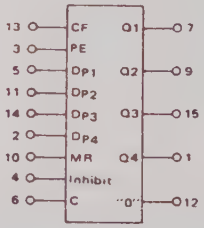
L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

## MAXIMUM RATINGS (Voltages referenced to $V_{SS}$, Pin 8)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| DC Supply Voltage — AL Version<br>— CL, CP Version | $V_{DD}$ | +18 to -0.5<br>+16 to -0.5 | Vdc |
| Input Voltage, All Inputs | $V_{in}$ | $V_{DD}$ to -0.5 | Vdc |
| DC Current Drain per Pin | I | 10 | mAdc |
| Operating Temperature Range — AL Version<br>— CL, CP Version | $T_A$ | -55 to +125<br>-40 to 85 | °C |
| Storage Temperature Range | $T_{stg}$ | -65 to +150 | °C |

### BLOCK DIAGRAM



$V_{DD}$ = Pin 16
$V_{SS}$ = Pin 8

### TRUTH TABLES

BOTH TYPES

| Clock | Inhibit | Preset Enable | Master Reset | Action |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | No Count |
| ↑ | 0 | 0 | 0 | Count 1 |
| X | 1 | 0 | 0 | No Count |
| 1 | ↓ | 0 | 0 | Count-1 |
| X | X | 1 | 0 | Preset |
| X | X | X | 1 | Reset |

MC14522

| Count | Output |  |  |  |
|---|---|---|---|---|
|  | Q4 | Q3 | Q2 | Q1 |
| 9 | 1 | 0 | 0 | 1 |
| 8 | 1 | 0 | 0 | 0 |
| 7 | 0 | 1 | 1 | 1 |
| 6 | 0 | 1 | 1 | 0 |
| 5 | 0 | 1 | 0 | 1 |
| 4 | 0 | 1 | 0 | 0 |
| 3 | 0 | 0 | 1 | 1 |
| 2 | 0 | 0 | 1 | 0 |
| 1 | 0 | 0 | 0 | 1 |
| 0 | 0 | 0 | 0 | 0 |

MC14526

| Count | Output |  |  |  |
|---|---|---|---|---|
|  | Q4 | Q3 | Q2 | Q1 |
| 15 | 1 | 1 | 1 | 1 |
| 14 | 1 | 1 | 1 | 0 |
| 13 | 1 | 1 | 0 | 1 |
| 12 | 1 | 1 | 0 | 0 |
| 11 | 1 | 0 | 1 | 1 |
| 10 | 1 | 0 | 1 | 0 |
| 9 | 1 | 0 | 0 | 1 |
| 8 | 1 | 0 | 0 | 0 |
| 7 | 0 | 1 | 1 | 1 |
| 6 | 0 | 1 | 1 | 0 |
| 5 | 0 | 1 | 0 | 1 |
| 4 | 0 | 1 | 0 | 0 |
| 3 | 0 | 0 | 1 | 1 |
| 2 | 0 | 0 | 1 | 0 |
| 1 | 0 | 0 | 0 | 1 |
| 0 | 0 | 0 | 0 | 0 |

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that $V_{in}$ and $V_{out}$ be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either $V_{SS}$ or $V_{DD}$).

# TTL PRESETTABLE HIGH SPEED DECADE COUNTER

NB2S90A

S-D P/N 103170

## DESCRIPTION

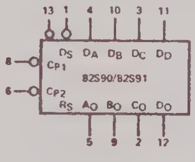
The 82S90 Decade Counter and 82S91 Binary Counter are very high speed versions of the popular 8290 Decade and 8291 Binary Counters. They are multifunctional MSI building blocks capable of being used in counting frequency synthesis, digital integration where high speed is essential.

## FEATURES

- 100 MHz TYPICAL COUNT FREQUENCY
- HIGH IMPEDANCE PNP INPUTS
- VARIABLE MODULUS, ÷2, 4, 5, 8, 10, and 16
- STROBED PARALLEL ENTRY
- PIN REPLACEABLE for the 8290/8291, 74196/74197

## LOGIC SYMBOL

**A, F PACKAGES**


13
1
4
10
3
11
DS
DA
DB
DC
DD
8
CP1
82S90/82S91
6
CP2
RS
AO
BO
CO
DO
5
9
2
12

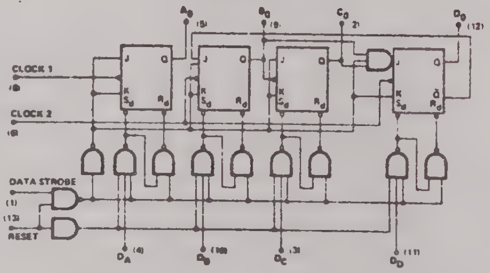
VCC = PIN 14
GND = PIN 7

## PIN DESIGNATIONS

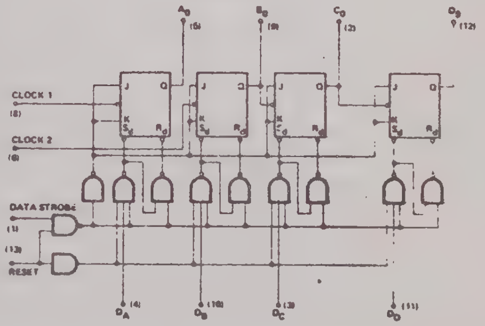
| | |
|---|---|
| $CP_1$ | Clock input to counter first stage (active low going edge) |
| $CP_2$ | Clock input to counter last three stages (active low going edge) |
| DS | Data Strobe Input for enabling data entry |
| RS | Reset input for resetting all stages and outputs to zero |
| $D_A, D_B, D_C, D_D$ | Data Inputs |
| $A_O, B_O, C_O, D_O$ | Data Outputs |

## LOGIC DIAGRAMS

**82S90**


A0 (5)
B0 (9)
C0 (2)
D0 (12)
CLOCK 1 (8)
CLOCK 2 (6)
DATA STROBE (1)
(13) RESET
DA (4)
DB (10)
DC (3)
DD (11)

**82S91**


A0 (5)
B0 (9)
C0 (2)
D0 (12)
CLOCK 1 (8)
CLOCK 2 (6)
DATA STROBE (1)
(13) RESET
DA (4)
DB (10)
DC (3)
DD (11)

**1. 82S90 Decade Counter**

The 82S90 can be used in three basic count modes as follows:

a. BCD Counter. The CP2 input must be connected to the $A_O$ output and CP1 receives the count input. The count sequence obtained is BCD in accordance with the truth table.

b. Bi-Quinary Counter. If a symmetrical output is required for divide by 10 operation, the $D_O$ output must be connected to the CP1 input and the count input applied to CP2. A symmetrical square wave is then obtained at $A_O$ of one-tenth the input frequency present at CP2 in accordance with the truth table.

c. Separate Divide by Two and Five Counters. Because the inherent structure of the counter is that of two separate divide by two and divide by five sections, no other connections are required for this mode of operation. An input presented to CP1 will appear at $A_O$ output at half the input frequency. An input presented to CP2 will appear at outputs $B_O$, $C_O$ and $D_O$ as a binary divide by five count (i.e., from 0 = 000 to 4 = 100). Operation of the $D_S$ and $R_S$ inputs remain common to all four flip flops as with any other count mode.

### TRUTH TABLES

| Decade (BCD) | | | | |
|---|---|---|---|---|
| Input | $A_0$ | $B_0$ | $C_0$ | $D_0$ |
| 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 |
| 2 | 0 | 1 | 0 | 0 |
| 3 | 1 | 1 | 0 | 0 |
| 4 | 0 | 0 | 1 | 0 |
| 5 | 1 | 0 | 1 | 0 |
| 6 | 0 | 1 | 1 | 0 |
| 7 | 1 | 1 | 1 | 0 |
| 8 | 0 | 0 | 0 | 1 |
| 9 | 1 | 0 | 0 | 1 |

| Bi-Quinary (5-2) | | | | |
|---|---|---|---|---|
| Input | $A_0$ | $B_0$ | $C_0$ | $D_0$ |
| 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 | 0 |
| 2 | 0 | 0 | 1 | 0 |
| 3 | 0 | 1 | 1 | 0 |
| 4 | 0 | 0 | 0 | 1 |
| 5 | 1 | 0 | 0 | 0 |
| 6 | 1 | 1 | 0 | 0 |
| 7 | 1 | 0 | 1 | 0 |
| 8 | 1 | 1 | 1 | 0 |
| 9 | 1 | 0 | 0 | 1 |

**2. 82S91 Binary Counter**

The 82S90 can be used in two basic count modes as follows:

a. Binary Counter—For this mode of operation $A_O$ output must be connected to CP2 input and the count input connected to CP1. Subdivisions of the count input frequency then appear at $A_O$ = ÷2, $B_O$ = ÷4, $C_O$ = ÷8, $D_O$ = ÷16 as shown in the truth table.

b. Separate Divide by Two and Divide by Eight Counters—In similar manner to the 82S90 the 82S91 inherent structure allows separate use of the first and last three stages. In the first stage the input count frequency presented to CP2 appears at outputs $B_O$ = ÷2, $C_O$ = ÷4 and $D_O$ = ÷8 simultaneously. Operation of the $D_S$ and $R_S$ inputs remains common to all stages.

### TRUTH TABLE

| Binary | | | | |
|---|---|---|---|---|
| Input | $A_0$ | $B_0$ | $C_0$ | $D_0$ |
| 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 |
| 2 | 0 | 1 | 0 | 0 |
| 3 | 1 | 1 | 0 | 0 |
| 4 | 0 | 0 | 1 | 0 |
| 5 | 1 | 0 | 1 | 0 |
| 6 | 0 | 1 | 1 | 0 |
| 7 | 1 | 1 | 1 | 0 |
| 8 | 0 | 0 | 0 | 1 |
| 9 | 1 | 0 | 0 | 1 |
| 10 | 0 | 1 | 0 | 1 |
| 11 | 1 | 1 | 0 | 1 |
| 12 | 0 | 0 | 1 | 1 |
| 13 | 1 | 0 | 1 | 1 |
| 14 | 0 | 1 | 1 | 1 |
| 15 | 1 | 1 | 1 | 1 |

**3. Operation of the $D_S$ Data Strobe and $R_S$ Reset Inputs:**

a. Data Strobe $D_S$ Input—When $D_S$ = 0 the four stages of the 82S90/91 can be used as four separate latches with the outputs $A_O$ - $D_O$ following the data presented to the inputs $D_A$ - $D_D$ regardless of clock inputs.

With $D_S$ = 1 the four stages remain unchanged until the next clock inputs, which activate counting in accordance with the various modes described previously. The Reset $R_S$ inputs when low overrides $D_S$ as described below.

b. Reset $R_S$ Input—With $R_S$ = 0 the clock inputs CP1/CP2 and $D_S$ input are overridden, all stages of the 82S90/91 are cleared and zeros appear at the counter outputs $A_O$ - $D_O$. When $R_S$ = 1, operation is controlled by $D_S$ or CP1/CP2 clock inputs as described.

# LINEAR WIDE RANGE TIMER

NE555V

S-D P/N 045208

## DESCRIPTION

The NE/SE 555 monolithic timing circuit is a highly stable controller capable of producing accurate time delays, or oscillation. Additional terminals are provided for triggering or resetting if desired. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For a stable operation as an oscillator, the free running frequency and the duty cycle are both accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on falling waveforms, and the output structure can source or sink up to 200mA or drive TTL circuits.

## FEATURES

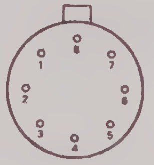
- TIMING FROM MICROSECONDS THROUGH HOURS
- OPERATES IN BOTH ASTABLE AND MONOSTABLE MODES
- ADJUSTABLE DUTY CYCLE
- HIGH CURRENT OUTPUT CAN SOURCE OR SINK 200mA
- OUTPUT CAN DRIVE TTL
- TEMPERATURE STABILITY OF 0.005% PER °C
- NORMALLY ON AND NORMALLY OFF OUTPUT

## APPLICATIONS

PRECISION TIMING
PULSE GENERATION
SEQUENTIAL TIMING
TIME DELAY GENERATION
PULSE WIDTH MODULATION
PULSE POSITION MODULATION
MISSING PULSE DETECTOR

## PIN CONFIGURATIONS

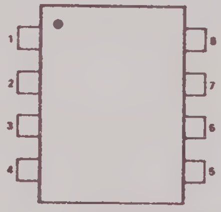
### T PACKAGE
(Top View)



1. Ground
2. Trigger
3. Output
4. Reset
5. Control Voltage
6. Threshold
7. Discharge
8. $V_{CC}$

ORDER PART NOS. SE555T/NE555T

### V PACKAGE
(Top View)



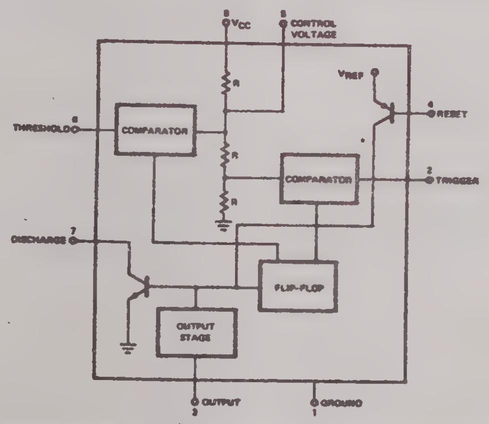
1. Ground
2. Trigger
3. Output
4. Reset
5. Control Voltage
6. Threshold
7. Discharge
8. $V_{CC}$

ORDER PART NOS. SE555V/NE555V

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply Voltage | +18V |
| Power Dissipation | 600 mW |
| Operating Temperature Range | |
| NE555 | 0°C to +70°C |
| SE555 | –55°C to +125°C |
| Storage Temperature Range | –65°C to +150°C |
| Lead Temperature (Soldering, 60 seconds) | +300°C |

## BLOCK DIAGRAM



### ASTABLE OPERATION

If the circuit is connected as shown in Figure 2a (pins 2 and 6 connected) it will trigger itself and free run as a multivibrator. The external capacitor charges through $R_A$ and $R_B$ and discharges through $R_B$ only. Thus the duty cycle may be precisely set by the ratio of these two resistors.

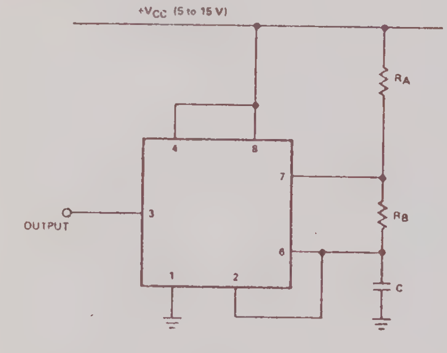


FIGURE 2a.

In this mode of operation, the capacitor charges and discharges between 1/3 $V_{CC}$ and 2/3 $V_{CC}$. As in the triggered mode, the charge and discharge times, and therefore the frequency are independent of the supply voltage.

The charge time (output high) is given by:

$$t_1 = 0.693\,(R_A + R_B)\,C$$

and the discharge time (output low) by:

$$t_2 = 0.693\,(R_B)\,C$$

Thus the total period is given by:

$$T = t_1 + t_2 = 0.693\,(R_A + 2R_B)\,C$$

The frequency of oscillation is then:

$$f = \frac{1}{T} = \frac{1.44}{(R_A + 2R_B)\,C}$$

and may be easily found by Figure 2c.

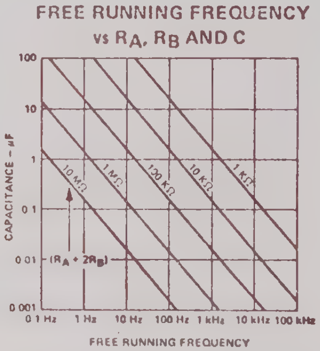


FIGURE 2c.

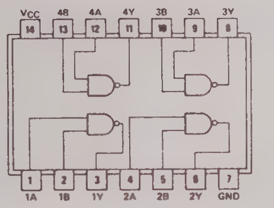
The duty cycle is given by:

$$D = \frac{R_B}{R_A + 2R_B}$$

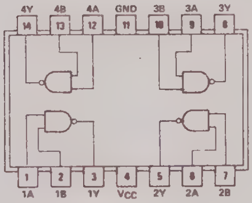
## TTL LOW POWER SCHOTTKY QUAD 2-INPUT NAND GATES

| | |
|---|---|
| SN7400N | S-D P/N 019705 |
| SN74L00N | S-D P/N 025796 |
| SN74LS00N | S-D P/N 103130 |
| SN74S00N | S-D P/N 025785 |

**positive logic:**
$Y = \overline{AB}$


VCC
4B
4A
4Y
3B
3A
3Y
14
13
12
11
10
9
8
1
2
3
4
5
6
7
1A
1B
1Y
2A
2B
2Y
GND

SN5400/SN7400(J, N)
SN54H00/SN74H00(J, N)
SN54L00/SN74L00(J, N)
SN54LS00/SN74LS00(J, N, W)
SN54S00/SN74S00(J, N, W)

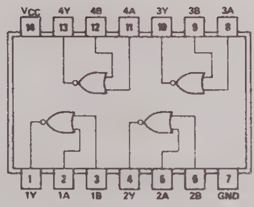

4Y
4B
4A
GND
3B
3A
3Y
14
13
12
11
10
9
8
1
2
3
4
5
6
7
1A
1B
1Y
VCC
2Y
2A
2B

SN5400/SN7400(W)
SN54H00/SN74H00(W)
SN54L00/SN74L00(T)

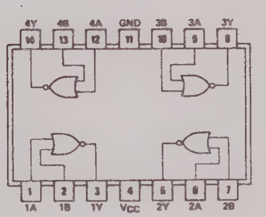
## QUADRUPLE 2-INPUT POSITIVE-NOR GATES

| | |
|---|---|
| SN7402N | S-D P/N 025709 |
| SN74L02N | S-D P/N 025797 |
| SN74LS02N | S-D P/N 103367 |

**positive logic:**
$Y = \overline{A+B}$


VCC
4Y
4B
4A
3Y
3B
3A
14
13
12
11
10
9
8
1
2
3
4
5
6
7
1Y
1A
1B
2Y
2A
2B
GND

SN5402/SN7402(J, N)
SN54L02/SN74L02(J, N)
SN54LS02/SN74LS02(J, N, W)
SN54S02/SN74S02(J, N, W)


4Y
4B
4A
GND
3B
3A
3Y
14
13
12
11
10
9
8
1
2
3
4
5
6
7
1A
1B
1Y
VCC
2Y
2A
2B

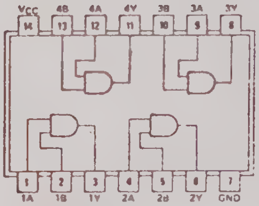
SN5402/SN7402(W)
SN54L02/SN74L02(T)

## QUADRUPLE 2-INPUT POSITIVE-AND GATES WITH OPEN-COLLECTOR OUTPUTS

SN7409N

S-D P/N 103321

**positive logic:**
Y = AB


VCC
4B
4A
4Y
3B
3A
3Y
14
13
12
11
10
9
8
1
2
3
4
5
6
7
1A
1B
1Y
2A
2B
2Y
GND

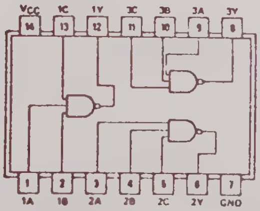
SN5409/SN7409(J, N, W)
SN54LS09/SN74LS09(J, N, W)

## TRIPLE 3-INPUT POSITIVE-NAND GATES

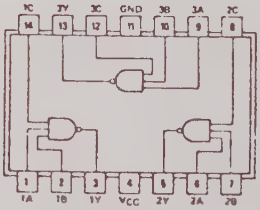
SN7410N
SN74H10N
SN74L10N
SN74LS10N

S-D P/N 019706
S-D P/N 025742
S-D P/N 045218
S-D P/N 103968

**positive logic:**
Y = $\overline{ABC}$


VCC
1C
1Y
3C
3B
3A
3Y
14
13
12
11
10
9
8
1
2
3
4
5
6
7
1A
1B
2A
2B
2C
2Y
GND

SN5410/SN7410(J, N)
SN54H10/SN74H10(J, N)
SN54L10/SN74L10(J, N)
SN54LS10/SN74LS10(J, N, W)
SN54S10/SN74S10(J, N, W)


1C
3Y
3C
GND
3B
3A
2C
14
13
12
11
10
9
8
1
2
3
4
5
6
7
1A
1B
1Y
VCC
2Y
2A
2B

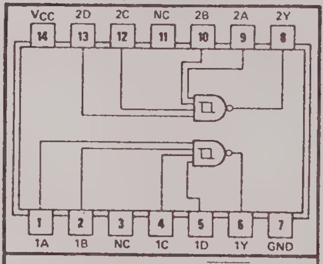
SN5410/SN7410(W)
SN54H10/SN74H10(W)
SN54L10/SN74L10(T)

# TTL LOW POWER SCHOTTKY SCHMITT TRIGGER HEX INVERTER

SN74LS13
SN74LS14N

S-D P/N
S-D P/N 117083

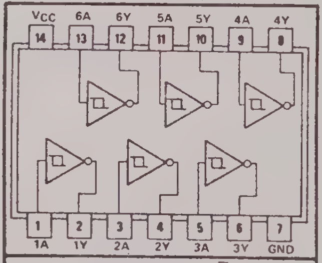
SN54LS13 . . . J OR W PACKAGE
SN74LS13 . . . J OR N PACKAGE
(TOP VIEW)


VCC
2D
2C
NC
2B
2A
2Y
14
13
12
11
10
9
8
1
2
3
4
5
6
7
1A
1B
NC
1C
1D
1Y
GND

positive logic: $Y = \overline{ABCD}$

NC—No internal connection

SN54LS14 . . . J OR W PACKAGE
SN74LS14 . . . J OR N PACKAGE
(TOP VIEW)


VCC
6A
6Y
5A
5Y
4A
4Y
14
13
12
11
10
9
8
1
2
3
4
5
6
7
1A
1Y
2A
2Y
3A
3Y
GND

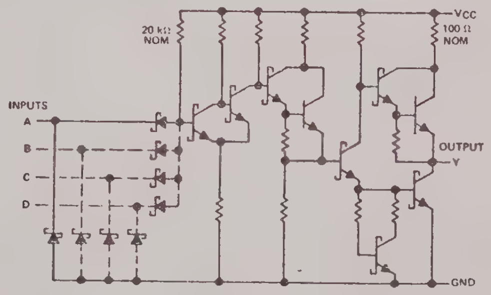
positive logic: $Y = \overline{A}$

## description

Each circuit functions as a NAND gate or inverter, but because of the Schmitt action, it has different input threshold levels for positive- and negative-going signals. The hysteresis or backlash, which is the difference between the two threshold levels, is typically 800 millivolts.

These circuits are temperature compensated and can be triggered from the slowest of input ramps and still give clean, jitter-free output signals.

## schematic (each gate)


VCC
20 kΩ NOM
100 Ω NOM
INPUTS
A
B
C
D
OUTPUT Y
GND

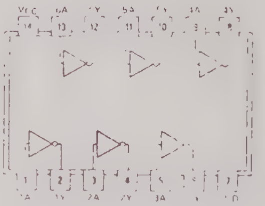
## TTL HEX INVERTER BUFFER W/OPEN COLLECTORS

SN7416N

S-D P/N 045230

HEX INVERTER BUFFERS/DRIVERS
WITH OPEN COLLECTOR
HIGH-VOLTAGE OUTPUTS

positive logic:
$Y = \bar{A}$


VCC
6A
6Y
5A
5Y
4A
4Y
14
13
12
11
10
9
8
1
2
3
4
5
6
7
1A
1Y
2A
2Y
3A
3Y
GND

SN5416/SN7416(J, N, W)

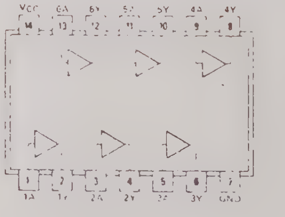
## TTL HEX BUFFER W/OPEN COLLECTORS

SN7417N

S-D P/N 106629

HEX BUFFERS/DRIVERS
WITH OPEN-COLLECTOR
HIGH-VOLTAGE OUTPUTS

positive logic:
$Y = A$


VCC
6A
6Y
5A
5Y
4A
4Y
14
13
12
11
10
9
8
1
2
3
4
5
6
7
1A
1Y
2A
2Y
3A
3Y
GND

SN5417/SN7417(J, N, W)

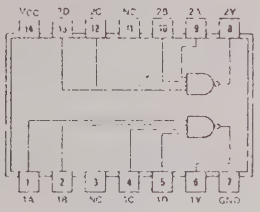
SN7420N
& SN74LS20N

## TTL DUAL 4-INPUT NAND GATES
## TTL DUAL 4-INPUT NAND GATES

S-D P/N 025713
S-D P/N 103969

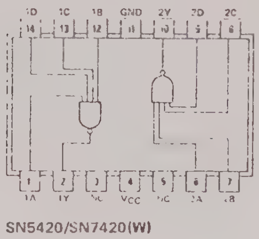
DUAL 4-INPUT
POSITIVE-NAND GATES

positive logic:
$Y = \overline{ABCD}$



VCC
2D
2C
NC
2B
2A
2Y
14
13
12
11
10
9
8
1
2
3
4
5
6
7
1A
1B
NC
1C
1D
1Y
GND

SN5420/SN7420(J, N)
SN54H20/SN74H20(J, N)
SN54L20/SN74L20(J, N)
SN54LS20/SN74LS20(J, N, W)
SN54S20/SN74S20(J, N, W)



1D
1C
1B
GND
2Y
2D
2C
14
13
12
11
10
9
8
1
2
3
4
5
6
7
1A
1Y
NC
VCC
NC
2A
2B

SN5420/SN7420(W)
SN54H20/SN74H20(W)
SN54L20/SN74L20(T)

NC -No internal connection

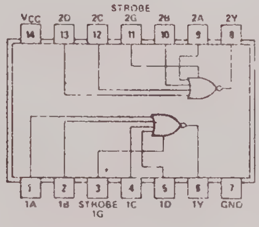
## TTL DUAL 4-INPUT NOR GATES W/STROBE

SN7425N

S-D P/N 045296

DUAL 4-INPUT
POSITIVE-NOR GATES
WITH STROBE

positive logic:
$Y = \overline{G(A+B+C+D)}$



STROBE
VCC
2D
2C
2G
2B
2A
2Y
14
13
12
11
10
9
8
1
2
3
4
5
6
7
1A
1B
STROBE
1G
1C
1D
1Y
GND

SN5425/SN7425 (J, N, W)

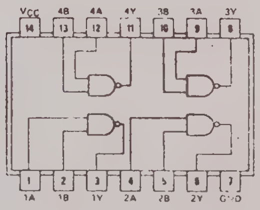
## TTL QUAD 2-INPUT HI VOLTAGE INTERFACE NAND GATES

SN7426N

S-D P/N 045252

QUADRUPLE 2-INPUT
HIGH-VOLTAGE INTERFACE
POSITIVE-NAND GATES

positive logic:
$Y = \overline{AB}$



VCC
4B
4A
4Y
3B
3A
3Y
14
13
12
11
10
9
8
1
2
3
4
5
6
7
1A
1B
1Y
2A
2B
2Y
GND

SN5426/SN7426(J, N)

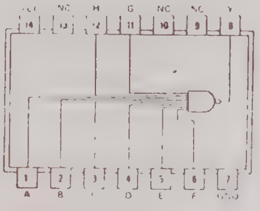
SN7430N
SN74LS30N

## TTL 8-INPUT NAND GATES
## TTL 8-INPUT NAND GATES

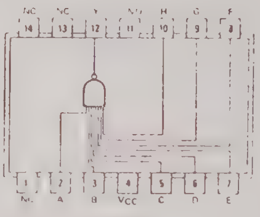
S-D P/N 025726
S-D P/N 103971

8-INPUT
POSITIVE-NAND GATES

positive logic:
$Y = \overline{ABCDEFGH}$


VCC
NC
H
G
NC
NC
Y
14
13
12
11
10
9
8
1
2
3
4
5
6
7
A
B
C
D
E
F
GND

SN5430/SN7430(J, N)
SN54H30/SN74H30(J, N)
SN54L30/SN74L30(J, N)
SN54LS30/SN74LS30(J, N, W)
SN54S30/SN74S30(J, N, W)


NC
NC
Y
NC
H
G
F
14
13
12
11
10
9
8
1
2
3
4
5
6
7
NC
A
B
VCC
C
D
E

SN5430/SN7430(W)
SN54H30/SN74H30(W)
SN54L30/SN74L30(T)

NC – No internal connection

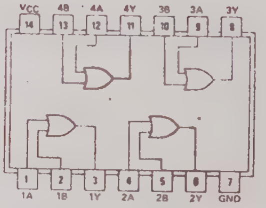
SN7432N
& SN74LS32N

## TTL QUAD 2-INPUT OR GATES
## TTL QUAD 2-INPUT OR GATES

S-D P/N 045257
S-D P/N 103972

QUADRUPLE 2-INPUT
POSITIVE-OR GATES

positive logic:
Y = A+B


VCC
4B
4A
4Y
3B
3A
3Y
14
13
12
11
10
9
8
1
2
3
4
5
6
7
1A
1B
1Y
2A
2B
2Y
GND

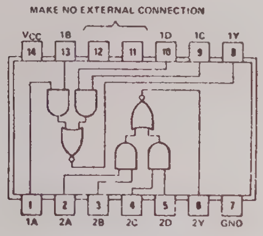
SN5432/SN7432(J, N, W)
SN54LS32/SN74LS32(J, N, W)

## TTL DUAL 2-WIDE 2-INPUT AND-OR-INVERT GATES

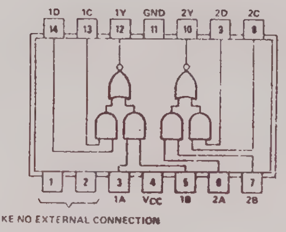
**SN7451N** S-D P/N 025707

**DUAL 2-WIDE 2-INPUT AND-OR-INVERT GATES**

'51, 'H51, 'S51
positive logic:
Y = $\overline{AB+CD}$

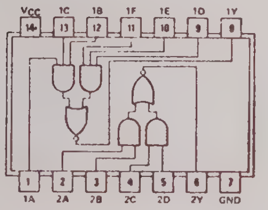

MAKE NO EXTERNAL CONNECTION
VCC
1B
1D
1C
1Y
14
13
12
11
10
9
8
1
2
3
4
5
6
7
1A
2A
2B
2C
2D
2Y
GND

SN5451/SN7451(J, N)
SN54H51/SN74H51(J, N)
SN54S51/SN74S51(J, N, W)

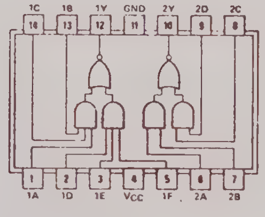

1D
1C
1Y
GND
2Y
2D
2C
14
13
12
11
10
9
8
1
2
3
4
5
6
7
1A
VCC
1B
2A
2B
MAKE NO EXTERNAL CONNECTION

SN5451/SN7451(W)
SN54H51/SN74H51(W)

'L51, 'LS51
positive logic:
1Y = $\overline{(1A\cdot 1B\cdot 1C)+(1D\cdot 1E\cdot 1F)}$
2Y = $\overline{(2A\cdot 2B)+(2C\cdot 2D)}$


VCC
1C
1B
1F
1E
1D
1Y
14
13
12
11
10
9
8
1
2
3
4
5
6
7
1A
2A
2B
2C
2D
2Y
GND

SN54L51/SN74L51(J, N)
SN54LS51/SN74LS51(J, N, W)


1C
1B
1Y
GND
2Y
2D
2C
14
13
12
11
10
9
8
1
2
3
4
5
6
7
1A
1D
1E
VCC
1F
2A
2B

SN54L51/SN74L51(T)

---

**SN7474N**
**SN74LS74N**

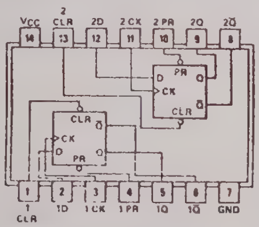
## TTL DUAL D TYPE FLIP-FLOPS
## TTL DUAL D TYPE FLIP-FLOPS

S-D P/N 025241
S-D P/N 103132

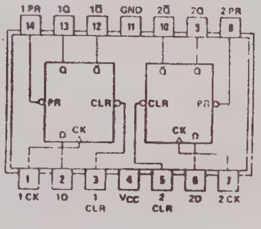
### DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

FUNCTION TABLE

| INPUTS | | | | OUTPUTS | |
|---|---|---|---|---|---|
| PRESET | CLEAR | CLOCK | D | Q | $\overline{Q}$ |
| L | H | X | X | H | L |
| H | L | X | X | L | H |
| L | L | X | X | H* | H* |
| H | H | ↑ | H | H | L |
| H | H | ↑ | L | L | H |
| H | H | L | X | $Q_0$ | $\overline{Q}_0$ |


VCC
2 CLR
2D
2 CK
2 PR
2Q
2Q̄
14
13
12
11
10
9
8
D
CK
PR
Q
Q̄
CLR
1
2
3
4
5
6
7
1 CLR
1D
1 CK
1 PR
1Q
1Q̄
GND

SN5474/SN7474(J, N)
SN54H74/SN74H74(J, N)
SN54L74/SN74L74(J, N)
SN54LS74/SN74LS74(J, N, W)
SN54S74/SN74S74(J, N, W)


1 PR
1Q
1Q̄
GND
2Q̄
2Q
2 PR
14
13
12
11
10
9
8
Q
Q̄
PR
CLR
D
CK
1
2
3
4
5
6
7
1 CK
1D
1 CLR
VCC
2 CLR
2D
2 CK

SN5474/SN7474(W)
SN54H74/SN74H74(W)
SN54L74/SN74L74(T)

---

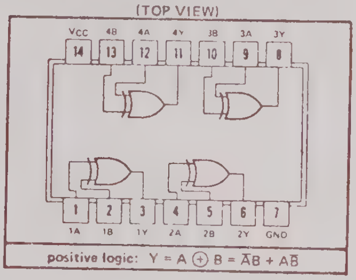
H = high level (steady state), L = low level (steady state), X = irrelevant
⎍ = high-level pulse; data inputs should be held constant while clock is high; data is transferred to output on the falling edge of the pulse.
↑ = transition from low to high level, ↓ = transition from high to low level
$Q_0$ = the level of Q before the indicated input conditions were established.
TOGGLE: Each output changes to the complement of its previous level on each active transition (pulse) of the clock.
*This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

# QUADRUPLE 2-INPUT EXCLUSIVE-OR GATE

SN74LS86

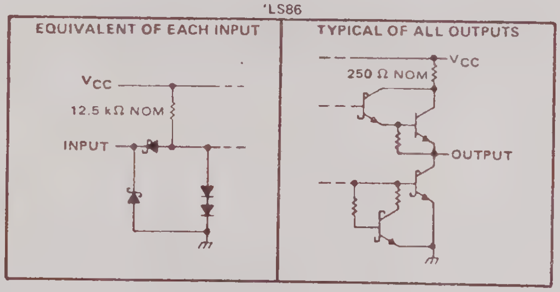
S-D P/N 103975

SN54', SN54LS', SN54S' . . . J OR W PACKAGE
SN74', SN74LS', SN74S' . . . J OR N PACKAGE
(TOP VIEW)


VCC 4B 4A 4Y 3B 3A 3Y
14 13 12 11 10 9 8
1 2 3 4 5 6 7
1A 1B 1Y 2A 2B 2Y GND

positive logic: $Y = A \oplus B = \overline{A}B + A\overline{B}$

'LS86


EQUIVALENT OF EACH INPUT
VCC
12.5 kΩ NOM
INPUT
TYPICAL OF ALL OUTPUTS
VCC
250 Ω NOM
OUTPUT

## TTL MONOSTABLE MULTIVIBRATOR WITH SCHMITT TRIGGER INPUT

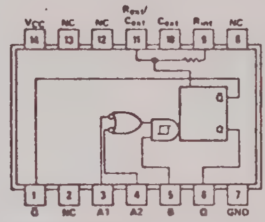
SN74121N S-D P/N 025786

### MONOSTABLE MULTIVIBRATORS

FUNCTION TABLE

| INPUTS | | | OUTPUTS | |
|---|---|---|---|---|
| A1 | A2 | B | Q | $\bar{Q}$ |
| L | X | H | L | H |
| X | L | H | L | H |
| X | X | L | L | H |
| H | H | X | L | H |
| H | ↓ | H | ⊓ | ⊔ |
| ↓ | H | H | ⊓ | ⊔ |
| ↓ | ↓ | H | ⊓ | ⊔ |
| L | X | ↑ | ⊓ | ⊔ |
| X | L | ↑ | ⊓ | ⊔ |

See Notes


$V_{CC}$
NC
NC
$R_{ext}$/$C_{ext}$
$C_{ext}$
$R_{int}$
NC
14
13
12
11
10
9
8
Q
$\bar{Q}$
1
2
3
4
5
6
7
$\bar{Q}$
NC
A1
A2
B
Q
GND

SN54121/SN74121(J, N, W)
SN54L121/SN74L121(J, N, T)
'121 . . . $R_{int}$ = 2 kΩ NOM
'L121 . . . $R_{int}$ = 4 kΩ NOM

NC—No internal connection

## TTL RETRIGGERABLE MONOSTABLE MULTIVIRATOR WITH CLEAR

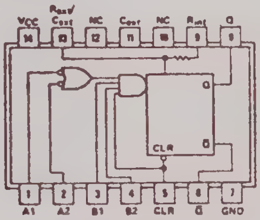
SN74122N S-D P/N 117392

### RETRIGGERABLE MONOSTABLE MULTIVIBRATORS WITH CLEAR

FUNCTION TABLE

| INPUTS | | | | | OUTPUTS | |
|---|---|---|---|---|---|---|
| CLEAR | A1 | A2 | B1 | B2 | Q | $\bar{Q}$ |
| L | X | X | X | X | L | H |
| X | H | H | X | X | L | H |
| X | X | X | L | X | L | H |
| X | X | X | X | L | L | H |
| X | L | X | H | H | L | H |
| H | L | X | ↑ | H | ⊓ | ⊔ |
| H | L | X | H | ↑ | ⊓ | ⊔ |
| H | X | L | H | H | L | H |
| H | X | L | ↑ | H | ⊓ | ⊔ |
| H | X | L | H | ↑ | ⊓ | ⊔ |
| H | H | ↓ | H | H | ⊓ | ⊔ |
| H | ↓ | ↓ | H | H | ⊓ | ⊔ |
| H | ↓ | H | H | H | ⊓ | ⊔ |
| ↑ | L | X | H | H | ⊓ | ⊔ |
| ↑ | X | L | H | H | ⊓ | ⊔ |

See Notes


$V_{CC}$
$R_{ext}$/$C_{ext}$
NC
$C_{ext}$
NC
$R_{int}$
Q
14
13
12
11
10
9
8
Q
$\bar{Q}$
CLR
1
2
3
4
5
6
7
A1
A2
B1
B2
CLR
$\bar{Q}$
GND

SN54122/SN74122(J, N, W)
SN54L122/SN74L122(J, N, T)
'122 . . . $R_{int}$ = 10 kΩ NOM
'L122 . . . $R_{int}$ = 20 kΩ NOM

NC—No internal connection

## TTL DUAL RETRIGGERABLE MONOSTABLE MULTIVIBRATOR WITH CLEAR

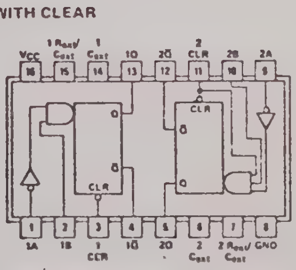
SN74123N S-D P/N 045209
SN74LS123 S-D P/N 103976

### DUAL RETRIGGERABLE MONOSTABLE MULTIVIBRATORS WITH CLEAR

FUNCTION TABLE

| INPUTS | | | OUTPUTS | |
|---|---|---|---|---|
| CLEAR | A | B | Q | $\bar{Q}$ |
| L | X | X | L | H |
| X | H | X | L | H |
| X | X | L | L | H |
| H | L | ↑ | ⊓ | ⊔ |
| H | ↓ | H | ⊓ | ⊔ |
| ↑ | L | H | ⊓ | ⊔ |

See Notes


$V_{CC}$
1 $R_{ext}$/$C_{ext}$
1 $C_{ext}$
1Q
2$\bar{Q}$
2 CLR
2B
2A
16
15
14
13
12
11
10
9
Q
$\bar{Q}$
CLR
$\bar{Q}$
Q
CLR
1
2
3
4
5
6
7
8
1A
1B
1 CLR
1$\bar{Q}$
2Q
2 $C_{ext}$
2 $R_{ext}$/$C_{ext}$
GND

SN54123/SN74123(J, N, W)
SN54L123/SN74L123(J, N)

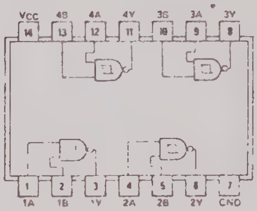
## TTL QUAD 2-INPUT NAND SCHMITT TRIGGERS

SN74132N

S-D P/N 045270

QUADRUPLE 2-INPUT
POSITIVE-NAND
SCHMITT TRIGGERS

positive logic:
$Y = \overline{AB}$


VCC
4B
4A
4Y
3B
3A
3Y
14
13
12
11
10
9
8
1
2
3
4
5
6
7
1A
1B
1Y
2A
2B
2Y
GND

SN54132/SN74132(J, N, W)
SN54S132/SN74S132(J, N, W)

---

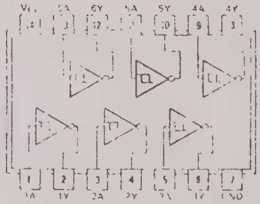
## TTL HEX SCHMITT TRIGGER BUFFERS

SN74LS14N

S-D P/N 117083

HEX SCHMITT-TRIGGER
INVERTERS

positive logic:
$Y = \overline{A}$


VCC
6A
6Y
5A
5Y
4A
4Y
14
13
12
11
10
9
8
1
2
3
4
5
6
7
1A
1Y
2A
2Y
3A
3Y
GND

SN5414/SN7414(J, N, W)

# TTL BCD-TO-DECIMAL DECODER/DRIVERS

SN74145N

S-D P/N 025754

## TYPES SN54145, SN74145
## BCD-TO-DECIMAL DECODER/DRIVERS

### FOR USE AS LAMP, RELAY, OR MOS DRIVERS

**featuring**

- Full Decoding of Input Logic
- 80-mA Sink-Current Capability
- All Outputs Are Off for Invalid BCD Input Conditions

### logic

FUNCTION TABLE

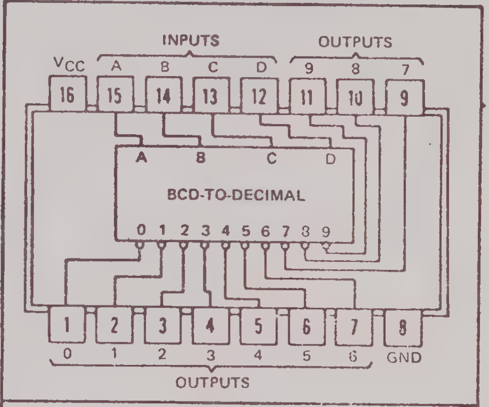
| NO. | INPUTS | | | | OUTPUTS | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | D | C | B | A | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 |
| 0 | L | L | L | L | L | H | H | H | H | H | H | H | H | H |
| 1 | L | L | L | H | H | L | H | H | H | H | H | H | H | H |
| 2 | L | L | H | L | H | H | L | H | H | H | H | H | H | H |
| 3 | L | L | H | H | H | H | H | L | H | H | H | H | H | H |
| 4 | L | H | L | L | H | H | H | H | L | H | H | H | H | H |
| 5 | L | H | L | H | H | H | H | H | H | L | H | H | H | H |
| 6 | L | H | H | L | H | H | H | H | H | H | L | H | H | H |
| 7 | L | H | H | H | H | H | H | H | H | H | H | L | H | H |
| 8 | H | L | L | L | H | H | H | H | H | H | H | H | L | H |
| 9 | H | L | L | H | H | H | H | H | H | H | H | H | H | L |
| INVALID | H | L | H | L | H | H | H | H | H | H | H | H | H | H |
| | H | L | H | H | H | H | H | H | H | H | H | H | H | H |
| | H | H | L | L | H | H | H | H | H | H | H | H | H | H |
| | H | H | L | H | H | H | H | H | H | H | H | H | H | H |
| | H | H | H | L | H | H | H | H | H | H | H | H | H | H |
| | H | H | H | H | H | H | H | H | H | H | H | H | H | H |

H = high level (off), L = low level (on)

### description

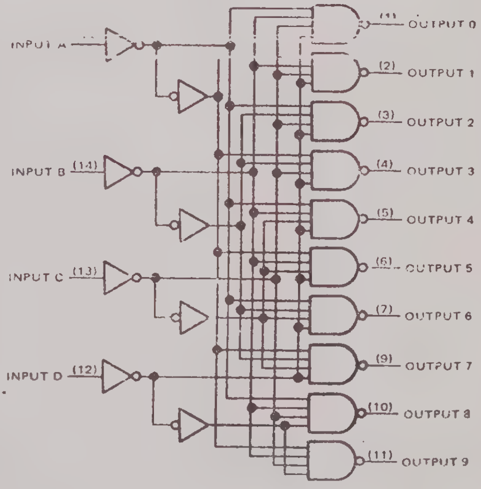
These monolithic BCD-to-decimal decoder/drivers consist of eight inverters and ten four-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. Full decoding of valid BCD input logic ensures that all outputs remain off for all invalid binary input conditions. These decoders feature TTL inputs and high-performance, n-p-n output transistors designed for use as indicator/relay drivers or as open-collector logic-circuit drivers. Each of the high-breakdown output transistors (15 volts) will sink up to 80 milliamperes of current. Each input is one normalized Series 54/74 load. Inputs and outputs are entirely compatible for use with TTL or DTL logic circuits, and the outputs are compatible for interfacing with most MOS integrated circuits. Power dissipation is typically 215 milliwatts.

J OR N DUAL-IN-LINE OR
W FLAT PACKAGE (TOP VIEW)


INPUTS
OUTPUTS
VCC
A
B
C
D
9
8
7
16
15
14
13
12
11
10
9
A
B
C
D
BCD-TO-DECIMAL
0 1 2 3 4 5 6 7 8 9
1
2
3
4
5
6
7
8
0
1
2
3
4
5
6
GND
OUTPUTS

positive logic: see function table

### functional block diagram


INPUT A
INPUT B (14)
INPUT C (13)
INPUT D (12)
(1) OUTPUT 0
(2) OUTPUT 1
(3) OUTPUT 2
(4) OUTPUT 3
(5) OUTPUT 4
(6) OUTPUT 5
(7) OUTPUT 6
(9) OUTPUT 7
(10) OUTPUT 8
(11) OUTPUT 9

# TTL 16-TO-1 DATA SELECTORS/MULTIPLEXERS

SN74150N

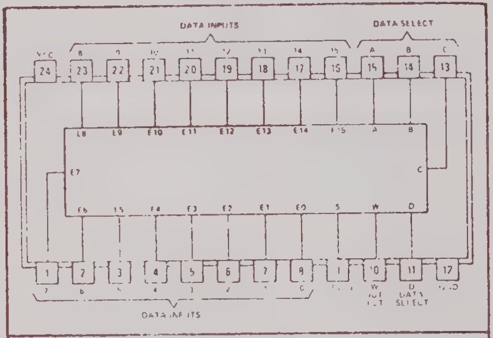
S-D P/N 106637

- '150 Selects One-of-Sixteen Data Sources
- Others Select One-of-Eight Data Sources
- Performs Parallel-to-Serial Conversion
- Permits Multiplexing from N Lines to One Line
- Also For Use as Boolean Function Generator
- Input-Clamping Diodes Simplify System Design
- Fully Compatible with Most TTL and DTL Circuits

| TYPE | TYPICAL AVERAGE PROPAGATION DELAY TIME DATA INPUT TO W OUTPUT | TYPICAL POWER DISSIPATION |
|---|---|---|
| '150 | 11 ns | 200 mW |
| '151A | 8 ns | 145 mW |
| '152A | 8 ns | 130 mW |
| 'LS151 | 11 ns† | 30 mW |
| 'LS152 | 11 ns† | 28 mW |
| 'S151 | 4.5 ns | 225 mW |

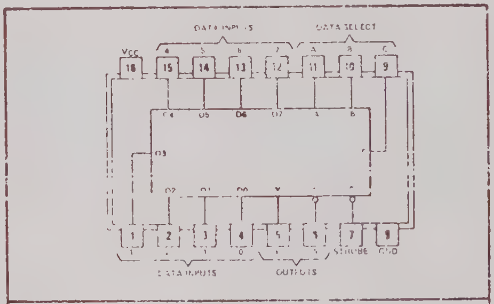
† Tentative data

'150
J OR N DUAL-IN-LINE OR
W FLAT PACKAGE (TOP VIEW)


DATA INPUTS
DATA SELECT
VCC
A
B
C
D
W
STROBE
GND
W OUTPUT
DATA SELECT
DATA INPUTS

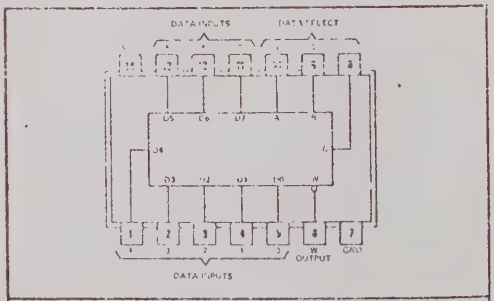
positive logic: see function table

'151A, 'LS151, 'S151
J OR N DUAL-IN-LINE OR
W FLAT PACKAGE (TOP VIEW)


DATA INPUTS
DATA SELECT
VCC
A
B
C
STROBE
GND
DATA INPUTS
OUTPUTS

positive logic: see function table

'152A, 'LS152
W FLAT PACKAGE
(TOP VIEW)


DATA INPUTS
DATA SELECT
W OUTPUT
GND
DATA INPUTS

positive logic: see function table

## description

These monolithic data selectors/multiplexers contain full on-chip binary decoding to select the desired data source. The '150 selects one-of-sixteen data sources; the '151A, '152A, 'LS151, 'LS152, and 'S151 select one-of-eight data sources. The '150, '151A, 'LS151, and 'S151 have a strobe input which must be at a low logic level to enable these devices. A high level at the strobe forces the W output high, and the Y output (as applicable) low.

The '151A, 'LS151, and 'S151 feature complementary W and Y outputs whereas the '150, '152A, and 'LS152 have an inverted (W) output only.

The '151A and '152A incorporate address buffers which have symmetrical propagation delay times through the complementary paths. This reduces the possibility of transients occurring at the output(s) due to changes made at the select inputs, even when the '151A outputs are enabled (i.e., strobe low).

# TYPES SN54150, SN54151A, SN54152A, SN54LS151, SN54LS152, SN54S151, SN74150, SN74151A, SN74152A, SN74LS151, SN74LS152, SN74S151 DATA SELECTORS/MULTIPLEXERS

## logic

'150

FUNCTION TABLE

| INPUTS | | | | | OUTPUT |
|---|---|---|---|---|---|
| SELECT | | | | STROBE | W |
| D | C | B | A | S | |
| X | X | X | X | H | H |
| L | L | L | L | L | $\overline{E0}$ |
| L | L | L | H | L | $\overline{E1}$ |
| L | L | H | L | L | $\overline{E2}$ |
| L | L | H | H | L | $\overline{E3}$ |
| L | H | L | L | L | $\overline{E4}$ |
| L | H | L | H | L | $\overline{E5}$ |
| L | H | H | L | L | $\overline{E6}$ |
| L | H | H | H | L | $\overline{E7}$ |
| H | L | L | L | L | $\overline{E8}$ |
| H | L | L | H | L | $\overline{E9}$ |
| H | L | H | L | L | $\overline{E10}$ |
| H | L | H | H | L | $\overline{E11}$ |
| H | H | L | L | L | $\overline{E12}$ |
| H | H | L | H | L | $\overline{E13}$ |
| H | H | H | L | L | $\overline{E14}$ |
| H | H | H | H | L | $\overline{E15}$ |

'151A, 'LS151, 'S151

FUNCTION TABLE

| INPUTS | | | | OUTPUTS | |
|---|---|---|---|---|---|
| SELECT | | | STROBE | Y | W |
| C | B | A | S | | |
| X | X | X | H | L | H |
| L | L | L | L | D0 | $\overline{D0}$ |
| L | L | H | L | D1 | $\overline{D1}$ |
| L | H | L | L | D2 | $\overline{D2}$ |
| L | H | H | L | D3 | $\overline{D3}$ |
| H | L | L | L | D4 | $\overline{D4}$ |
| H | L | H | L | D5 | $\overline{D5}$ |
| H | H | L | L | D6 | $\overline{D6}$ |
| H | H | H | L | D7 | $\overline{D7}$ |

'152A, 'LS152

FUNCTION TABLE

| SELECT INPUTS | | | OUTPUT |
|---|---|---|---|
| C | B | A | W |
| L | L | L | $\overline{D0}$ |
| L | L | H | $\overline{D1}$ |
| L | H | L | $\overline{D2}$ |
| L | H | H | $\overline{D3}$ |
| H | L | L | $\overline{D4}$ |
| H | L | H | $\overline{D5}$ |
| H | H | L | $\overline{D6}$ |
| H | H | H | $\overline{D7}$ |

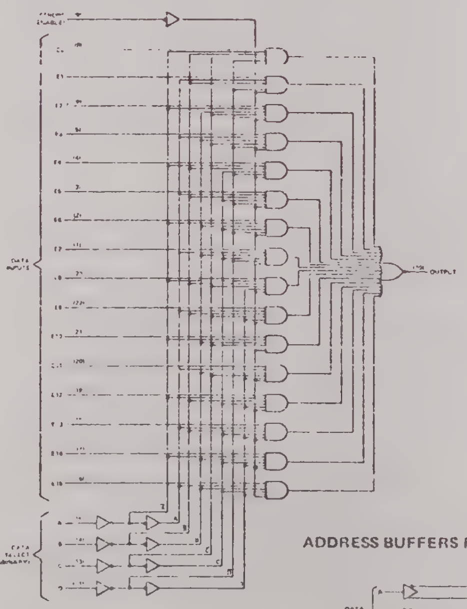
H = high level, L = low level, X = irrelevant

$\overline{E0}$, $\overline{E1}$ . . . $\overline{E15}$ = the complement of the level of the respective E input

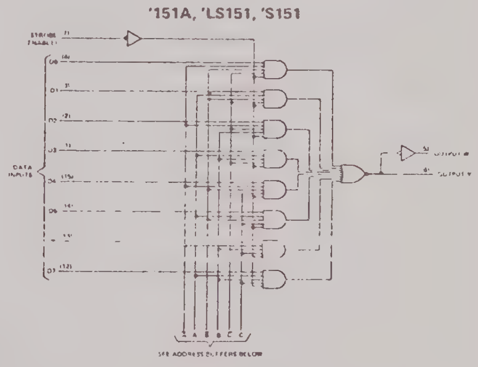
D0, D1 . . . D7 = the level of the D respective input

## functional block diagrams

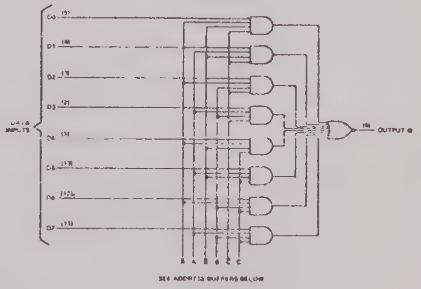
'150


STROBE (ENABLE)
DATA INPUTS
OUTPUT
DATA SELECT (BINARY)
A
B
C
D

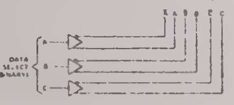
'151A, 'LS151, 'S151


STROBE (ENABLE)
D0
D1
D2
D3
D4
D5
D6
D7
DATA INPUTS
OUTPUT Y
OUTPUT W
SEE ADDRESS BUFFERS BELOW

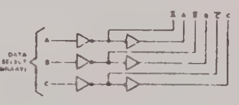
'152A, 'LS152


D0
D1
D2
D3
D4
D5
D6
D7
DATA INPUTS
OUTPUT W
SEE ADDRESS BUFFERS BELOW

ADDRESS BUFFERS FOR '151A, '152A


DATA SELECT (BINARY)
A
B
C

ADDRESS BUFFERS FOR 'LS151, 'S151, 'LS152


DATA SELECT (BINARY)
A
B
C

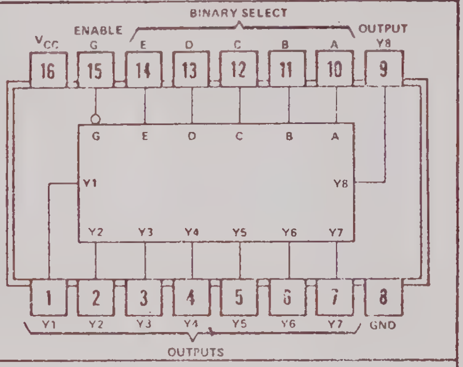
## TTL 256 BIT PROGRAMMABLE ROM

SN74188N S-D P/N 055123

# TYPE SN74188A
# 256-BIT PROGRAMMABLE READ-ONLY MEMORY

- Field Programmable for Custom or Prototype Memories
- Mask-Programmable SN7488A is a Direct Replacement for the SN74188A
- Typical Access Time . . . 30 ns
- Organized as 32 Words of 8 Bits Each
- Ideal for Microprogramming and Code Converters
- Open-Collector Outputs are Easily Expanded
- Fully-Decoded Buffered Inputs
- Fully Compatible with Most TTL and DTL Circuits

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



logic: see description

## description

The SN74188A is a field-programmable, 256-bit, read-only memory organized as 32 words of eight bits each. This monolithic, high-speed, transistor-transistor-logic (TTL) memory array is addressed in five bit binary with full on-chip decoding. An overriding memory-enable input is provided which, when taken high, will inhibit the function causing all eight outputs to remain high. The organization is expandable to 1,856 words of n-bits with no additional output buffering.

The address of an eight-bit word is accomplished through the buffered binary select inputs in coincidence with a low logic level at the enable input. Where multiple SN74188A devices are used in a memory system, the enable input allows easy decoding of additional address bits.

Data can be electronically programmed, as desired, at any of the 256 bit locations of the SN74188A in accordance with the programming procedure specified. Prior to programming, the memory contains a low-logic-level output condition at all 256 bit locations. The programming procedure open-circuits metal links which results in a high-logic-level output at selected locations. The procedure is irreversible and, once altered, the output for that bit is permanently programmed to provide a high logic level. Outputs never having been altered may later be programmed to supply a high-level output. Operation of the unit within the recommended operating conditions will not alter the memory content.

The open-collector outputs are capable of sinking 12 milliamperes of current and may be wire-AND-connected to other memories to increase the number of words without additional output buffering. External pull-up resistors should be used to improve noise margin and dynamic response. The best low-to-high propagation delay time is achieved when using minimum $R_L$ (see Table 1).

The mask-programmable SN7488A can be used to replace the SN74188A as they are functionally and mechanically identical. Likewise, most applications currently using the SN7488A can utilize the SN74188A as a direct replacement where field programming is desired.

TABLE 1
WORD CAPACITY vs TTL LOADS
($V_{CC}$ = 5 V, $T_A$ = 0°C to 70°C)

| LOADS | MIN $R_L$ (Ω) | MAX NO. WIRE-ANDS† | MAX NO. OF WORDS |
|---|---|---|---|
| 1 | 442 | 58 | 1856 |
| 2 | 522 | 49 | 1568 |
| 3 | 639 | 39 | 1248 |
| 4 | 821 | 30 | 960 |
| 5 | 1150 | 20 | 640 |
| 6 | 1916 | 10 | 320 |
| 7 | 5750 | 2 | 64 |

† Total number of SN74188A outputs connected to each common bus.

## TYPE SN74188A
## 256-BIT PROGRAMMABLE READ-ONLY MEMORY

### step-by-step programming procedure

1. Apply steady-state supply voltage ($V_{CC}$ = 5 V) and address the word to be programmed with specified input voltage levels.
2. Disable the outputs by applying a high-logic-level voltage to the enable input.
3. Only one bit location is programmed at a time. Open-circuit all outputs except the one to be programmed as a high logic level. Apply −0.7 V to the output to be programmed.
4. Apply the program pulse ($V_{CC}$ = 10 V) and after the 10-volt level is achieved, enable the outputs (enable low). The 10-volt level and the enabling of the outputs should occur within the first 10 milliseconds of the program pulse. Disable the outputs (enable high) prior to removing the program pulse. (See Figure 1). The power supply must be capable of supplying 100 milliamperes at 10 volts.
5. Repeat steps 2 through 4 for each output of this address to be programmed as a high level.
6. Address next location and repeat steps 2 through 5.

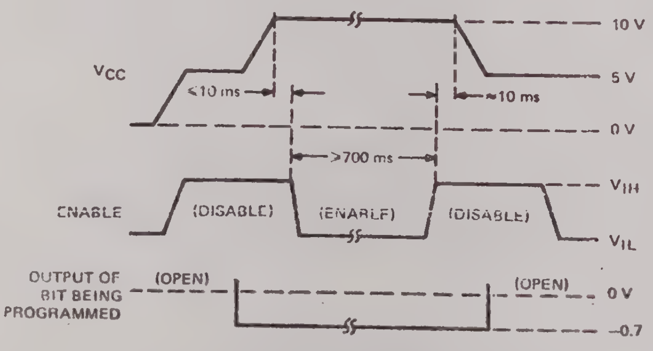
### recommended conditions for programming

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Supply voltage, $V_{CC}$ (see Note 1) | Steady state | 0 | 5 | 5.5 | V |
| | Program pulse | 9 | 10 | 11† | |
| Input voltage | Low level | | | 0.5 | V |
| | High level | 2.4 | | 5 | |
| Output conditions for programming | To a low logic level | Open circuit | | | V |
| | To a high logic level | −0.6 | | −0.8 | |
| Duration of programming pulse (see Note 2) | | 700 | | | ms |
| Case temperature (see Note 3) | | | | 75 | °C |

NOTES: 1. All voltage values are with respect to network ground terminal.
2. Programming is guaranteed if the pulse is applied for 700 ms. Typically, programming occurs in less than 200 ms.
3. This refers to the temperature measured at the center of the bottom of the case.

† Absolute maximum rating.

### programming pulses

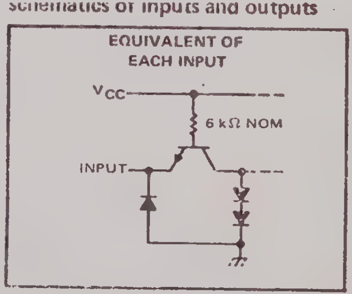


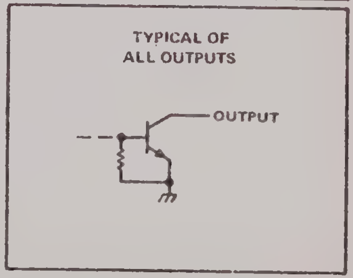
VOLTAGE WAVEFORMS

Location to be programmed must be addressed prior to enabling. Repeat pulses for each output at this address which is to be programmed to a high logic level.

FIGURE 1

### schematics of inputs and outputs





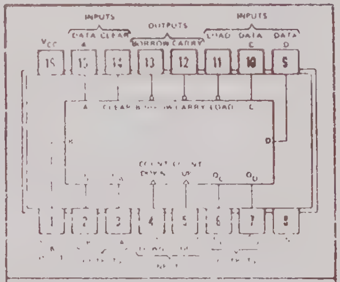
SN74LS192N TTL SYNCHRONOUS BCD UP/DOWN COUNTER S-D P/N 103106
& SN74LS193N TTL SYNCHRONOUS 4-BIT BINARY UP/DOWN COUNTER S-D P/N 103162

# TYPES SN54192, SN54193, SN54L192, SN54L193, SN54LS192, SN54LS193 SN74192, SN74193, SN74L192, SN74L193, SN74LS192, SN74LS193 SYNCHRONOUS 4-BIT UP/DOWN COUNTERS (DUAL CLOCK WITH CLEAR)

- Cascading Circuitry Provided Internally
- Synchronous Operation
- Individual Preset to Each Flip Flop
- Fully Independent Clear Input

| TYPES | TYPICAL MAXIMUM COUNT FREQUENCY | TYPICAL POWER DISSIPATION |
|---|---|---|
| '192, '193 | 32 MHz | 325 mW |
| 'L192, 'L193 | 7 MHz | 43 mW |
| 'LS192, 'LS193 | 32 MHz | 85 mW |

192, '193 . . . J, N, OR W PACKAGE
'L192, 'L193 . . . J OR N PACKAGE
'LS192, 'LS193 . . . J, N, OR W PACKAGE
(TOP VIEW)



logic: Low input to load sets $Q_A = A$, $Q_B = B$, $Q_C = C$, and $Q_D = D$

## description

These monolithic circuits are synchronous reversible (up/down) counters having a complexity of 55 equivalent gates. The '192, 'L192, and 'LS192 circuits are BCD counters and the '193, 'L193 and 'LS193 are 4 bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincidently with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple-clock) counters.

The outputs of the four master-slave flip-flops are triggered by a low-to-high-level transition of either count (clock) input. The direction of counting is determined by which count inputs is pulsed while the other count input is high.

All four counters are fully programmable; that is, each output may be preset to either level by entering the desired data at the data inputs while the load input is low. The output will change to agree with the data inputs independently of the count pulses. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

A clear input has been provided which forces all outputs to the low level when a high level is applied. The clear function is independent of the count and load inputs. The clear, count, and load inputs are buffered to lower the drive requirements. This reduces the number of clock drivers, etc., required for long words.

These counters were designed to be cascaded without the need for external circuitry. Both borrow and carry outputs are available to cascade both the up- and down-counting functions. The borrow output produces a pulse equal in width to the count-down input when the counter underflows. Similarly, the carry output produces a pulse equal in width to the count-down input when an overflow condition exists. The counters can then be easily cascaded by feeding the borrow and carry outputs to the count-down and count-up inputs respectively of the succeeding counter.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

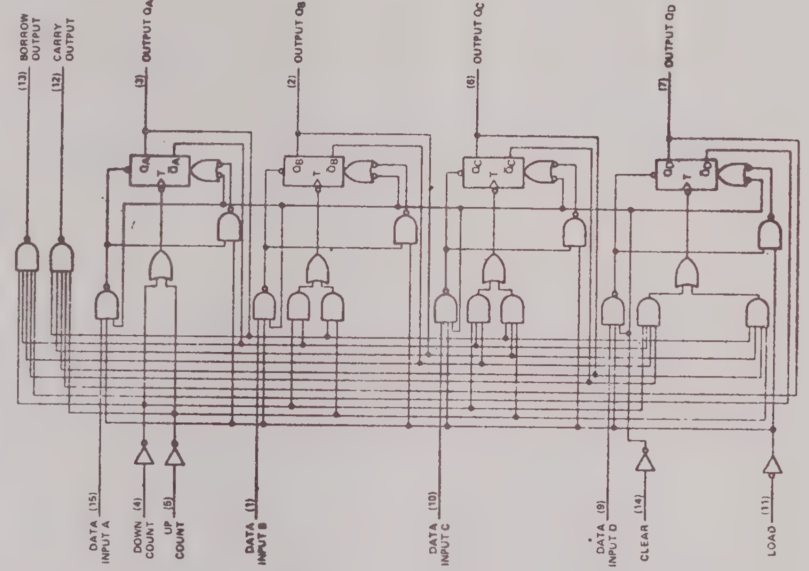
| | SN54' | SN54L' | SN54LS' | SN74' | SN74L' | SN74LS' | UNIT |
|---|---|---|---|---|---|---|---|
| Supply voltage, $V_{CC}$ (see Note 1) | 7 | 8 | 7 | 7 | 8 | 7 | V |
| Input voltage | 5.5 | 5.5 | 7 | 5.5 | 5.5 | 7 | V |
| Operating free-air temperature range | –55 to 125 | | | 0 to 70 | | | °C |
| Storage temperature range | –65 to 150 | | | –65 to 150 | | | °C |

NOTE 1: Voltage values are with respect to network ground terminal.

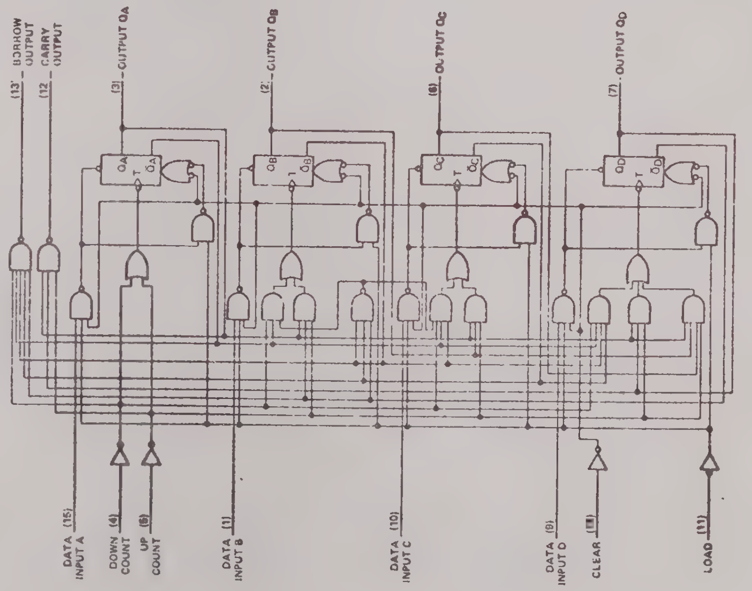
# TTL SYNCHRONOUS BCD UP/DOWN COUNTER
# TTL SYNCHRONOUS 4-BIT BINARY UP/DOWN COUNTER
## (CONT)

functional block diagrams

'193, 'L193, 'LS193


(13) BORROW OUTPUT
(12) CARRY OUTPUT
(3) OUTPUT QA
(2) OUTPUT QB
(6) OUTPUT QC
(7) OUTPUT QD
QA
T
Q̄A
QB
Q̄B
QC
Q̄C
QD
Q̄D
DATA INPUT A (15)
DOWN COUNT (4)
UP COUNT (5)
DATA INPUT B (1)
DATA INPUT C (10)
DATA INPUT D (9)
CLEAR (14)
LOAD (11)

'192, 'L192, 'LS192


(13) BORROW OUTPUT
(12) CARRY OUTPUT
(3) OUTPUT QA
(2) OUTPUT QB
(6) OUTPUT QC
(7) OUTPUT QD
QA
T
Q̄A
QB
Q̄B
QC
Q̄C
QD
Q̄D
DATA INPUT A (15)
DOWN COUNT (4)
UP COUNT (5)
DATA INPUT B (1)
DATA INPUT C (10)
DATA INPUT D (9)
CLEAR (14)
LOAD (11)

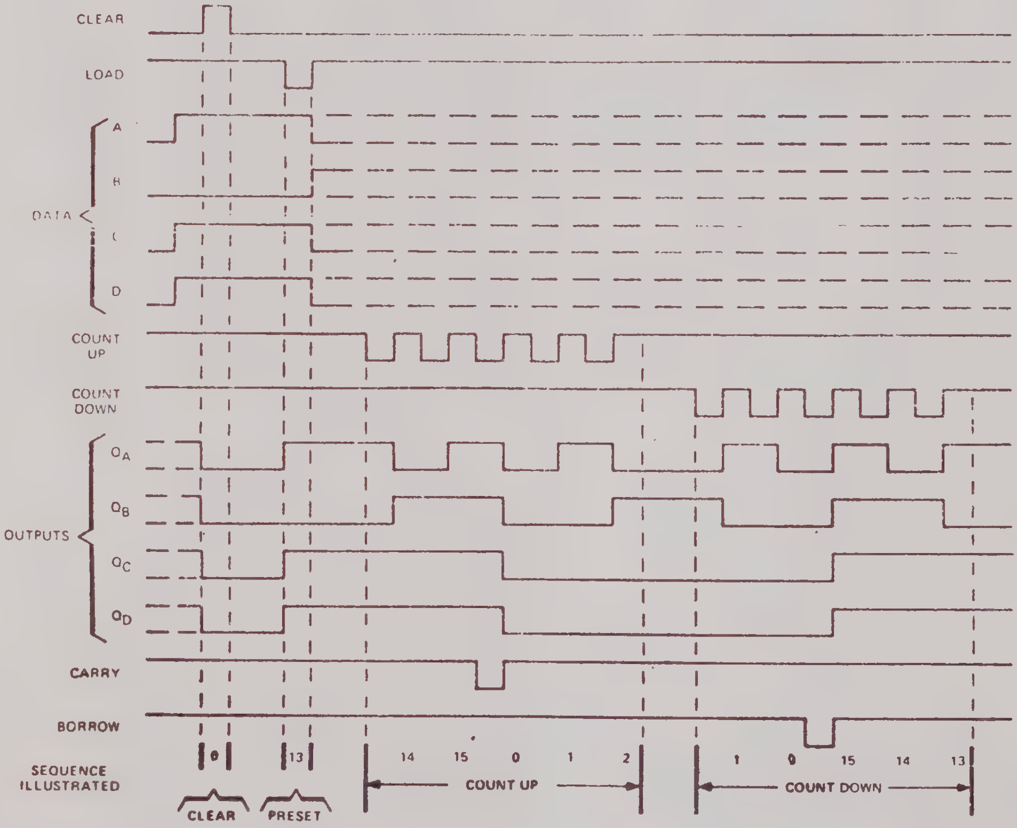
⊳. . . Dynamic input activated by a transition from a high level to a low level

## '193, 'L193, 'LS193 BINARY COUNTERS

### typical clear, load, and count sequences

Illustrated below is the following sequence:

1. Clear outputs to zero.
2. Load (preset) to binary thirteen.
3. Count up to fourteen, fifteen, carry, zero, one, and two.
4. Count down to one, zero, borrow, fifteen, fourteen, and thirteen.


CLEAR
LOAD
DATA
A
B
C
D
COUNT UP
COUNT DOWN
OUTPUTS
$Q_A$
$Q_B$
$Q_C$
$Q_D$
CARRY
BORROW
SEQUENCE ILLUSTRATED
0
13
14
15
0
1
2
COUNT UP
1
0
15
14
13
COUNT DOWN
CLEAR
PRESET

NOTES: A. Clear overrides load, data, and count inputs.

B. When counting up, count-down input must be high; when counting down, count-up input must be high.

SN74LS192N
& SN74LS193N

## TTL SYNCHRONOUS BCD UP/DOWN COUNTER
## TTL SYNCHRONOUS 4-BIT BINARY UP/DOWN COUNTER
## (CONT)

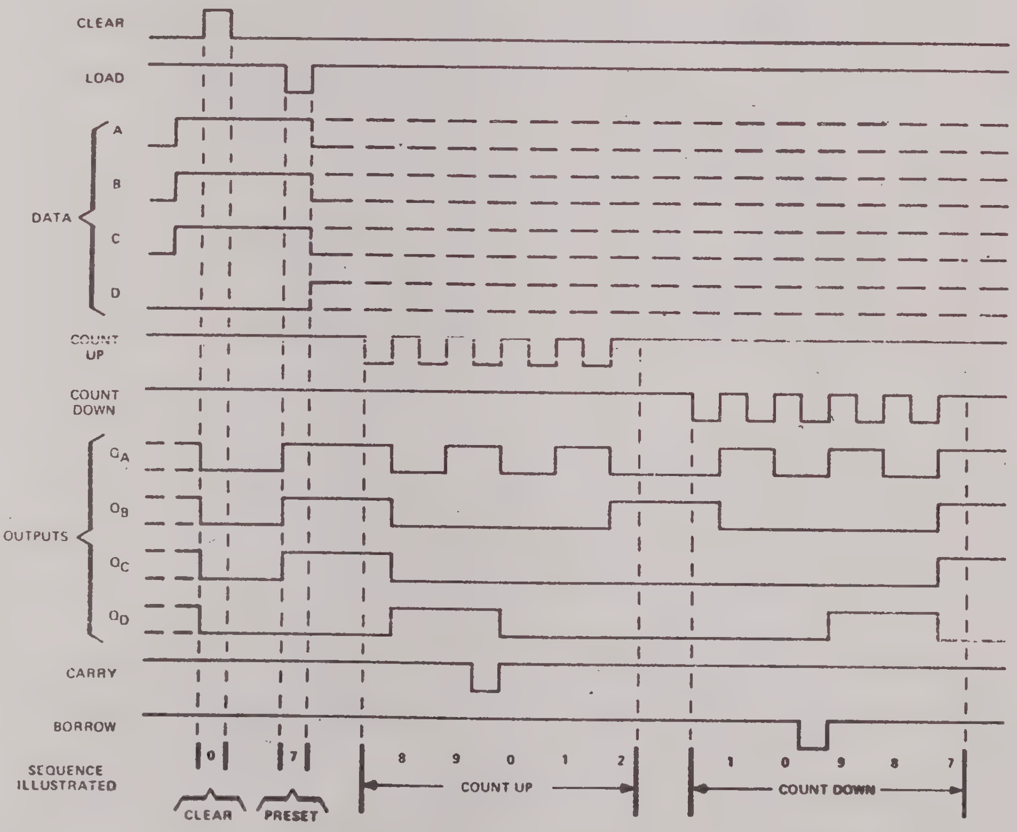
S-D P/N 103106
S-D P/N 103162

### '192,'L192, 'LS192 DECADE COUNTERS

**typical clear, load, and count sequences**

Illustrated below is the following sequence:

1. Clear outputs to zero.
2. Load (preset) to BCD seven.
3. Count up to eight, nine, carry, zero, one, and two.
4. Count down to one, zero, borrow, nine, eight, and seven.


CLEAR
LOAD
A
B
DATA
C
D
COUNT UP
COUNT DOWN
$Q_A$
$Q_B$
OUTPUTS
$Q_C$
$Q_D$
CARRY
BORROW
SEQUENCE ILLUSTRATED
0
7
8
9
0
1
2
COUNT UP
1
0
9
8
7
COUNT DOWN
CLEAR
PRESET

NOTES: A. Clear overrides load, data, and count inputs.
B. When counting up, count-down input must be high; when counting down, count-up input must be high.

# TTL 4-BIT PARALLEL-ACCESS SHIFT REGISTER

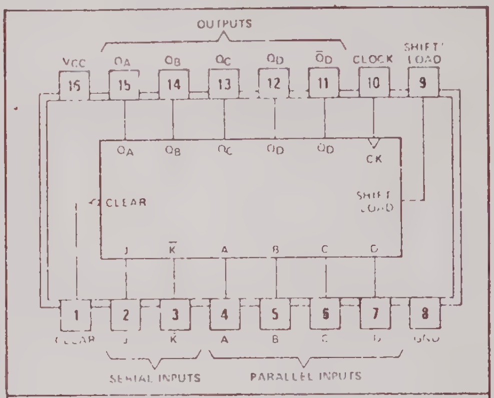
SN74LS195N

S-D P/N 103163

## TYPES SN54195, SN54LS195, SN54S195, SN74195, SN74LS195, SN74S195 4-BIT PARALLEL-ACCESS SHIFT REGISTERS

- Synchronous Parallel Load
- Positive-Edge-Triggered Clocking
- Parallel Inputs and Outputs from Each Flip-Flop
- Direct Overriding Clear
- J and $\overline{K}$ Inputs to First Stage
- Complementary Outputs from Last Stage
- For Use in High-Performance:
  - Accumulators/Processors
  - Serial-to-Parallel, Parallel-to-Serial Converters

**J OR N DUAL-IN-LINE OR W FLAT PACKAGE (TOP VIEW)**



positive logic: see function table

### description

These 4-bit registers feature parallel inputs, parallel outputs, J-$\overline{K}$ serial inputs, shift/load control input, and a direct overriding clear. All inputs are buffered to lower the input drive requirements. The registers have two modes of operation:

Parallel (Broadside) Load

Shift (In direction $Q_A$ toward $Q_D$)

| TYPE | TYPICAL MAXIMUM CLOCK FREQUENCY | TYPICAL POWER DISSIPATION |
|---|---|---|
| '195 | 39 MHz | 195 mW |
| 'LS195 | 28 MHz | 50 mW |
| 'S195 | 105 MHz | 375 mW |

Parallel loading is accomplished by applying the four bits of data and taking the shift/load control input low. The data is loaded into the associated flip-flop and appears at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

Shifting is accomplished synchronously when the shift/load control input is high. Serial data for this mode is entered at the J-$\overline{K}$ inputs. These inputs permit the first stage to perform as a J-$\overline{K}$, D-, or T-type flip-flop as shown in the function table.

The high performance 'S195, with a 105-megahertz typical maximum shift-frequency, is particularly attractive for very-high-speed data processing systems. In most cases existing systems can be upgraded merely by using this Schottky clamped shift register.

FUNCTION TABLE

| INPUTS | | | | | | | | | OUTPUTS | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CLEAR | SHIFT/ LOAD | CLOCK | SERIAL | | PARALLEL | | | | $Q_A$ | $Q_B$ | $Q_C$ | $Q_D$ | $\overline{Q}_D$ |
| | | | J | $\overline{K}$ | A | B | C | D | | | | | |
| L | X | X | X | X | X | X | X | X | L | L | L | L | H |
| H | L | ↑ | X | X | a | b | c | d | a | b | c | d | d |
| H | H | L | X | X | X | X | X | X | $Q_{A0}$ | $Q_{B0}$ | $Q_{C0}$ | $Q_{D0}$ | $\overline{Q}_{D0}$ |
| H | H | ↑ | L | H | X | X | X | X | $Q_{A0}$ | $Q_{A0}$ | $Q_{Bn}$ | $Q_{Cn}$ | $\overline{Q}_{Cn}$ |
| H | H | ↑ | L | L | X | X | X | X | L | $Q_{An}$ | $Q_{Bn}$ | $Q_{Cn}$ | $\overline{Q}_{Cn}$ |
| H | H | ↑ | H | H | X | X | X | X | H | $Q_{An}$ | $Q_{Bn}$ | $Q_{Cn}$ | $\overline{Q}_{Cn}$ |
| H | H | ↑ | H | L | X | X | X | X | $\overline{Q}_{An}$ | $Q_{An}$ | $Q_{Bn}$ | $Q_{Cn}$ | $\overline{Q}_{Cn}$ |

H = high level (steady state)

L = low level (steady state)

X = irrelevant (any input, including transitions)

↑ = transition from low to high level

a, b, c, d = the level of steady state input at A, B, C, or D, respectively

$Q_{A0}$, $Q_{B0}$, $Q_{C0}$, $Q_{D0}$ = the level of $Q_A$, $Q_B$, $Q_C$, or $Q_D$, respectively, before the indicated steady-state input conditions were established

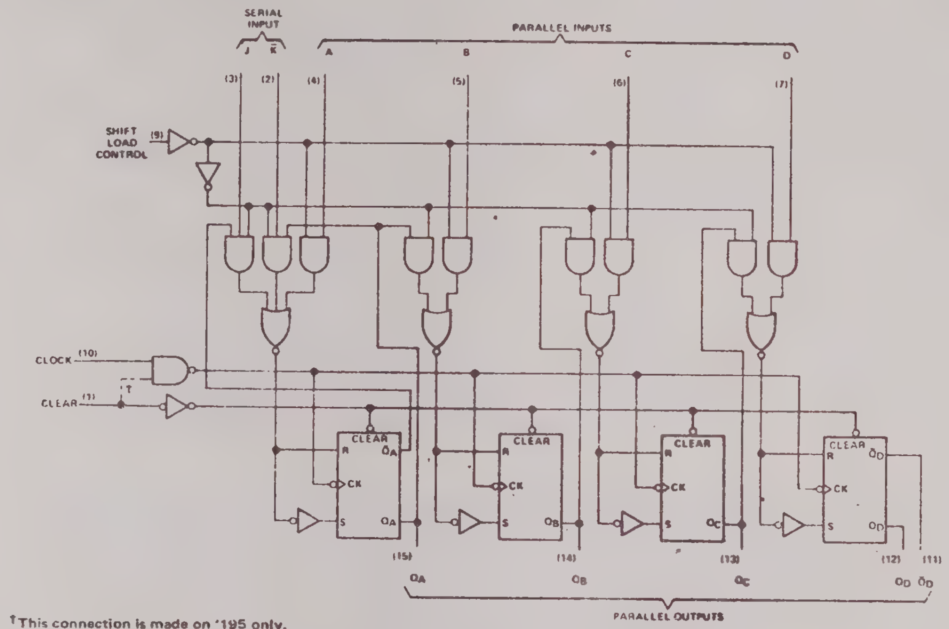
$Q_{An}$, $Q_{Bn}$, $Q_{Cn}$ = the level of $Q_A$, $Q_B$, or $Q_C$, respectively, before the most-recent transition of the clock

# TTL 4-BIT PARALLEL-ACCESS SHIFT REGISTERS (CONT)

SN74LS195N

S-D P/N 103163

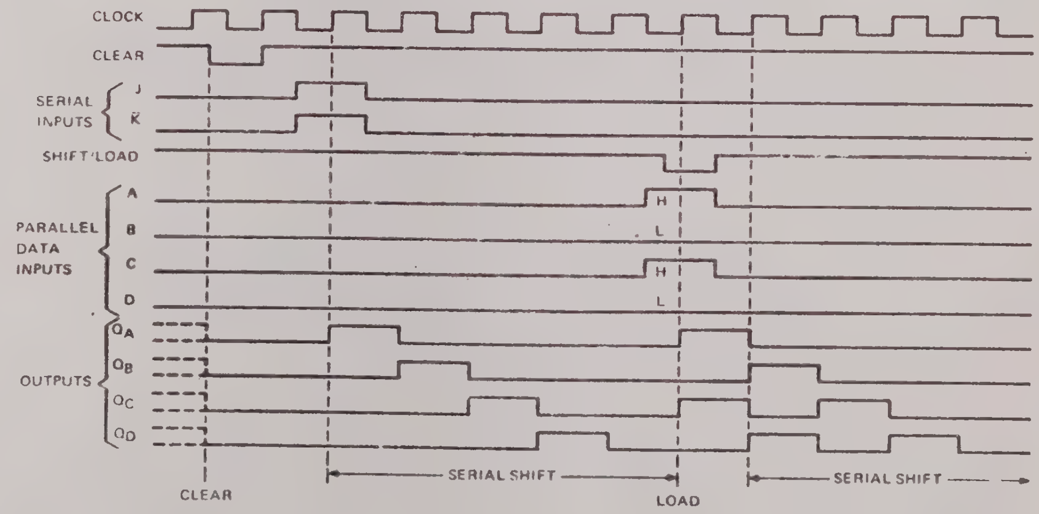
## functional block diagram


SERIAL INPUT
J
K̄
PARALLEL INPUTS
A
B
C
D
(3)
(2)
(4)
(5)
(6)
(7)
SHIFT LOAD CONTROL
(9)
CLOCK
(10)
CLEAR
(1)
†
CLEAR
R
Q̄A
CK
S
QA
QB
QC
QD
Q̄D
(15)
(14)
(13)
(12)
(11)
QA
QB
QC
QD Q̄D
PARALLEL OUTPUTS

† This connection is made on '195 only.

. . . dynamic input activated by a transition from a high level to a low level.

## typical clear, shift, and load sequences



SN74LS196N
SN74LS197N

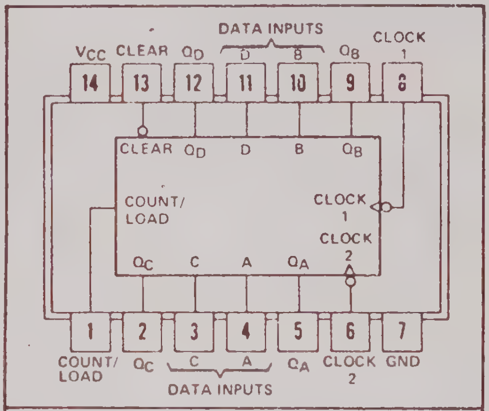
# TTL PRESETTABLE DECADE COUNTERS/LATCHES
# TTL PRESETTABLE BINARY COUNTERS/LATCHES

S-D P/N 103164
S-D P/N 103165

- Performs BCD, Bi-Quinary, or Binary Counting
- Fully Programmable
- Fully Independent Clear Input
- Input Clamping Diodes Simplify System Design
- Output $Q_A$ Maintains Full Fan-out Capability In Addition to Driving Clock-2 Input

| TYPES | GUARANTEED COUNT FREQUENCY CLOCK 1 | GUARANTEED COUNT FREQUENCY CLOCK 2 | TYPICAL POWER DISSIPATION |
|---|---|---|---|
| '196, '197 | 0-50 MHz | 0-25 MHz | 240 mW |
| 'LS196, 'LS197 | 0-30 MHz | 0-15 MHz | 60 mW |

J OR N DUAL-IN LINE OR
W FLAT PACKAGE (TOP VIEW)



asynchronous input: Low input to clear sets $Q_A$, $Q_B$, $Q_C$, and $Q_D$ low.

## description

These high-speed monolithic counters consist of four d-c coupled, master-slave flip-flops which are internally interconnected to provide either a divide-by-two and a divide-by-five counter ('196, 'LS196) or a divide-by-two and a divide-by-eight counter ('197, 'LS197). These four counters are fully programmable; that is, the outputs may be preset to any state by placing a low on the count/load input and entering the desired data at the data inputs. The outputs will change to agree with the data inputs independent of the state of the clocks.

During the count operation, transfer of information to the outputs occurs on the negative-going edge of the clock pulse. These counters feature a direct clear which when taken low sets all outputs low regardless of the states of the clocks.

These counters may also be used as 4-bit latches by using the count/load input as the strobe and entering data at the data inputs. The outputs will directly follow the data inputs when the count/load is low, but will remain unchanged when the count/load is high and the clock inputs are inactive.

All inputs are diode-clamped to minimize transmission-line effects and simplify system design. These circuits are compatible with most TTL and DTL logic families. Typical power dissipation is 60 milliwatts. Series 54 and 54LS circuits are characterized for operation over the full military temperature range of –55°C to 125°C; Series 74 and 74LS circuits are characterized for operation from 0°C to 70°C.

## typical count configurations

'196 and 'LS196 typical count configurations and function tables are the same as those for '176. See page 370.
'197 and 'LS197 typical count configurations and function tables are the same as those for '177. See page 370.

## functional block diagrams

'196 and 'LS196 functional block diagram is the same as that for '176. See page 371.
'197 and 'LS197 functional block diagram is the same as that for '177. See page 371.

## TTL 4-TO-7 LINE DECODER/DRIVER

SN74LS247N
SN74247N

S-D P/N 103166
S-D P/N 103314

**TTL**
**MSI**

# TYPES SN54246 THRU SN54249, SN54LS247 THRU SN54LS249, SN74246 THRU SN74249, SN74LS247 THRU SN74LS249 BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS

**'246, '247, 'LS247**
**feature**

- Open-Collector Outputs Drive Indicators Directly
- Lamp-Test Provision
- Leading/Trailing Zero Suppression

**'248, 'LS248**
**feature**

- Internal Pull-Ups Eliminate Need for External Resistors
- Lamp-Test Provision
- Leading/Trailing Zero Suppression

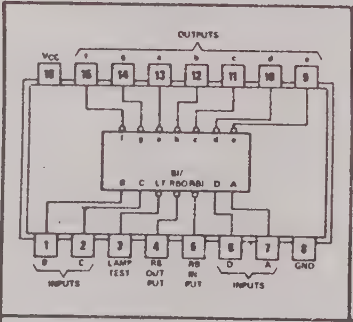
**'249, 'LS249**
**feature**

- Open-Collector Outputs
- Lamp-Test Provision
- Leading/Trailing Zero Suppression

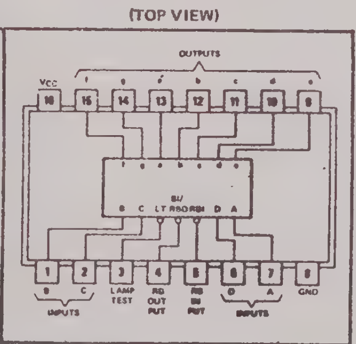
- All Circuit Types Feature Lamp Intensity Modulation Capability

| TYPE | DRIVER OUTPUTS | | | | TYPICAL POWER DISSIPATION | PACKAGES |
|---|---|---|---|---|---|---|
| | ACTIVE LEVEL | OUTPUT CONFIGURATION | SINK CURRENT | MAX VOLTAGE | | |
| SN54246 | low | open-collector | 40 mA | 30 V | 320 mW | J, W |
| SN54247 | low | open-collector | 40 mA | 15 V | 320 mW | J, W |
| SN54248 | high | 2-kΩ pull-up | 6.4 mA | 5.5 V | 265 mW | J, W |
| SN54249 | high | open-collector | 10 mA | 5.5 V | 265 mW | J, W |
| SN54LS247 | low | open-collector | 12 mA | 15 V | 35 mW | J, W |
| SN54LS248 | high | 2-kΩ pull-up | 2 mA | 5.5 V | 125 mW | J, W |
| SN54LS249 | high | open-collector | 4 mA | 5.5 V | 40 mW | J, W |
| SN74246 | low | open-collector | 40 mA | 30 V | 320 mW | J, N |
| SN74247 | low | open-collector | 40 mA | 15 V | 320 mW | J, N |
| SN74248 | high | 2-kΩ pull-up | 6.4 mA | 5.5 V | 265 mW | J, N |
| SN74249 | high | open-collector | 10 mA | 5.5 V | 265 mW | J, N |
| SN74LS247 | low | open-collector | 24 mA | 15 V | 35 mW | J, N |
| SN74LS248 | high | 2-kΩ pull-up | 6 mA | 5.5 V | 125 mW | J, N |
| SN74LS249 | high | open-collector | 8 mA | 5.5 V | 40 mW | J, N |

'246, '247, 'LS247
(TOP VIEW)



'248, '249, 'LS248, 'LS249
(TOP VIEW)



positive logic: see function tables

### description

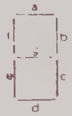
The '246 through '248 are electrically and functionally identical to the SN5446A/SN7446A, SN5447A/SN7447A, and SN5448/SN7448, respectively, and have the same pin assignments as their equivalents. Also the 'LS247 and 'LS248 are electrically and functionally identical to the SN54LS47/SN74LS47 and SN54LS48/SN74LS48, respectively, and have the same pin assignments as their equivalents. They can be used interchangeably in present or future designs to offer designers a choice between two indicator fonts. The '249 and 'LS249 are 16-pin versions of the 14-pin SN5449 and SN54LS49/SN74LS49, respectively. Included in the '249 and 'LS249 circuits is the full functional capability for lamp test and ripple blanking, which is not available in the '49 and 'LS49 circuits. The '46A, '47A, '48, '49, 'LS47, 'LS48, and 'LS49 compose the b and the q without tails and the '246 through '249 and 'LS247, 'LS248, and 'LS249

## description (continued)

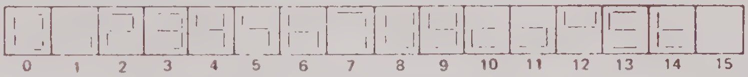
compose the 6 and the 9 with tails. Composition of all other characters, including display patterns for BCD inputs above nine, is identical. The '246, '247, and 'LS247 feature active-low outputs designed for driving indicators directly, and the '248, '249, 'LS248, and 'LS249 feature active-high outputs for driving lamp buffers. All of the circuits have full ripple-blanking input/output controls and a lamp test input. Segment identification and resultant displays are shown below. Display patterns for BCD input counts above 9 are unique symbols to authenticate input conditions.

All of these circuits incorporate automatic leading and/or trailing-edge zero-blanking control (RBI and RBO). Lamp test (LT) of these types may be performed at any time when the BI/RBO node is at a high level. All types contain an overriding blanking input (BI) which can be used to control the lamp intensity by pulsing or to inhibit the outputs. Inputs and outputs are entirely compatible for use with TTL or DTL logic outputs.

Series 54 and Series 54LS devices are characterized for operation over the full military temperature range of −55°C to 125°C; Series 74 and Series 74LS devices are characterized for operation from 0°C to 70°C.



SEGMENT IDENTIFICATION



NUMERICAL DESIGNATIONS AND RESULTANT DISPLAYS

'246, '247, 'LS247

FUNCTION TABLE

| DECIMAL OR FUNCTION | INPUTS | | | | | | BI/RBO† | OUTPUTS | | | | | | | NOTE |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | LT | RBI | D | C | B | A | | a | b | c | d | e | f | g | |
| 0 | H | H | L | L | L | L | H | ON | ON | ON | ON | ON | ON | OFF | 1 |
| 1 | H | X | L | L | L | H | H | OFF | ON | ON | OFF | OFF | OFF | OFF | |
| 2 | H | X | L | L | H | L | H | ON | ON | OFF | ON | ON | OFF | ON | |
| 3 | H | X | L | L | H | H | H | ON | ON | ON | ON | OFF | OFF | ON | |
| 4 | H | X | L | H | L | L | H | OFF | ON | ON | OFF | OFF | ON | ON | |
| 5 | H | X | L | H | L | H | H | ON | OFF | ON | ON | OFF | ON | ON | |
| 6 | H | X | L | H | H | L | H | ON | OFF | ON | ON | ON | ON | ON | |
| 7 | H | X | L | H | H | H | H | ON | ON | ON | OFF | OFF | OFF | OFF | |
| 8 | H | X | H | L | L | L | H | ON | ON | ON | ON | ON | ON | ON | |
| 9 | H | X | H | L | L | H | H | ON | ON | ON | ON | OFF | ON | ON | |
| 10 | H | X | H | L | H | L | H | OFF | OFF | OFF | ON | ON | OFF | ON | |
| 11 | H | X | H | L | H | H | H | OFF | OFF | ON | ON | OFF | OFF | ON | |
| 12 | H | X | H | H | L | L | H | OFF | ON | OFF | OFF | OFF | ON | ON | |
| 13 | H | X | H | H | L | H | H | ON | OFF | OFF | ON | OFF | ON | ON | |
| 14 | H | X | H | H | H | L | H | OFF | OFF | OFF | ON | ON | ON | ON | |
| 15 | H | X | H | H | H | H | H | OFF | OFF | OFF | OFF | OFF | OFF | OFF | |
| BI | X | X | X | X | X | X | L | OFF | OFF | OFF | OFF | OFF | OFF | OFF | 2 |
| RBI | H | L | L | L | L | L | L | OFF | OFF | OFF | OFF | OFF | OFF | OFF | 3 |
| LT | L | X | X | X | X | X | H | ON | ON | ON | ON | ON | ON | ON | 4 |

H = high level, L = low level, X = irrelevant

NOTES:
1. The blanking input (BI) must be open or held at a high logic level when output functions 0 through 15 are desired. The ripple-blanking input (RBI) must be open or high if blanking of a decimal zero is not desired.
2. When a low logic level is applied directly to the blanking input (BI), all segment outputs are off regardless of the level of any other input.
3. When ripple blanking input (RBI) and inputs A, B, C, and D are at a low level with the lamp test input high, all segment outputs go off and the ripple blanking output (RBO) goes to a low level (response condition).
4. When the blanking input/ripple blanking output (BI/RBO) is open or held high and a low is applied to the lamp test input, all segment outputs are on.

†BI/RBO is wire AND logic serving as blanking input (BI) and/or ripple blanking output (RBO).

# TTL 4-TO-7 LINE DECODER/DRIVER (CONT)

SN74LS247N

S-D P/N 103166

'248, '249, 'LS248, 'LS249

FUNCTION TABLE

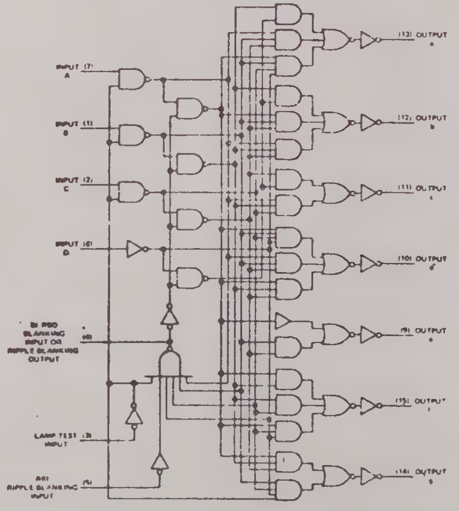
| DECIMAL OR FUNCTION | INPUTS | | | | | | BI/RBO† | OUTPUTS | | | | | | | NOTE |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | LT | RBI | D | C | B | A | | a | b | c | d | e | f | g | |
| 0 | H | H | L | L | L | L | H | H | H | H | H | H | H | L | 1 |
| 1 | H | X | L | L | L | H | H | L | H | H | L | L | L | L | 1 |
| 2 | H | X | L | L | H | L | H | H | H | L | H | H | L | H | 1 |
| 3 | H | X | L | L | H | H | H | H | H | H | H | L | L | H | |
| 4 | H | X | L | H | L | L | H | L | H | H | L | L | H | H | |
| 5 | H | X | L | H | L | H | H | H | L | H | H | L | H | H | |
| 6 | H | X | L | H | H | L | H | H | L | H | H | H | H | H | |
| 7 | H | X | L | H | H | H | H | H | H | H | L | L | L | L | |
| 8 | H | X | H | L | L | L | H | H | H | H | H | H | H | H | |
| 9 | H | X | H | L | L | H | H | H | H | H | H | L | H | H | |
| 10 | H | X | H | L | H | L | H | L | L | L | H | H | L | H | |
| 11 | H | X | H | L | H | H | H | L | L | H | H | L | L | H | |
| 12 | H | X | H | H | L | L | H | L | H | L | L | L | H | H | |
| 13 | H | X | H | H | L | H | H | H | L | L | H | L | H | H | |
| 14 | H | X | H | H | H | L | H | L | L | L | H | H | H | H | |
| 15 | H | X | H | H | H | H | H | L | L | L | L | L | L | L | |
| BI | X | X | X | X | X | X | L | L | L | L | L | L | L | L | 2 |
| RBI | H | L | L | L | L | L | L | L | L | L | L | L | L | L | 3 |
| LT | L | X | X | X | X | X | H | H | H | H | H | H | H | H | 4 |

H = high level, L = low level, X = irrelevant

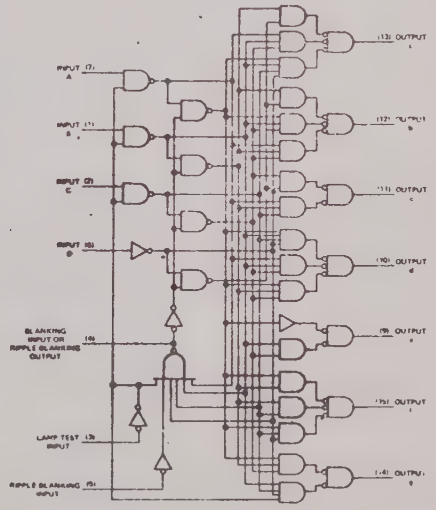
NOTES:
1. The blanking input (BI) must be open or held at a high logic level when output functions 0 through 15 are desired. The ripple-blanking input (RBI) must be open or high if blanking of a decimal zero is not desired.
2. When a low logic level is applied directly to the blanking input (BI), all segment outputs are low regardless of the level of any other input.
3. When ripple-blanking input (RBI) and inputs A, B, C, and D are at a low level with the lamp test input high, all segment outputs go low and the ripple-blanking output (RBO) goes to a low level (response condition).
4. When the blanking input/ripple-blanking output (BI/RBO) is open or held high and a low is applied to the lamp-test input, all segment outputs are high.

†BI/RBO is wire-AND logic serving as blanking input (BI) and/or ripple-blanking output (RBO).

'246, '247, 'LS247


INPUT (7) A
INPUT (1) B
INPUT (2) C
INPUT (6) D
BI/RBO BLANKING INPUT OR RIPPLE BLANKING OUTPUT (4)
LAMP TEST (3) INPUT
RBI RIPPLE BLANKING (5) INPUT
(13) OUTPUT a
(12) OUTPUT b
(11) OUTPUT c
(10) OUTPUT d
(9) OUTPUT e
(15) OUTPUT f
(14) OUTPUT g

'248, '249, 'LS248, 'LS249


INPUT (7) A
INPUT (1) B
INPUT (2) C
INPUT (6) D
BLANKING INPUT OR RIPPLE BLANKING OUTPUT (4)
LAMP TEST (3) INPUT
RIPPLE BLANKING (5) INPUT
(13) OUTPUT a
(12) OUTPUT b
(11) OUTPUT c
(10) OUTPUT d
(9) OUTPUT e
(15) OUTPUT f
(14) OUTPUT g

# DIFFERENTIAL COMPARATORS WITH STROBE

**SN72311P** **S-D P/N 103943**

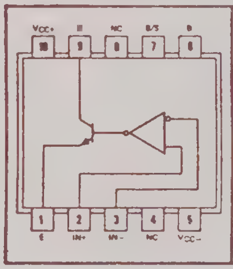
## description

The SN52111 and SN72311 are single high-speed voltage comparators. These devices are designed to operate from a wide range of power supply voltage, including ±15-volt supplies for operational amplifiers and 5-volt supplies for logic systems. The output levels are compatible with most DTL, TTL, and MOS circuits. These comparators are capable of driving lamps or relays and switching voltages up to 50 volts at 50 milliamperes. All inputs and outputs can be isolated from system ground. The outputs can drive loads referenced to ground, $V_{CC+}$, or $V_{CC-}$. Offset balancing and strobe capability are available and the outputs can be wire-OR connected. If the strobe input is low, the output will be in the off state regardless of the differential input. Although slower than the SN52506 and SN52514, these devices are not as sensitive to spurious oscillations.

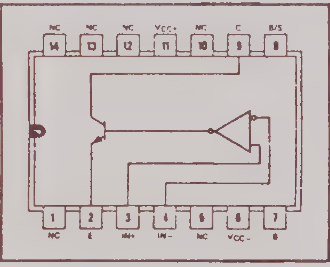
The SN52111 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN72311 is characterized for operation from 0°C to 70°C.

## terminal assignments

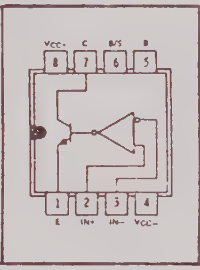
FA FLAT PACKAGE
(TOP VIEW)


VCC+
B
NC
B/S
B
10
9
8
7
6
1
2
3
4
5
E
IN+
IN−
NC
VCC−

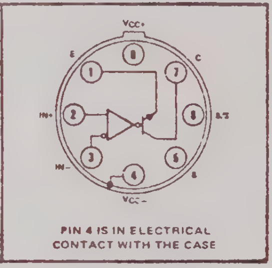
J OR N DUAL-IN-LINE
PACKAGE (TOP VIEW)


NC
NC
NC
VCC+
NC
C
B/S
14
13
12
11
10
9
8
1
2
3
4
5
6
7
NC
E
IN+
IN−
NC
VCC−
B

JP OR P DUAL-IN-LINE
PACKAGE (TOP VIEW)

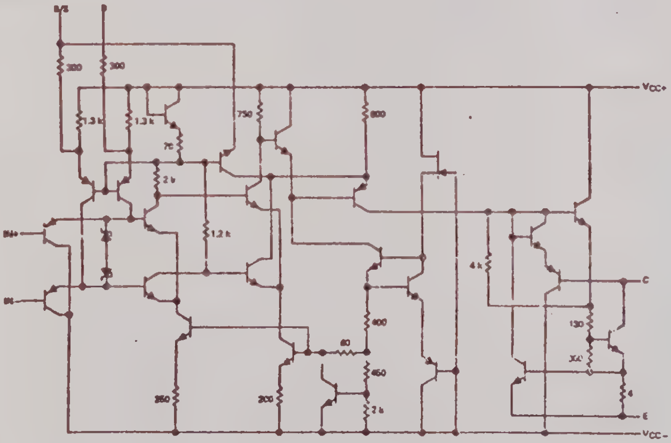

VCC+
C
B/S
B
8
7
6
5
1
2
3
4
E
IN+
IN−
VCC−

L PLUG-IN PACKAGE
(TOP VIEW)


VCC+
E
C
IN+
B/S
IN−
B
VCC−
1
2
3
4
5
6
7
8

PIN 4 IS IN ELECTRICAL CONTACT WITH THE CASE

## schematic


B/S
B
300
300
VCC+
1.3 k
1.3 k
750
800
70
2 k
1.2 k
IN+
IN−
4 k
C
130
300
4
E
400
60
450
2 k
250
200
VCC−

| | |
|---|---|
| B | Balance |
| B/S | Balance/Strobe |
| C | Collector Output |
| E | Emitter Output |
| IN+ | Noninverting Input |
| IN− | Inverting Input |
| NC | No Internal Connection |
| $V_{CC+}$ | Positive Supply Voltage |
| $V_{CC-}$ | Negative Supply Voltage |

Resistor values shown are nominal and in ohms.

# SP8634B ÷ 10 700 MHz SP8635B ÷ 10 600 MHz
# SP8636B ÷ 10 500 MHz SP8637B ÷ 10 400 MHz

The SP8634B, SP8635B, SP8636B and SP8637B are divide-by-ten circuits with binary coded decimal outputs for operation from DC up to specified input frequencies of 700, 600, 500 and 400 MHz, respectively, over a guaranteed temperature range of 0°C to +70°C.

These devices, optimised for counter applications in systems using both ECL and TTL, are intended to be operated between 0V and −5.2V power rails and to interface with TTL operating between 0V and +5V. The BCD outputs and one of two carry outputs are TTL-compatible, while the second carry output is ECL-compatible. The clock input, which is normally capacitively coupled to the signal source, is gated by an ECL III/ECL 10k-compatible input. The TTL-compatible reset forces the 0000 state regardless of the state of the other inputs.

## FEATURES

- Direct gating capability at up to 700 MHz
- TTL- compatible BCD outputs
- TTL- and ECL-compatible carry outputs
- Power consumption less than 500 mW
- Wide dynamic input range

## APPLICATIONS

- Counters
- Timers
- Synthesisers

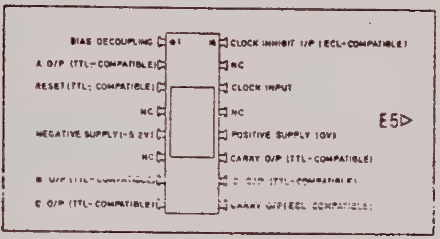

BIAS DECOUPLING
A O/P (TTL-COMPATIBLE)
RESET (TTL-COMPATIBLE)
NC
NEGATIVE SUPPLY (-5.2V)
NC
B O/P (TTL-COMPATIBLE)
C O/P (TTL-COMPATIBLE)
1
16
CLOCK INHIBIT I/P (ECL-COMPATIBLE)
NC
CLOCK INPUT
NC
POSITIVE SUPPLY (0V)
CARRY O/P (TTL-COMPATIBLE)
D O/P (TTL-COMPATIBLE)
CARRY O/P (ECL COMPATIBLE)
E5

*Fig. 1 Pin connections (top)*

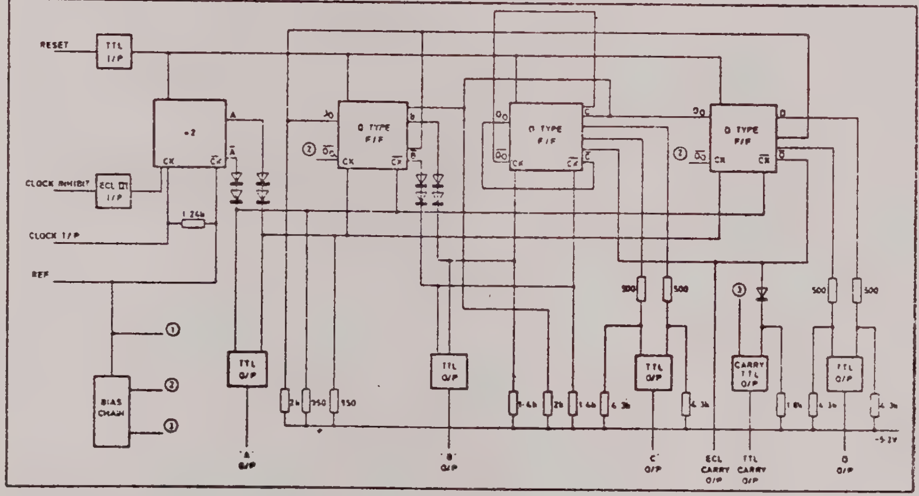

RESET
TTL I/P
÷2
CLOCK INHIBIT
ECL I/P
CLOCK I/P
REF
1.2k
BIAS CHAIN
①
②
③
D TYPE F/F
TTL O/P
CARRY TTL O/P
500
2k
250
150
1.6k
4.3k
-5.2V
'A' O/P
'B' O/P
'C' O/P
ECL CARRY O/P
TTL CARRY O/P
D O/P

*Fig. 2 Logic diagram*

## QUICK REFERENCE DATA

| | | |
|---|---|---|
| Power Supplies | $V_{CC}$ | 0V |
| | $V_{EE}$ | −5.2V ± 0.25V |
| Range of clock input amplitude | | 400-800mV p-p |
| Operational temperature range | | 0°C to +70°C |
| Frequency range with sinusoidal I/P | | 40-700 MHz (SP8634B) |
| Frequency range with square wave I/P | | DC to 700 MHz (SP8634B) |

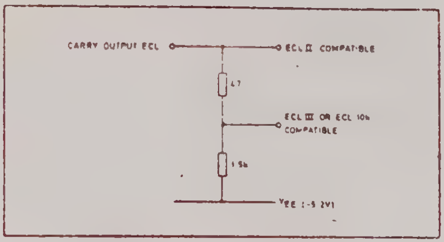

CARRY OUTPUT ECL
ECL II COMPATIBLE
47
ECL III OR ECL 10k COMPATIBLE
1.5k
VEE (-5.2V)

*Fig. 3 ECL III/ECL 10000 interfacing*

## OPERATING NOTES

The devices are intended to be used with TTL and ECL in a counting system — the ECL and the decade counter being connected between voltage rails of 0V and −5.2V and the TTL between voltage rails of 0V and +5.2V. Provided that this is done ECL and TTL compatibility is achieved (see Fig. 4).

The clock is normally capacitively coupled to the signal source: a 1000pF UHF capacitor is normally adequate. If low frequency operation is required the 1000pF capacitor should be connected in parallel with a higher value capacitor. The bias decoupling (pin 1) should be connected to earth via a capacitor — preferably a chip type – but in any case a low inductance type suitable for UHF applications. The devices normally have an input amplitude operating range far greater than the specified 400 to 800 mV pk/pk. However, if the decoupling capacitor is not of a UHF type, or it is connected to an earth point that has a significant impedance between the capacitor and the $V_{CC}$ connection, then the input dynamic range will suffer and the maximum signal for correct operation will be reduced.

Under certain conditions, the absence of an input signal may cause the device to self-oscillate. This can be prevented (while still maintaining the specified input sensitivity) by connecting a 68kΩ resistor between the clock input and the negative supply. If the transition of either the clock input or the clock inhibit input is slow the device may start to self-oscillate during the transition. For this reason, the input slew rates should be greater than 100 V/µs. It should also be noted that a positive-going transition on either the clock input or the clock inhibit input will clock the device, provided that the other input is in the low state.

The BCD outputs give TTL-compatible outputs (fanout = 1) when a 10kΩ resistor is connected from the output to the +5V rail. In this configuration the outputs will be very slow compared with the clocking rate of the decade and so the state on the BCD outputs can only be determined when the clock has stopped or is inhibited.

The fan out capability of the TTL carry output can be increased by buffering it with a PNP emitter follower. The interface is shown in Fig. 4.

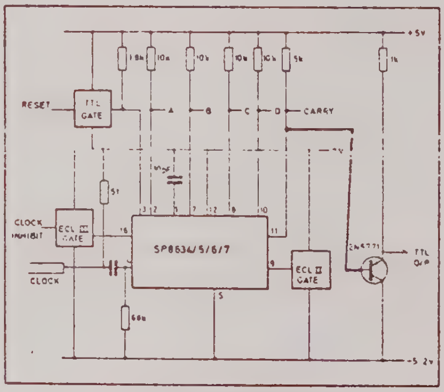
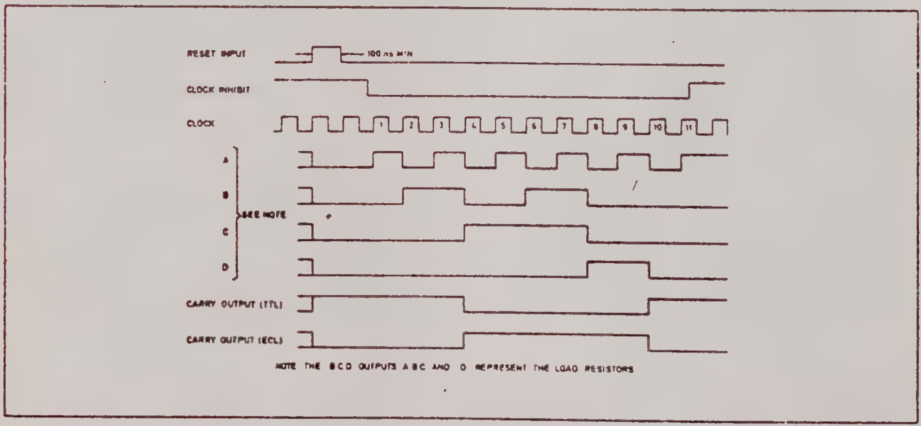

+5V
1.8k
10k
10k
10k
10k
5k
1k
RESET
TTL GATE
A
B
C
D
CARRY
-5V
10nF
51
3
2
5
7
12
8
10
CLOCK INHIBIT
ECL II GATE
16
11
SP8634/5/6/7
2N5771
TTL O/P
CLOCK
9
ECL II GATE
5
68k
-5.2V

*Fig. 4 Typical application configuration*


RESET INPUT
100 ns MIN
CLOCK INHIBIT
CLOCK
1
2
3
4
5
6
7
8
9
10
11
A
B
C
D
SEE NOTE
CARRY OUTPUT (TTL)
CARRY OUTPUT (ECL)

NOTE THE BCD OUTPUTS A B C AND D REPRESENT THE LOAD RESISTORS

*Fig. 5 Decade counter timing diagram*

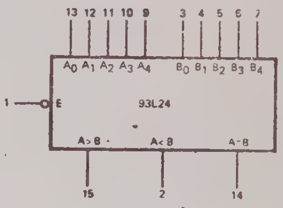
# TTL 5-BIT COMPARATOR

93L24 S-D P/N 117020

**DESCRIPTION** — The LPTTL/MSI 93L24 is a Medium Speed Expandable Comparator which provides comparison between two 5-bit words and gives three outputs, "less than", "greater than", and "equal to". A HIGH level on the active LOW enable input forces all three outputs LOW.

- THREE SEPARATE OUTPUTS . . . A < B, A > B, A = B
- EASILY EXPANDABLE
- ACTIVE LOW-LEVEL ENABLE INPUT
- HIGH DRIVE OUTPUT CIRCUITRY
- TYPICAL PROPAGATION DELAY OF 55 ns (A > B)
- TYPICAL POWER DISSIPATION OF 52 mW
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- ALL CERAMIC "HERMETIC" 16-LEAD DUAL IN LINE AND FLAT PACKAGES
- TTL COMPATIBLE

## LOGIC SYMBOL



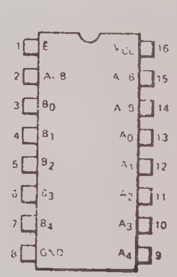
13 12 11 10 9
3 4 5 6 7
$A_0$ $A_1$ $A_2$ $A_3$ $A_4$
$B_0$ $B_1$ $B_2$ $B_3$ $B_4$
1
E
93L24
A>B
A<B
A=B
15
2
14

$V_{CC}$ = Pin 16
GND = Pin 8

| PIN NAMES | | LOADING HIGH | LOADING LOW |
|---|---|---|---|
| $\bar{E}$ | Enable (Active LOW) Input | 1.0 U.L. | 0.5 U.L. |
| $A_0, A_1, A_2, A_3, A_4$ | Word A Parallel Inputs | 1.0 U.L. | 0.5 U.L. |
| $B_0, B_1, B_2, B_3, B_4$ | Word B Parallel Inputs | 1.0 U.L. | 0.5 U.L. |
| A < B | A Less than B Output | 9 U.L. | 2.25 U.L. |
| A > B | A Greater than B Output | 9 U.L. | 2.25 U.L. |
| A = B | A Equal to B Output | 10 U.L. | 2.5 U.L. |

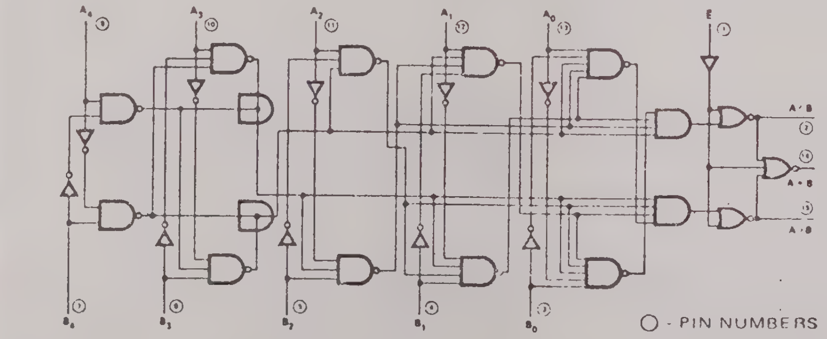
1 Unit Load (U.L.) = 40μA HIGH/1.6mA LOW.

## CONNECTION DIAGRAMS
## DIP (TOP VIEW)



1 E
2 A<B
3 $B_0$
4 $B_1$
5 $B_2$
6 $B_3$
7 $B_4$
8 GND
16 $V_{CC}$
15 A>B
14 A=B
13 $A_0$
12 $A_1$
11 $A_2$
10 $A_3$
9 $A_4$

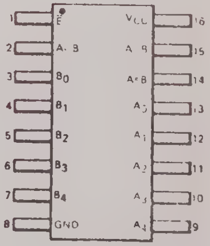
## LOGIC DIAGRAM



$A_4$ 9
$A_3$ 10
$A_2$ 11
$A_1$ 12
$A_0$ 13
E 1
A<B 2
14
A=B
15
A>B
7
$B_4$
6
$B_3$
5
$B_2$
4
$B_1$
3
$B_0$

○ - PIN NUMBERS

## FLATPAK (TOP VIEW)



1 E
2 A<B
3 $B_0$
4 $B_1$
5 $B_2$
6 $B_3$
7 $B_4$
8 GND
16 $V_{CC}$
15 A>B
14 A=B
13 $A_0$
12 $A_1$
11 $A_2$
10 $A_3$
9 $A_4$

**FUNCTIONAL DESCRIPTION** – The 93L24 5-bit comparator uses combinational circuitry to directly generate "A greater than B" and "A less than B" outputs. As evident from the logic diagram, these outputs are generated in only three gate delays. The "A equals B" output is generated in one additional gate delay by decoding the "A neither less than nor greater than B" condition with a NOR gate. All three outputs are activated by the active LOW enable input ($\bar{E}$).

Tying the A > B output from one device into an A input on another device and the A < B output into the corresponding B input permits easy expansion as shown in Figure 1.

The $A_4$ and $B_4$ inputs are the most significant inputs and $A_0$, $B_0$ the least significant. Thus if $A_4$ is HIGH and $B_4$ is LOW, the A > B output will be HIGH regardless of all other inputs except $\bar{E}$.

## TRUTH TABLE

| $\bar{E}$ | A | B | A < B | A > B | A = B |
|---|---|---|---|---|---|
| H | X | X | L | L | L |
| L | Word A = Word B | | L | L | H |
| L | Word A > Word B | | L | H | L |
| L | Word A < Word B | | H | L | L |

**L** = LOW Voltage Level
**H** = HIGH Voltage Level
**X** = Either HIGH or LOW Voltage Level

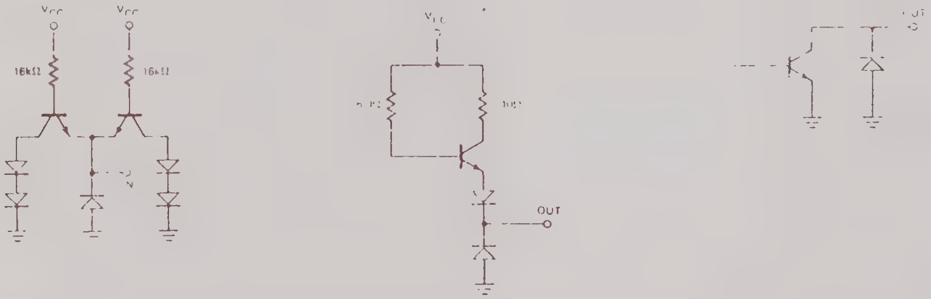
## TYPICAL INPUT AND OUTPUT CIRCUITS

INPUTS EQUIVALENT CIRCUIT

OUTPUTS EQUIVALENT CIRCUITS

OUTPUT HIGH

OUTPUT LOW



**ABSOLUTE MAXIMUM RATINGS** (above which the useful life may be impaired)

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Temperature (Ambient) Under Bias | −55°C to +125°C |
| $V_{CC}$ Pin Potential to Ground Pin | −0.5 V to +7.0 V |
| *Input Voltage (dc) | −0.5 V to +5.5 V |
| *Input Current (dc) | −30 mA to +5.0 mA |
| Voltage Applied to Outputs (Output HIGH) | −0.5 V to $+V_{CC}$ value |
| Output Current (dc) (Output LOW) | +30 mA |

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

**GUARANTEED OPERATING RANGES**

| PART NUMBER | SUPPLY VOLTAGE ($V_{CC}$) | | | TEMPERATURE |
|---|---|---|---|---|
| | MIN. | TYP. | MAX. | |
| 93L24XM | 4.5 V | 5.0 V | 5.5 V | −55°C to 125°C |
| 93L24XC | 4.75 V | 5.0 V | 5.25 V | 0°C to 75°C |

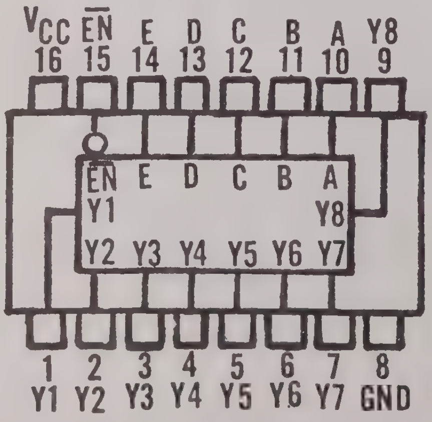
X = package type, F for Flatpak, D for Ceramic Dip, P for Plastic Dip.

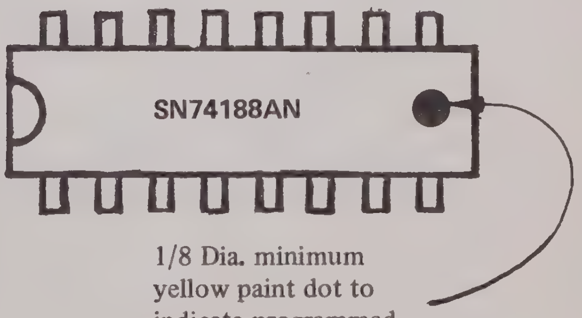
## PROGRAMMED READ ONLY MEMORY (A12U4)

SD055123

S-D P/N 055123

| PROGRAMMED INPUTS | | | | | PROGRAMMED OUTPUTS | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| E | D | C | B | A | Y8 | Y7 | Y6 | Y5 | Y4 | Y3 | Y2 | Y1 |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 |
| 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 |
| 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 |
| 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 |
| 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 |
| 0 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 |
| 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 |
| 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |


$V_{CC}$ 16
$\overline{EN}$ 15
E 14
D 13
C 12
B 11
A 10
Y8 9
$\overline{EN}$
E
D
C
B
A
Y1
Y8
Y2
Y3
Y4
Y5
Y6
Y7
1 Y1
2 Y2
3 Y3
4 Y4
5 Y5
6 Y6
7 Y7
8 GND



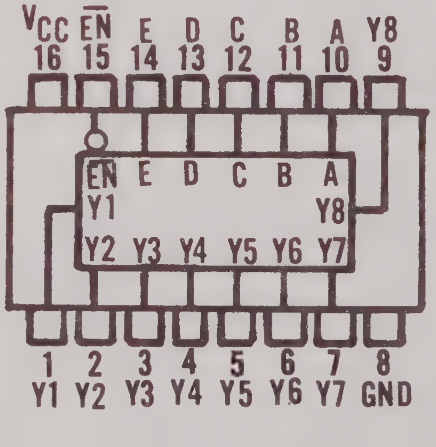
1/8 Dia. minimum
yellow paint dot to
indicate programmed
IC to this specification.

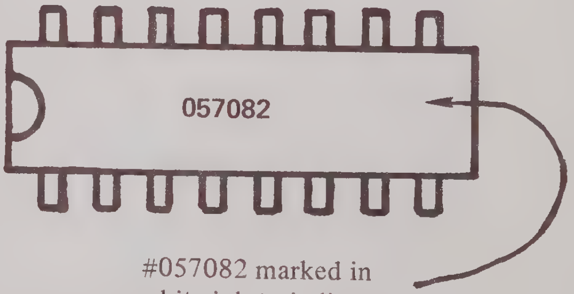
## PROGRAMMED READ ONLY MEMORY (A2U2)

SD057082

S-D P/N 057082

| PROGRAMMED INPUTS | | | | | PROGRAMMED OUTPUTS | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| E | D | C | B | A | Y8 | Y7 | Y6 | Y5 | Y4 | Y3 | Y2 | Y1 |
| 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |


$V_{CC}$ 16
$\overline{EN}$ 15
E 14
D 13
C 12
B 11
A 10
Y8 9
$\overline{EN}$ E D C B A
Y1
Y8
Y2 Y3 Y4 Y5 Y6 Y7
1 Y1
2 Y2
3 Y3
4 Y4
5 Y5
6 Y6
7 Y7
8 GND



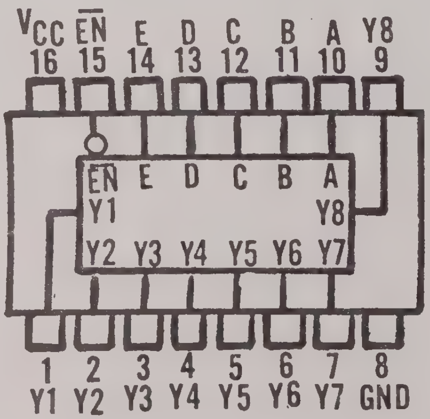
#057082 marked in
white ink to indicate
programmed IC to
this specification.

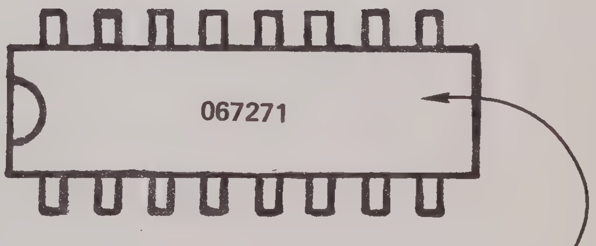
## PROGRAMMED READ ONLY MEMORY (A12U7)

SD067271

S-D P/N 067271

| PROGRAMMED INPUTS | | | | | PROGRAMMED OUTPUTS | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| E | D | C | B | A | Y8 | Y7 | Y6 | Y5 | Y4 | Y3 | Y2 | Y1 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 |


VCC 16
$\overline{EN}$ 15
E 14
D 13
C 12
B 11
A 10
Y8 9
$\overline{EN}$ E D C B A
Y1
Y8
Y2 Y3 Y4 Y5 Y6 Y7
1 Y1
2 Y2
3 Y3
4 Y4
5 Y5
6 Y6
7 Y7
8 GND



#067271 marked in white
ink to indicate programmed
IC to this specification.

# CHAPTER 6

# REPLACEABLE PARTS

## 6-1 INTRODUCTION

This chapter contains the parts list for each assembly in the Model 6054B Frequency Counter. Chapter 7 shows the assemblies where the listed parts are installed. Ordering information is included and should be used when purchasing parts from the factory. Explanation of the column listings and Table 6-1 Manufacturer's Code-To-Name Index are also included.

## 6-2. PART ORDERING INFORMATION

To order a part from the Replaceable Parts List, state the Systron-Donner part number, and indicate the quantity required and address the order to the nearest Systron Donner Sales or Service Center.

To order a part not listed in the Replaceable Parts List, state the instrument model number, instrument serial number, the description and function of the part and the number of parts required. Address the order to the nearest Systron Donner Sales or Service Center.

## 6-3 PARTS LIST

The replaceable parts lists are placed in "A" board reference numbered sequence.

Each column in the parts lists provide specific information relating to the listed parts as follows:

(1) DESIGNATOR: Reference numbers applicable to assemblies are listed in alpha-numeric order.

(2) COMPONENT NOMENCLATURE AND DESCRIPTION: Component names and specifications are provided in these columns and include value, tolerance, wattage rating, working voltages, construction, etc.

(3) MANUFACTURER'S CODE: H4-2 Federal Supply Code numbers are listed to identify component manufacturers. A Manufacturer's Index is provided in this chapter for cross-reference.

(4) MANUFACTURER'S PART NUMBER: True manufacturer part numbers are listed in this column.

(5) SD STOCK NUMBER: The Systron Donner stock number is listed in this column.

(6) T/Q (Total Quantity): This quantity, appearing after an item entry, indicates the number of times the component is used in that assembly. The total quantity for each part is given only once – at the first appearance of the part number in the list.

### TABLE 6-1 MANUFACTURER'S CODE-TO-NAME INDEX

| Code | Name & Address |
|---|---|
| 00779 | AMP Inc.<br>P.O. Box 3608<br>Harrisburg, PA 17105 |
| 01121 | Allen-Bradley Co.<br>1201 So. 2nd Street<br>Milwaukee, WI 53204 |
| 01295 | Texas Instrument Inc.<br>13500 No. Central Expressway<br>Dallas, TX 75231 |
| 02114 | Ferroxcube Corp.<br>P.O. Box 359 - Mt. Marion Road<br>Saugerties, NY 12477 |
| 02660 | Bunker Ramo Corp.<br>Amphenol Connector Division<br>2801 So. 25th Avenue<br>Broadview, IL 60153 |
| 02735 | RCA Corp. - Solid State Division<br>Route 202<br>Somerville, NJ 08876 |
| 02777 | Hopkins Eng. Co.<br>12900 Foothill Blvd.<br>San Fernando, CA 91342 |
| 03296 | Nylon Molding Corp.<br>40 Brown Street<br>Springfield, NJ 07081 |
| 03508 | General Electric Co.<br>Semiconductor Products Dept.<br>Electronics Park<br>Syracuse, NY 13201 |
| 03877 | Transitron Electronic Corp.<br>168 - 186 Albion Street<br>Wakefield, MA 01880 |
| 04222 | AVX Ceramic Corp.<br>P.O. Box 867<br>Myrtle Beach, SC 29577 |
| 04713 | Motorola Semiconductor Prod. Inc.<br>5005 E. McDowell Road<br>Phoenix, AZ 85008 |
| 05574 | Viking Industries Inc.<br>21001 Nordhoff<br>Chatsworth, CA 91311 |
| 06383 | Panduit Corp.<br>17301 Ridgeland<br>Tinley Park, IL 60477 |
| 06540 | Amatom Electronic Hardware<br>Division of Mite Corp.<br>81 Rockdale Avenue<br>New Rochelle, NY 10806 |
| 06560 | Airco Speer Electronics<br>Div. of Air Reduction Co. Inc.<br>P.O. Box 1692 Grand Plaza<br>Nogales, AZ 85621 |
| 07263 | Fairchild Camera & Instrument Corp.<br>Semiconductor Division<br>313 Frontage Road<br>Mountain View, CA 94040 |
| 07700 | Technical Wire Products Inc.<br>129 Dermody Street<br>Cranford, NJ 07016 |
| 07933 | Raytheon Co.<br>Semiconductor Div. Hq.<br>350 Ellis Street<br>Mountain View, CA 94040 |
| 08289 | Delbert Blinn Co. Inc.<br>P.O. Box 2007<br>1678 Mission Blvd.<br>Pomona, CA 91766 |
| 08547 | R. G. Wallace Co. Inc.<br>2301 E. Del Amo Blvd.<br>Compton, CA 90220 |
| 09353 | C and K Components Inc.<br>103 Morse<br>Newton, MA 02158 |
| 11236 | CTS of Berne Inc.<br>406 Parr Road<br>Berne, IN 46711 |
| 12014 | Chicago Rivet & Machine Co.<br>950 So. 25th Avenue<br>Bellwood, IL 60104 |
| 12517 | Component Research Co. Inc.<br>1717 - 19th Street<br>Santa Monica, CA 90404 |

## TABLE 6-1 MANUFACTURER'S CODE-TO-NAME INDEX (Cont'd)

| Code | Name & Address |
|---|---|
| 13103 | Thermalloy Co.<br>2021 W. Valley View Lane<br>Dallas, TX 75234 |
| 14655 | Cornell - Dubilier Electronics<br>Govt. contracts Dept.<br>150 Avenue L<br>Newark, NJ 07101 |
| 16179 | Omni Spectra Inc.<br>24600 Hallwood Ct.<br>Farmington, MI 48024 |
| 16733 | Phelps Dodge Communications Co.<br>North Haven, CT 06473 |
| 18324 | Signetics Corp.<br>811 E. Arques<br>Sunnyvale, CA 94086 |
| 19701 | Mepco/Electra Inc.<br>Electra Division<br>P.O. Box 760<br>Mineral Wells, TX 76067 |
| 23936 | Pamotor<br>Division of William J. Purdy Co.<br>770 Airport Blvd.<br>Burlingame, CA 94010 |
| 27014 | National Semiconductor Corp.<br>2950 San Ysidro Way<br>Santa Clara, CA 95051 |
| 27264 | Molex Products Co.<br>5224 Katrine Ave.<br>Downers Grove, IL 60515 |
| 28480 | Hewlett - Packard Co.<br>1501 Page Mill Rd.<br>Palo Alto, CA 94304 |
| 28520 | Heyman Mfg. Co.<br>147 N. Michigan Avenue<br>Kenilworth, NJ 07033 |
| 29990 | American Technical Ceramics<br>Division of Phase Industries<br>1 Nordon Lane<br>Huntington Station, NY 11746 |
| 31433 | Union Carbide Corp.<br>Materials Systems Div. Components Div.<br>Highway 276 S.E.<br>Greenville, SC 29606 |
| 32159 | West - Cap Arizona<br>2201 E. Elvira Rd.<br>Tucson, AZ 85706 |
| 50346 | Monolithic Memories Inc.<br>1165 E. Arques Ave.<br>Sunnyvale, CA 94086 |
| 50522 | Monsanto Co.<br>Electronic Special Products<br>10131 Bubb Rd.<br>Cupertino, CA 95014 |
| 51495 | R & D Plastics<br>780 - 32nd Street<br>Richmond, CA 94804 |
| 52542 | Systron Donner Corp.<br>Instrument Division<br>2727 Systron Drive<br>Concord, CA 94518 |
| 52648 | Plessey Semiconductor<br>1641 Kaiser Avenue<br>Irvine, CA 92714 |
| 55210 | Gettig Engineering & Mfg.<br>P.O. Box 85 Off Route 45<br>Spring Mill, PA 16875 |
| 56289 | Sprague Electronic Co.<br>North Adams, MA 01247 |
| 70903 | Belden Corp.<br>415 So. Kilpatrick<br>Chicago, IL 60644 |
| 71279 | Cambridge Thermonic Corp.<br>445 Concord Ave.<br>Cambridge, MA 01238 |
| 71286 | Rexnard Inc.<br>Specialty Fastener Division<br>22 Spring Valley Road<br>Paramus, NJ 07652 |
| 71400 | Bussmann Mfg.<br>Division of McGraw-Edison Co.<br>2536 W. University Street<br>St. Louis, MO 63017 |
| 71590 | Globe-Union Inc.<br>Centralab Electronics Division<br>5757 No. Green Bay Avenue<br>Milwaukee, WI 53201 |

## TABLE 6-1 MANUFACTURER'S CODE-TO-NAME INDEX (Cont'd)

| Code | Name & Address |
|---|---|
| 71744 | Chicago Miniature Lamp Works<br>4433 Ravenswood Avenue<br>Chicago, IL 60640 |
| 72136 | Electro Motive Mfg. Co. Inc.<br>South Park & John Sts.<br>Willimantic, CT 06226 |
| 72259 | Nytronics Inc.<br>10 Pelham Pky.<br>Pelham Mannor, NY 10803 |
| 72982 | Erie Technological Products Inc.<br>644 W. 12th Street<br>Erie, PA 16512 |
| 73734 | Federal Screw Products Inc.<br>3917 N. Kenzie Avenue<br>Chicago, IL 60618 |
| 73803 | Texas Instruments Inc.<br>Metallurigical Materials Division<br>Attleboro, MA 02703 |
| 73957 | Groov-Pin Corp.<br>1125 Hendricks Causeway<br>Ridgefield, NJ 07657 |
| 75915 | LIttlefuse Inc.<br>800 E. Northwest Hwy.<br>Des Plaines, IL 60016 |
| 78189 | Illinois Tool Works Inc.<br>Shakeproof Division<br>St. Charles Road<br>Elgin, IL 60120 |
| 78526 | Stanwyck Winding<br>Div. San Fernando Electric Mfg. Co.<br>Newborgh, NY |
| 79727 | C–W Industries<br>P.O. Box 96<br>550 Davisville Road<br>Warminister, PA 18974 |
| 79963 | Zierick Mfg. Co.<br>Radio Circle<br>Mt. Kisco, NY 10549 |
| 80294 | Bourns Inc.<br>Instrument Division<br>6135 Magnolia Avenue<br>Riverside, CA 92506 |
| 81349 | MIL STD |
| 81483 | International Rectifier Corp.<br>9220 Sunset Blvd.<br>Los Angeles, CA 90069 |
| 82389 | Switchcraft Inc.<br>5555 N. Elston Ave.<br>Chicago, IL 60630 |
| 83186 | Victory Engineering Corp.<br>128 Springfield Ave.<br>Springfield, NJ 07081 |
| 83330 | Herman H. Smith Inc.<br>812 Snediker AVenue<br>Brooklyn, NY 11207 |
| 86445 | Penn Fibre & Specialty Co.<br>2032 E. Westmoreland St.<br>Philadelphia, PA 19134 |
| 86684 | RCA Corp.<br>Electronic Components<br>415 S. 5th Street<br>Harrison, NJ 07029 |
| 86797 | Rogan Corp.<br>3455 Woodhead Drive<br>Northbrook, IL 60062 |
| 86928 | Seastrom Mfg. Co. Inc.<br>701 Sonora Avenue<br>Glendale, CA 91201 |
| 88245 | Litton Systems Inc.<br>USECO Division<br>13536 Saticoy Street<br>Van Nuys, CA 91409 |
| 91418 | Radio Materials Co.<br>4242 W. Bryn Mawr<br>Chicago, IL 60646 |

## TABLE 6-1 MANUFACTURER'S CODE-TO-NAME INDEX (Cont'd)

| Code | Name & Address |
|---|---|
| 91673 | Epiphone Inc.<br>New York, NY |
| 91836 | Kings Electronics Co. Inc.<br>40 Marbledale Road<br>Tuckahoe, NY 10707 |
| 96067 | Microwave Associates West<br>999 E. Arques Avenue<br>Sunnyvale, CA 94086 |
| 95987 | Weckesser Co. Inc.<br>4444 W. Irving Park Road<br>Chicago, IL 60641 |
| 96733 | San Fernando Electric Mfg. Co.<br>1509 First Street<br>San Fernando, CA 91341 |
| 96906 | MIL STD |
| 98291 | Sealectro Corp.<br>225 Hoyt<br>Mamaroneck, NY 10544 |
| 99800 | American Precision Industries Inc.<br>Delevan Division<br>270 Quaker Road<br>E. Aurora, NY 14052 |

# REPLACEABLE PARTS LIST

| TITLE | MODEL 6054B FINAL ASSEMBLY #067087 Rev $B_3$ (Figure 7-1) | | | | | |
|---|---|---|---|---|---|---|
| ITEM | REF | COMPONENT DESCRIPTION | MFR'S CODE | MANUFACTURER'S PART NUMBER | SD STOCK NUMBER | T/Q |
| | | ASSEMBLY, Test | 52542 | 057164 | 057164 | 1 |
| | A28 | ASSEMBLY, Digital Extender | 52542 | 05502901 | 05502901 | 1 |
| | A29 | ASSEMBLY, ACTO Extender Assembly | 52542 | 05502801 | 05502801 | 1 |
| | | WINDOW | 52542 | 049695 | 049695 | 1 |
| | | SHIELD, Window | 52542 | 049596 | 049596 | 1 |
| | | INSERT, Trim Strip | 52542 | 055687 | 055687 | 1 |
| | | STRIP, Trim | 52542 | 04177311 | 04177311 | 1 |
| | | TRIM, Bottom Front | 52542 | 033762 | 033762 | 1 |
| | | TRIM, Top Front | 52542 | 053951 | 053951 | 1 |
| | | COVER, Top | 52542 | 06748802 | 06748802 | 1 |
| | | COVER, Bottom | 52542 | 06748801 | 06748801 | 1 |
| | | FOOT | 52542 | 067498 | 067498 | 4 |
| | | BAIL | 52542 | 067499 | 067499 | 1 |
| | | TRIM, Side | 52542 | 067469 | 067469 | 2 |
| | | LINE CORD | 70903 | BR1736 | 117644 | 1 |
| | | SCREW, FHMS 2-56 x 1/4 | 96906 | NAS662C2R4 | 10070004 | 3 |
| | | SCREW, PHMS 4-40 x 1/4 | 96906 | MS51957-13 | 10062604 | 4 |
| | | SCREW, PHMS 4-40 x 9/16 | 08547 | By Description | 100835 | 2 |
| | | SCREW, FHMS 6-32 x 7/16 | 96906 | MS24693-C27 | 10073107 | 8 |
| | | SCREW, FHMS 8-32 x 1/4 | 96906 | MS24693-C46 | 10074304 | 12 |
| | | SCREW, FHMS 8-32 x 1/2 | 96906 | MS24693-C50 | 10074308 | 4 |
| | | SCREW, FHMS 8-32 x 5/8 | 96906 | MS24693-C51 | 10074310 | 4 |
| | | WASHER, Flat #4 | 96906 | MS15795-803 | 100703 | 4 |
| | | WASHER, Split-Lock #4 | 96906 | MS35338-135 | 100711 | 6 |
| | | **OPTIONS** | | | | |
| | | OPTION 04, BCD System Interface | 52542 | 055500 | 055500 | 1 |
| | | OPTION 05, IEEE 488 System Interface | 52542 | 057359 | 057359 | 1 |
| | | OPTION 11, High Stability Oscillator | 52542 | 05545201 | 05545201 | 1 |
| | | OPTION 12, High Stability Oscillator | 52542 | 05545202 | 05545202 | 1 |
| | | OPTION 13, High Stability Oscillator | 52542 | 05545203 | 05545203 | 1 |
| | | OPTION 18, 18 GHz Operation | 52542 | 057549 | 057549 | 1 |
| | | OPTION 19, APC-7 Connector | 52542 | 057550 | 057550 | 1 |
| | | OPTION 20, Rear Panel Inputs | 52542 | 057379 | 057379 | 1 |
| | | OPTION 26.5, 26.5 GHz Operation | 52542 | 067194 | 067194 | 1 |
| | | OPTION 27, 50-60/400 Hz Operations | 52542 | 055515 | 055515 | 1 |
| | | OPTION 28, IF Offsets | 52542 | 067674 | 067674 | 1 |
| | | RACK MOUNT, Optional | 52542 | 076501 | 076501 | 1 |
| | | IF ACTO MODULE, Optional (Test Cover Accessory) | 52542 | 055625 | 055625 | 1 |

## REPLACEABLE PARTS LIST

TITLE **MODEL 6054B TEST ASSEMBLY #057164 Rev $M_2$ (Figure 7-42)**

| ITEM | REF | COMPONENT DESCRIPTION | MFR'S CODE | MANUFACTURER'S PART NUMBER | SD STOCK NUMBER | T/Q |
|---|---|---|---|---|---|---|
| 1 | | ASSEMBLY, Universal Chassis | 52542 | 057496 | 057496 | 1 |
| 2 | | ASSEMBLY, Front Panel | 52542 | 057162 | 057162 | 1 |
| 4 | A1 | ASSEMBLY, Decade MSD PC | 52542 | 05394301 | 05394301 | 1 |
| 5 | A3 | ASSEMBLY, Decade LSD PC | 52542 | 05394401 | 05394401 | 1 |
| 6 | A4 | ASSEMBLY, 500 MHz Decade PC | 52542 | 05331301 | 05331301 | 1 |
| 7 | A9 | ASSEMBLY, 10 kHz Generator PC | 52542 | 05334201 | 05334201 | 1 |
| 8 | A12 | ASSEMBLY, 20 MHz Amp PC | 52542 | 05341201 | 05341201 | 1 |
| 9 | A13 | ASSEMBLY, Display PC | 52542 | 05326301 | 05326301 | 1 |
| 10 | A22 | ASSEMBLY, 500 MHz Pre Amp PC | 52542 | 06748401 | 06748401 | 1 |
| 11 | AT1 | ATTENUATOR, 6 dB | 52542 | 05542806 | 05542806 | 1 |
| 12 | | ADAPTOR, Rt. Angle Plug/Jack | 16733 | 705979 | 705979 | 1 |
| 13 | | BRACKET, Mtg. Connector | 52542 | 057445 | 057445 | 1 |
| 18 | | SCREW, FHMS 8-32 x 1/4 | 96906 | MS24693-C46 | 10074304 | 6 |
| 20 | | SCREW, PHMS 4-40 x 1/4 | 96906 | MS51957-13 | 1--62604 | 2 |
| 21 | | WASHER, Flat #4 | 96906 | MS15795-805 | 100704 | 2 |
| 22 | | WASHER, Split-Lock #4 | 96906 | MS35338-135 | 100711 | 2 |
| 23 | | SCREW, PHMS 6-32 x 5/16 | 96906 | MS51957-27 | 10063208 | 2 |
| 24 | | WASHER, Flat #6 | 86928 | 5710-23-10 | 100662 | 2 |
| 25 | | WASHER, Split-Lock #6 | 96906 | MS35338-136 | 100712 | 2 |
| 26 | | SPACER, 8-3/16 L x 1/4 round | 06540 | 9223B-171-34 | 101018 | 2 |

## REPLACEABLE PARTS LIST

TITLE MODEL 6054B UNIVERSAL CHASSIS ASSEMBLY #057496 Rev H (Figure 7-43)

| ITEM | REF | COMPONENT DESCRIPTION | MFR'S CODE | MANUFACTURER'S PART NUMBER | SD STOCK NUMBER | T/Q |
|---|---|---|---|---|---|---|
| 1 | | ASSEMBLY, Main Chassis | 52542 | 057163 | 057163 | 1 |
| 2 | A27 | ASSEMBLY, Interconnect PC | 52542 | 05344001 | 05344001 | 1 |
| 3 | | ASSEMBLY, Rear Panel | 52542 | 055115 | 055115 | 1 |
| 4 | A25 | ASSEMBLY, Diode PC | 52542 | 05389001 | 05389001 | 1 |
| 5 | | GUSSET, Left | 52542 | 053421 | 053421 | 1 |
| 6 | | ASSEMBLY, Transformer Chassis | 52542 | 055116 | 055116 | 1 |
| 7 | | CAGE, Front Card | 52542 | 053423 | 053423 | 1 |
| 8 | | INSULATOR, Mtg. Plate Capacitor | 52542 | 075286 | 075286 | 1 |
| 10 | A6 | ASSEMBLY, IF Integrator PC | 52542 | 05336901 | 05336901 | 1 |
| 11 | A8 | ASSEMBLY, Timebase PC | 52542 | 05337901 | 05337901 | 1 |
| 12 | A10 | ASSEMBLY, N Computer PC | 52542 | 05736401 | 05736401 | 1 |
| 13 | A11 | ASSEMBLY, Function PC | 52542 | 05338601 | 05338601 | 1 |
| 15 | A14 | ASSEMBLY, N IF ACTO Module | 52542 | 055369 | 055369 | 1 |
| 16 | A15 | ASSEMBLY, Search Osc. ACTO Module | 52542 | 055370 | 055370 | 1 |
| 17 | A16 | ASSEMBLY, LO/Shifter ACTO Module | 52542 | 057167 | 057167 | 1 |
| 18 | A17 | ASSEMBLY, Lock IF ACTO Module | 52542 | 055367 | 055367 | 1 |
| 20 | U2 | DETECTOR, Power Divider & | 52542 | 055841 | 055841 | 1 |
| 21 | U1 | PIN LEVELER | 50436 | 33102A | 103203 | 1 |
| 25 | | GUIDE, PC Modification | 52542 | 053424 | 053424 | 1 |
| 26 | | GUIDE, PC | 52542 | 02134011 | 02134011 | 11 |
| 27 | | CABLE, Semirigid Coax | 52542 | 055211 | 055211 | 1 |
| 28 | | CABLE, Semirigid Coax | 52542 | 055212 | 055212 | 2 |
| 29 | | ASSEMBLY, Coax Cable | 52542 | 055365 | 055365 | 1 |
| 30 | | ASSEMBLY, Coax Cable | 52542 | 055357 | 055357 | 5 |
| 31 | | ADAPTER, Rt. Angle Plug/Plug | 16733 | 705976-001 | 103305 | 1 |
| 32 | AT2 | TERMINATION, 50Ω | 16179 | 2002CP | 102969 | 1 |
| 34 | | ASSEMBLY, Chassis Cable | 52542 | 055306 | 055306 | 1 |
| 35 | | PLUG, 5-pos. (P/O Item 34) | 27264 | 03-06-2055 | 101263 | 1 |
| 36 | | RECEPTACLE, 5-pos (P/O Item 34) | 27264 | 03-06-1055 | 101264 | 1 |
| 37 | | PIN, Connector Male | 27264 | 02-06-2103 | 10282202 | 4 |
| 39 | | BUSHING, Snap | 28520 | SB-437-5 | 100820 | 1 |
| 40 | | CLAMP, Cable 5/16 | 95987 | 5/16-4NA | 100717 | 3 |
| 41 | | CLAMP, Cable 3/16 | 95987 | 3716 | 102931 | 2 |
| 42 | | TIE, Cable | 06383 | SS11.51 | 101115 | 1 |
| 43 | | SCREW, PHMS 4-40 x 5/16 | 96906 | MS51957-14 | 10062605 | 1 |
| 44 | | SCREW, PHMS 6-32 x 5/16 | 96906 | MS51957-27 | 10063205 | 16 |
| 45 | | SCREW, PHMS 6-32 x 3/8 | 96906 | MS51957-28 | 10063206 | 5 |
| 46 | | SCREW, PHMS 6-32 x 7/16 | 96906 | MS51957-29 | 10063207 | 2 |
| 47 | | SCREW, FHMS 6-32 x 5/16 | 96906 | MS24693-C25 | 10073105 | 6 |
| 48 | | SCREW, FHMS 6-32 x 3/8 | 73734 | 22444 | 100677 | 1 |
| 50 | | SCREW, FHMS 8-32 x 5/16 | 96906 | MS24693-C47 | 10074305 | 6 |
| 52 | | SCREW, PHMS 10-32 x 3/8 | 96906 | MS51957-61 | 10064406 | 8 |
| 54 | | WASHER, Flat #6 | 86928 | 5710-23-10 | 100662 | 8 |

## REPLACEABLE PARTS LIST

TITLE MODEL 6054B UNIVERSAL CHASSIS ASSEMBLY #057496 (Cont'd)

| ITEM | REF | COMPONENT DESCRIPTION | MFR'S CODE | MANUFACTURER'S PART NUMBER | SD STOCK NUMBER | T/Q |
|---|---|---|---|---|---|---|
| 55 | | WASHER, Split-Lock #6 | 96906 | MS35338-136 | 100712 | 19 |
| 56 | | WASHER, Flat #8 | 96906 | MS15795-807 | 100705 | 12 |
| 57 | | NUT, Kep 6-32 | 78189 | 511-061800-01 | 112472 | 8 |
| 58 | | WASHER, Internal Tooth | 78189 | 1218-02-CAD | 101118 | 8 |
| 59 | | NUT, Kep 4-40 | 78189 | 511-041800-00 | 100941 | 1 |

## REPLACEABLE PARTS LIST

TITLE **MAIN CHASSIS ASSEMBLY #057163 Rev H (Figure 7-44)**

| ITEM | REF | COMPONENT DESCRIPTION | MFR'S CODE | MANUFACTURER'S PART NUMBER | SD STOCK NUMBER | T/Q |
|---|---|---|---|---|---|---|
| 1 | | CHASSIS, Main | 52542 | 053416 | 053416 | 1 |
| 2 | | PLATE, Counter PS Regulator Mtg. | 52542 | 053942 | 053942 | 1 |
| 3 | | PLATE, ACTO PS Regulator Mtg. | 52542 | 053934 | 053934 | 1 |
| 4 | A24 | ASSEMBLY, ACTO PS Regulator PC | 52542 | 05393301 | 05393301 | 1 |
| 5 | A23 | ASSEMBLY, Counter PS Regulator PC | 52542 | 05394101 | 05394101 | 1 |
| 6 | | NUT, Hex 6-32 | 96906 | NAS671C6 | 100638 | 8 |
| 7 | U3,U4 | SAMPLER | 52542 | 057169 | 057169 | 2 |
| 8 | Q1 | TRANSISTOR, SIPNP 60V | 04713 | MJ2500 | 102889 | 1 |
| 9 | Q2 | TRANSISTOR, SINPN 60V | 04713 | MJ3000 | 103068 | 1 |
| 10 | Q3 | TRANSISTOR, SINPN 40V | 04713 | 2N5190 | 101394 | 1 |
| 11 | Q4 | TRANSISTOR, SIPNP 40V | 04713 | 2N5193 | 101405 | 1 |
| 12 | U1 | INTEGRATED CIRCUIT<br>Voltage Regulator 5V | 27014 | LM309K | 025787 | 1 |
| 13 | U2 | INTEGRATED CIRCUIT<br>Voltage Regulator | 27014 | LM320K-5.2K | 103064 | 1 |
| 14 | | PLATE, Capacitor Mtg. | 52542 | 053843 | 053843 | 1 |
| 15 | U4,U9 | INTEGRATED CIRCUIT<br>Voltage Regulator -15V | 04713 | MC7915CT | 103040 | 2 |
| 16 | U5,U8 | INTEGRATED CIRCUIT<br>Voltage Regulator 15V | 04713 | MC7815CT | 103039 | 2 |
| 17 | U6 | INTEGRATED CIRCUIT<br>Voltage Regulator 5V | 04713 | MC7805CT | 045256 | 1 |
| 18 | U7 | INTEGRATED CIRCUIT<br>Voltage Regulator -5.2V | 04713 | MC7905.2CT | 103033 | 1 |
| 19 | | INSULATOR | 08289 | MW 500 125 002 | 112003 | 2 |
| 20 | | SPACER, Capacitor Mtg. | 52542 | 053917 | 053917 | 2 |
| 21 | | WASHER, Flat #6 | 96906 | MS35337-77 | 100662 | 8 |
| 22 | | LUG, #6 | 83330 | 1413-6 | 100486 | 4 |
| 23 | XA14-17 | CONNECTOR, PC 20-pin | 05574 | 2VK10D/1-2 | 101253 | 4 |
| 24 | | BUSHING, Snap | 28520 | SB-587-9 | 103003 | 1 |
| 25 | | SPACER, 4-40 x 7/8 | 06540 | 8110A-0440-17 | 100905 | 8 |
| 27 | | KEY, Polarizing | 05574 | 091-0024-000 | 100808 | 4 |
| 28 | | SCREW, PHMS 4-40 x 3/16 | 96906 | MS51957-12 | 10062603 | 4 |
| 29 | | SCREW, PHMS 4-40 x 1/4 | 96906 | MS51957-13 | 10062604 | 27 |
| 30 | | SCREW, PHMS 4-40 x 3/16 | 96906 | MS24693-C1 | 10072003 | 7 |
| 31 | | SCREW, PHMS 4-40 x 7/16 | 96906 | MS51957-16 | 10062607 | 8 |
| 32 | | SCREW, PHMS 6-32 x 7/16 | 96906 | MS51957-29 | 10063207 | 8 |
| 33 | | SCREW, PHMS 6-32 x 5/16 | 96906 | MS24693-C25 | 10073105 | 4 |
| 34 | | WASHER, Ins. Shoulder | 02735 | DF137A | 103397 | 3 |
| 35 | | WASHER, Flat #4 | 96906 | MS15795-803 | 100703 | 14 |
| 36 | | WASHER, Split-Lock #4 | 96906 | MS35338-135 | 100711 | 30 |
| 37 | | INSULATOR, Mica | 08289 | SM-115 | 112563 | 4 |

## REPLACEABLE PARTS LIST

**TITLE** **MAIN CHASSIS ASSEMBLY #057163 (Cont'd)**

| ITEM | REF | COMPONENT DESCRIPTION | MFR'S CODE | MANUFACTURER'S PART NUMBER | SD STOCK NUMBER | T/Q |
|---|---|---|---|---|---|---|
| 38 | | INSULATOR | 08289 | SK-73-48-13 | 103352 | 6 |
| 39 | | SCREW, PHMS 4-40 x 5/16 | 96906 | MS51957-14 | 10062605 | 2 |
| 40 | | LUG, Solder #4 | 12517 | ITA332JSN W/SLV | 100509 | 1 |
| 41 | | SCREW, FHMS 8-32 x 3/8 | 96906 | MS24693-C48 | 10074306 | 2 |
| 42 | | SCREW, PHMS 8-32 x 3/8 | 96906 | MS51957-43 | 10064206 | 2 |
| 43 | | LUG, Solder #8 | 78189 | 2104-08-00 | 102961 | 4 |
| 44 | C1 | CAPACITOR, Tant 1 µF 10%, 50V | 56289 | 150D105X0050A2 | 103275 | 1 |
| 45 | | WASHER, Split-Lock #8 | 96906 | MS35338-137 | 100713 | 1 |
| 46 | C3,C4 | CAPACITOR, El Can (P/O Diode Assy) | | | | |
| 47 | C1,C2 | CAPACITOR, El Can (P/O Diode Assy) | | | | |
| 48 | | WASHER, Split-Lock #6 | 96906 | MS35338-136 | 100712 | 4 |
| 49 | | GUSSET, Right | 52542 | 053420 | 053420 | 1 |
| 51 | | SPACER, 4-40 x 3/36 | 06540 | 9723-B-0440-3A | 117154 | 4 |
| 53 | C3 | CAPACITOR, Tant 1 µF 10%, 35V | 56289 | 150D107X9010R2 | 100082 | 1 |
| 54 | C2,C4 | CAPACITOR, Tant 100 µF 20%, 20V | 56289 | 150D105X9035A2 | 100119 | 2 |
| 55 | R1,R2 | RESISTOR, WW 2 Ω 5%, 5W | 56289 | 240E2R05 | 101772 | 2 |

## REPLACEABLE PARTS LIST

TITLE **INTERCONNECT PC ASSEMBLY #05344001 Rev B (Figure 7-45)**

| ITEM | REF | COMPONENT DESCRIPTION | MFR'S CODE | MANUFACTURER'S PART NUMBER | SD STOCK NUMBER | T/Q |
|---|---|---|---|---|---|---|
| 11 | XA1-13 | CONNECTOR, PC 18-pos | 05574 | 2VK18D14-12 | 103190 | 24 |
| 13 | | KEY, Polarizing used on XA1 - XA12 | 05574 | 091-0024-000 | 100808 | 12 |
| 15 | | TERMINAL, Swage | 88245 | 1309B-1 | 100508 | 10 |
| 16 | | TERMINAL, Swage | 88245 | 2000B | 100482 | 18 |
| 18 | W1-W4 | JUMPER, Molded | 55210 | L-2007-1 | 102879 | 4 |
| 7 | | BOARD, PC | 52542 | 053440 | 053440 | 1 |

## REPLACEABLE PARTS LIST

TITLE FRONT PANEL ASSEMBLY #057162 Rev $C_1$ (Figure 7-46)

| ITEM | REF | COMPONENT DESCRIPTION | MFR'S CODE | MANUFACTURER'S PART NUMBER | SD STOCK NUMBER | T/Q |
|---|---|---|---|---|---|---|
| 1 | | PANEL, Sub | 52542 | 053427 | 053427 | 1 |
| 2 | | PANEL, Decorative | 52542 | 053426 | 053426 | 1 |
| 3 | | BRACKET, Left Switch Mtg. | 52542 | 05343402 | 05343402 | 1 |
| 4 | | BRACKET, Right Switch Mtg. | 52542 | 05343401 | 05343401 | 1 |
| 5 | J1 | CONNECTOR, Type N | 16179 | 21011 | 101185 | 1 |
| 6 | J2 | ASSEMBLY, Coaxial w/connector | 52542 | 055354 | 055354 | 1 |
| 7 | S3 | SWITCH, Rotary | 52542 | 039655 | 039655 | 1 |
| 8 | S4 | SWITCH, Pushbutton 6-pos | 52542 | 055106 | 055106 | 1 |
| 9 | S1 | SWITCH, SPDT Toggle w/dressnut | 09353 | 7101PNP Dressnut | 102446 | 1 |
| 10 | S2,R1 | RESISTOR, SPST Variable w/switch | 52542 | 102103 | 102103 | 1 |
| 11 | | RING, LED Blank Mtg. | 50522 | MP52 | 10320001 | 2 |
| 12 | DS1 | DIODE, LED Red | 50522 | MV5753 | 117227 | 1 |
| 13 | DS2 | DIODE, LED Green w/clear Mtg. Ring | 50522 | MV5253w/MTGGRM | 103202 | 1 |
| 14 | | KNOB, Rectangular Skirt 1/4S | 86797 | 70-2WD-2G | 100694 | 1 |
| 15 | | KNOB, Rectangular Skirt 1/8S | 07933 | 50-2WD-1G | 102764 | 1 |
| 16 | | SCREW, PHMS 2-56 x 1/4 | 96906 | MS51957-3 | 10062504 | 2 |
| 17 | | SCREW, FHMS 4-40 x 5/16 | 96906 | MS24693-C3 | 10072005 | 6 |
| 18 | | WASHER, Split-Lock #2 | 96906 | MS35337-77 | 100661 | 2 |
| 19 | | NUT, Hex 2-56 | 96906 | MS35649-224 | 100636 | 2 |
| 20 | | NUT, Kep 4-40 | 78189 | 511-041800-00 | 100941 | 10 |
| 22 | | WASHER, Internal Tooth 3/8 | 78189 | 1220-02 CAD | 100665 | 1 |

## REPLACEABLE PARTS LIST

TITLE REAR PANEL ASSEMBLY #055115 Rev D$_1$ (Figure 7-47)

| ITEM | REF | COMPONENT DESCRIPTION | MFR'S CODE | MANUFACTURER'S PART NUMBER | SD STOCK NUMBER | T/Q |
|---|---|---|---|---|---|---|
| 1 | | PANEL, Rear | 52542 | 053418 | 053418 | 1 |
| 2 | | PLATE, BCD Cover & Remove | 52542 | 055229 | 055229 | 1 |
| 3 | | PLATE, Cover Rear Input | 52542 | 055018 | 055018 | 1 |
| 4 | | FILTER, Air | 52542 | 055656 | 055656 | 1 |
| 5 | | FILTER, Air Retainer | 52542 | 055654 | 055654 | 1 |
| 6 | B1 | BLOWER, 50-60 Hz | 23926 | 8500 | 100887 | 1 |
| 7 | | SPACER, Fuse Post | 52542 | 067464 | 067464 | 2 |
| 8 | J3,5,6 | RECEPTICAL, RF BNC | 81349 | UG-1094/U | 101155 | 3 |
| 9 | | LUG, BNC Solder Ground | 79963 | 814 | 107077 | 3 |
| 10 | S5 | SWITCH, SPDT Slide | 52542 | 117574 | 117574 | 1 |
| 11 | S6 | SWITCH, 4PDT Slide | 82389 | 47227LF NO BARS | 102329 | 1 |
| 12 | XF1,2 | POST, Fuse | 75915 | 342025 | 117973 | 2 |
| 13 | F2 | FUSE, .25A | 71400 | MIL 1/4 | 100600 | 1 |
| 14 | F1 | FUSE, 1.5A | 75915 | 31301.5 | 100591 | 1 |
| 15 | | LABEL, Model & Serial Number | 52542 | 03711201 | 03711201 | 1 |
| 16 | | FILTER, Line | 02777 | F85417 | 117643 | 1 |
| 17 | | LUG, Ground #4 | 83330 | 1416-4 | 100509 | 1 |
| 18 | | RIVET, Tubular | 12014 | R-3472X1/8NICL | 100645 | 2 |
| 19 | | RIVET, .088 Dia x .125 Long | 12014 | R-2484X1/8NICL | 100924 | 2 |
| 20 | | SCREW, PHMS 2-56 x 1/4 | 96906 | MS51957-3 | 10062504 | 4 |
| 21 | | SCREW, PHMS 4-40 x 1/4 | 96906 | MS51957-13 | 10062604 | 2 |
| 22 | | SCREW, PHMS 4-40 x 3/8 | 96906 | MS51957-15 | 10062606 | 4 |
| 24 | | WASHER, Split-Lock #6 | 96906 | MS35338-136 | 100712 | 4 |
| 25 | | WASHER, Split-Lock #4 | 96906 | MS35338-135 | 100711 | 3 |
| 26 | | WASHER, Split-Lock #2 | 96906 | MS35337-77 | 100661 | 4 |
| 27 | | WASHER, Flat #4 | 96906 | MS15795-803 | 100703 | 4 |
| 28 | | NUT, Hex 6-32 | 96906 | NAS35649-224 | 100638 | 4 |
| 29 | | NUT, Hex 4-40 | 96906 | NAS671C4 | 100622 | 2 |
| 30 | | NUT, Kep 4-40 | 78189 | 511-041800-00 | 100914 | 2 |

## REPLACEABLE PARTS LIST

TITLE **TRANSFORMER CHASSIS ASSEMBLY #055116 Rev $B_2$ (Figure 7-36)**

| ITEM | REF | COMPONENT DESCRIPTION | MFR'S CODE | MANUFACTURER'S PART NUMBER | SD STOCK NUMBER | T/Q |
|---|---|---|---|---|---|---|
| 1 | | CHASSIS, Transformer | 52542 | 053417 | 053417 | 1 |
| 2 | A26 | ASSEMBLY, Time Base Oscillator PC | 52542 | 06738201 | 06738201 | 1 |
| 3 | | PLATE, Oscillator Cover | 52542 | 055104 | 055104 | 1 |
| 4 | T1 | TRANSFORMER | 52542 | 053698 | 053698 | 1 |
| 5 | | BUSHING, Snap 1/2 | 28520 | SB-500-6 | 100680 | 1 |
| 6 | | GUIDE, PC | 52542 | 02134011 | 02134011 | 12 |
| 7 | | PLATE, Transformer & Cap. Cover | 52542 | 055435 | 055435 | 1 |
| 8 | | WAHSER, Flat #8 | 96906 | MS15795-807 | 100705 | 8 |
| 9 | | WASHER, Split-Lock #6 | 96906 | MS35338-136 | 100712 | 4 |
| 10 | | NUT, Kep 8-32 | 78189 | 511-081800-00 | 100940 | 4 |
| 11 | | SCREW, PHMS 6-32 x 5/8 | 96906 | MS51957-18 | 10063210 | 1 |
| 12 | | SCREW, PHMS 6-32 x 1/4 | 96906 | MS51957-26 | 10063204 | 2 |
| 13 | | SCREW, PHMS 4-40 x 1/4 | 96906 | MS51957-13 | 10062604 | 2 |
| 14 | | WASHER, Split-Lock #4 | 96906 | MS35338-135 | 100711 | 2 |
| 15 | | NUT, Kep 6-32 | 78189 | 511-061800-01 | 112472 | 1 |
| 16 | | SCREW, PHMS 6-32 x 3/4 | 96906 | MS51957-32 | 10063212 | 1 |
| | | **A26, TIMEBASE OSCILLATOR PC ASSEMBLY #06738201 Rev $A_1$ (Figure 7-37)** | | | | |
| 5 | | BOARD, PC | 52542 | 067382 | 067382 | 1 |
| 8 | U1 | OSCILLATOR, TCXO | 52542 | 057817 | 057817 | 1 |
| 15 | | SPACER, Swage 6-32 x 3/16 | 88245 | 1530 | 100511 | 4 |
| 16 | | TERMINAL, Swage | 88245 | 2000B | 100482 | 4 |
| 18 | | SCREW, PHMS 4-40 x 1/4 | 96906 | MS51957-13 | 10062604 | 2 |
| 19 | | WASHER, Flat #4 | 96906 | MS15795-803 | 100703 | 2 |
| 20 | | WASHER, Split-Lock #4 | 96906 | MS35338-135 | 100711 | 2 |
| 21 | | WASHER, Nylon | 86445 | S331-H | 100815 | 2 |

## REPLACEABLE PARTS LIST

TITLE A23, COUNTER PS REGULATOR PC ASSEMBLY #05394101 Rev $E_1$ (Figure 7-39)

| ITEM | REF | COMPONENT DESCRIPTION | MFR'S CODE | MANUFACTURER'S PART NUMBER | SD STOCK NUMBER | T/Q |
|---|---|---|---|---|---|---|
| | C1 | CAPACITOR, Tant<br>1 µF 10%, 50V | 56289 | 150D105X0050A2 | 103275 | 1 |
| | C2 | CAPACITOR, Tant<br>1 µF 10%, 35V | 56289 | 150D105X9035A2 | 100082 | 1 |
| | C3 | CAPACITOR, Tant<br>6.8 µF 10%, 35V | 56289 | 150D685X9035B | 100182 | 2 |
| | C4 | CAPACITOR, Tant<br>10 µF 10%, 20V | 56289 | 150D106X9020B2 | 100063 | 2 |
| | C5 | Same as C3 | | | | |
| | C6 | Same as C4 | | | | |
| | CR1 thru CR8 | DIODE, Rectifier 100V | 04713 | SSIM | 106555 | 8 |
| | VR1 | DIODE, Zener | 04713 | 1N964B | 100412 | 1 |
| | | SPACER, Swage 4-40 | 71279 | 1300-9 | 100492 | 2 |
| | | TERMINAL, Swage | 88245 | 2000B | 100482 | 13 |
| | | TERMINAL, Swage | 88245 | 1309B-1 | 100508 | 7 |
| | | BOARD, PC | 52542 | 053941 | 053941 | 1 |

## REPLACEABLE PARTS LIST

| TITLE | A24, ACTO PS REGULATOR PC ASSEMBLY #05393301 Rev $C_1$ (Figure 7-40) | | | | | |
|---|---|---|---|---|---|---|
| ITEM | REF | COMPONENT DESCRIPTION | MFR'S CODE | MANUFACTURER'S PART NUMBER | SD STOCK NUMBER | T/Q |
| | C1 | CAPACITOR, Tant<br>100 μF 10%, 25V | 56289 | 109D107X9025F2 | 100262 | 2 |
| | C2 | CAPACITOR, Tant<br>6.8 μF 10%, 35V | 56289 | 150D685X9035B | 100182 | 2 |
| | C3 | CAPACITOR, Tant<br>10 μF 10%, 20V | 56289 | 150D105X9020B2 | 100063 | 6 |
| | C4 | Same as C1 | | | | |
| | C5 | Same as C2 | | | | |
| | C6 thru C10 | Same as C3 | | | | |
| | R1 | RESISTOR, CC<br>100 Ω 5%, 1/4W | 01121 | CB1015 | 101609 | 2 |
| | R2 | Same as R1 | | | | |
| | | SPACER, Swage 4-40 x 1/8 | 71279 | 1300-0 | 100492 | 3 |
| | | LUG, Terminal | 88245 | 2000B | 100482 | 23 |
| | | LUG, Terminal | 88245 | 1309B-1 | 100508 | 4 |
| | | BOARD, PC | 52542 | 053933 | 053933 | 1 |

## REPLACEABLE PARTS LIST

TITLE **A25, DIODE PC ASSEMBLY #05389001 Rev $A_3$ (Figure 7-38)**

| ITEM | REF | COMPONENT DESCRIPTION | MFR'S CODE | MANUFACTURER'S PART NUMBER | SD STOCK NUMBER | T/Q |
|---|---|---|---|---|---|---|
| | CR1 thru CR4 | DIODE, Rectifier 20V | 04713 | MBR1520W/MH7-45 | 103066 | 4 |
| | | BRACKET, Diode Mtg. | 52542 | 053916 | 053916 | 1 |
| | | BUSHING, Snap 3/8 | 28520 | SB-375-4 | 100781 | 1 |
| | | SCREW, PHMS 4-40 x 3/8 | 96906 | MS51957-15 | 10062606 | 2 |
| | | WASHER, Flat #4 | 96906 | MS15795-15 | 100703 | 2 |
| | | NUT, Kep 4-40 | 78189 | 511-041800-00 | 100941 | 2 |
| | | CATERPILLAR, Nylon | 03296 | G51-HA | 102749 | A/R |
| | | NUT, Hex 10-32 | 96906 | MS35650-304 | 100709 | 4 |
| | | WASHER, Comp. #10 | 52829 | SP-115310 | 117118 | 4 |
| | | WASHER, Flat #10 | 96906 | MS15795-807 | 100705 | 4 |
| | | INSULATOR, Kit | 81483 | 40-8022 | 990350 | 4 |
| | | BOARD, PC | 52542 | 053890 | 053890 | 1 |

## REPLACEABLE PARTS LIST

TITLE **A1, MSD DECADE PC ASSEMBLY #05394301 Rev $A_1$ (Figure 7-2 & 7-3)**

| ITEM | REF | COMPONENT DESCRIPTION | MFR'S CODE | MANUFACTURER'S PART NUMBER | SD STOCK NUMBER | T/Q |
|---|---|---|---|---|---|---|
| | C1 | CAPACITOR, Ceramic .05 μF +80-20%, 10V | 71590 | UK10-503 | 100122 | 3 |
| | U1 thru U5 | INTEGRATED CIRCUIT, TTL MSI Presettable BCD Counter | 01295 | SN74LS196N | 103164 | 5 |
| | U6 | INTEGRATED CIRCUIT, TTL SSI Quad 2-Input NAND Gate | 01295 | SN7400N | 019705 | 1 |
| | U7 | INTEGRATED CIRCUIT, TTL SSI Quad 2-Input AND Gate | 01295 | SN7408N | 103093 | 1 |
| | U8 thru U12 | INTEGRATED CIRCUIT, TTL MSI 4-Bit Shift Register | 01295 | SN74LS195N | 103163 | 5 |
| | U13 | INTEGRATED CIRCUIT, TTL SSI Dual D Flip-Flop | 01295 | SN7474N | 025241 | 1 |
| | U14 | INTEGRATED CIRCUIT, TTL SSI Quad 2-Input OR Gate | 01295 | SN7423N | 045257 | 2 |
| | U15 thru U19 | INTEGRATED CIRCUIT, TTL MSI Syn BCD Up/Down Counter | 01295 | SN74LS192N | 103106 | 5 |
| | U20 | Same as U14 | | | | |
| | | EXTRACTOR | 51495 | 1743 | 100865 | 1 |
| | | EXTRACTOR, Hot Stamped A1 | 52542 | 03984201 | 03984201 | 1 |
| | | ROLL PIN | 73957 | 50-094-0250 | 100752 | 2 |
| | | BOARD, PC | 52542 | 053943 | 053943 | 1 |

## REPLACEABLE PARTS LIST

| TITLE | A3, LSD DECADE PC ASSEMBLY #05394401 Rev $A_1$ (Figure 7-4 & 7-5) | | | | | |
|---|---|---|---|---|---|---|
| ITEM | REF | COMPONENT DESCRIPTION | MFR'S CODE | MANUFACTURER'S PART NUMBER | SD STOCK NUMBER | T/Q |
| | C1 | CAPACITOR, Ceramic<br>.1 µF 20%, 50V | 56289 | 5C023104X0500C5 | 100178 | 2 |
| | C2 | Same as C1 | | | | |
| | C3 | CAPACITOR, Ceramic<br>.05 µF +80-20%, 10V | 71590 | UK10-503 | 100122 | 1 |
| | U1 | INTEGRATED CIRCUIT, TTL SSI<br>Quad 2-Input OR Gate | 01295 | SN7423N | 045257 | 1 |
| | U2 | INTEGRATED CIRCUIT, TTL MSI<br>Presettable BCD Counter | 18324 | N82S90A | 103170 | 1 |
| | U3<br>thru<br>U6 | INTEGRATED CIRCUIT, TTL MSI<br>Presettable BCD Counter | 01295 | SN74LS196N | 103164 | 4 |
| | U7 | INTEGRATED CIRCUIT, TTL SSI<br>Quad 2-Input AND Gate | 01295 | SN7408N | 103093 | 1 |
| | U8<br>thru<br>U12 | INTEGRATED CIRCUIT, TTL MSI<br>4-Bit Shift Register | 01295 | SN74LS195N | 103163 | 5 |
| | U13<br>thru<br>U18 | INTEGRATED CIRCUIT, TTL MSI<br>Syn BCD Up/Down Counter | 01295 | SN74LS192N | 103106 | 6 |
| | | EXTRACTOR | 51495 | 1743 | 100865 | 1 |
| | | EXTRACTOR, Hot Stamped A3 | 52542 | 03984203 | 03984203 | 1 |
| | | ROLL PIN | 73957 | 50-094-0250 | 100752 | 2 |
| | | BOARD, PC | 52542 | 053944 | 053944 | 1 |

## REPLACEABLE PARTS LIST

| TITLE | A4, 500 MHz DECADE & GATE PC ASSEMBLY #05331301 Rev F (Figure 7-6 & 7-7) | | | | | |
|---|---|---|---|---|---|---|
| **ITEM** | **REF** | **COMPONENT DESCRIPTION** | **MFR'S CODE** | **MANUFACTURER'S PART NUMBER** | **SD STOCK NUMBER** | **T/Q** |
| | C1 | CAPACITOR, DP Ceramic<br>.01 μF 20%, 100V | 04222 | 3429100C103M | 117570 | 17 |
| | C2 | CAPACITOR, Ceramic<br>.05 μF +80-20%, 10V | 71590 | UK10-503 | 100122 | 7 |
| | C3 | Same as C1 | | | | |
| | C4 | CAPACITOR, DP Ceramic<br>15 pF 5%, 100V | 96733 | DB44BY15J | 117624 | 6 |
| | C5 | Same as C1 | | | | |
| | C6 | Same as C1 | | | | |
| | C7 | Same as C4 | | | | |
| | C8 | Same as C1 | | | | |
| | C9 | Same as C1 | | | | |
| | C10 | Same as C4 | | | | |
| | C11 | Same as C1 | | | | |
| | C12 | CAPACITOR, Tant<br>4.7 μF 10%, 25V | 56289 | 150D475X9035B2 | 100071 | 2 |
| | C13 | Same as C1 | | | | |
| | C14 | Same as C4 | | | | |
| | C15 | Same as C1 | | | | |
| | C16 | CAPACITOR, Ceramic<br>1000 pF 20%, 50V | 71590 | CW15C102M | 100251 | 15 |
| | C17 | Same as C1 | | | | |
| | C18 | Same as C4 | | | | |
| | C19 | Same as C1 | | | | |
| | C20 | CAPACITOR, Ceramic<br>1 μF 20%, 50V | 56289 | 4C02105X0250B3 | 100176 | 1 |
| | C21 | CAPACITOR, Ceramic<br>10 pF 1 kV | 72982 | 831-00C0G0100D | 100282 | 1 |
| | C22 | Same as C16 | | | | |
| | C23 thru C25 | Same as C1 | | | | |
| | C26 | CAPACITOR, DP Ceramic<br>10 pF 5%, 10V | 96733 | DP44BY100J | 117621 | 2 |
| | C27 | Same as C4 | | | | |
| | C28 | Same as C26 | | | | |
| | C29 | Same as C1 | | | | |
| | C30 | Same as C16 | | | | |

## REPLACEABLE PARTS LIST

**TITLE** **A4, 500 MHz DECADE & GATE PC ASSEMBLY #05331301 (Cont'd)**

| ITEM | REF | COMPONENT DESCRIPTION | MFR'S CODE | MANUFACTURER'S PART NUMBER | SD STOCK NUMBER | T/Q |
|---|---|---|---|---|---|---|
| | C31 | Same as C16 | | | | |
| | C32 | Same as C1 | | | | |
| | C33 | CAPACITOR, Ceramic .1 μF 20%, 50V | 56289 | 5C023104X0500C5 | 100178 | 1 |
| | C34 | Same as C16 | | | | |
| | C35 | Same as C1 | | | | |
| | C36 thru C39 | Same as C2 | | | | |
| | C40 | Same as C16 | | | | |
| | C41 | Same as C12 | | | | |
| | C42 | Same as C2 | | | | |
| | C43 thru C50 | Same as C16 | | | | |
| | C51 | Same as C2 | | | | |
| | C52 | Same as C16 | | | | |
| | C53 | CAPACITOR, Ceramic 1000 pF 20%, 1 kV | 52542 | 117568 | 117568 | 1 |
| | CR1 | Not Used | | | | |
| | CR2 | Not Used | | | | |
| | CR3 thru CR6 | DIODE, Signal 70V | 28480 | 5082-2800 | 100442 | 6 |
| | CR7 | DIODE, Pin | 96067 | MA47600 | 100447 | 1 |
| | CR8 | Same as CR3 | | | | |
| | CR9 | Same as CR3 | | | | |
| | CR10 | DIODE, Signal 50V | 03508 | 1N4151 | 100385 | 2 |
| | CR11 | Same as CR10 | | | | |
| | L1 thru L3 | INDUCTOR, Fixed 2.7 μH 10% | 72259 | WEE-WEE-2.7 | 101327 | 3 |
| | L4 | INDUCTOR, Wire Loop | 52542 | 067637 | 067637 | 2 |
| | L5 | Same as L4 | | | | |
| | L6 | INDUCTOR, Fixed .06 μH 10% | 06560 | 10150-2 | 101322 | 1 |
| | L7 | INDUCTOR, Ferrite Bead | 52542 | 112420 | 112420 | 1 |
| | P1 | CONNECTOR, RF Plug/Cable (P/O 201) | 91836 | 875-9 | 106707 | 1 |
| | Q1 | TRANSISTOR, SINPN 15V | 04713 | 2N6304 | 103171 | 5 |

## REPLACEABLE PARTS LIST

TITLE A4, 500 MHz DECADE & GATE PC ASSEMBLY #05331301 (Cont'd)

| ITEM | REF | COMPONENT DESCRIPTION | MFR'S CODE | MANUFACTURER'S PART NUMBER | SD STOCK NUMBER | T/Q |
|---|---|---|---|---|---|---|
| | Q2 | TRANSISTOR, SINPN | 04713 | 2N5835 | 101410 | 2 |
| | Q3 | Same as Q1 | | | | |
| | Q4 | Same as Q2 | | | | |
| | Q5 thru Q7 | Same as Q1 | | | | |
| | Q8 thru Q10 | TRANSISTOR, SINPN 15V | 07263 | PN3646 | 101369 | 3 |
| | R1 | Not Used | | | | |
| | R2 | RESISTOR, CC 1 k 5%, 1/8W | 01121 | BB1025 | 101711 | 21 |
| | R3 | RESISTOR, CC 82 Ω 5%, 1/8W | 01121 | BB8205 | 101800 | 5 |
| | R4 | RESISTOR, CC 27 Ω 5%, 1/8W | 01121 | BB2705 | 101810 | 5 |
| | R5 | RESISTOR, CC 3 k 5%, 1/8W | 01121 | BB3025 | 101913 | 5 |
| | R6 | Same as R2 | | | | |
| | R7 | Same as R3 | | | | |
| | R8 | Same as R4 | | | | |
| | R9 | Same as R5 | | | | |
| | R10 | Same as R2 | | | | |
| | R11 | Same as R3 | | | | |
| | R12 | Same as R4 | | | | |
| | R13 | Same as R5 | | | | |
| | R14 | Same as R2 | | | | |
| | R15 | Same as R3 | | | | |
| | R16 | Same as R4 | | | | |
| | R17 | Same as R5 | | | | |
| | R18 | Same as R2 | | | | |
| | R19 | Same as R3 | | | | |
| | R20 | Same as R4 | | | | |
| | R21 | Same as R5 | | | | |
| | R22 | RESISTOR, CC 8.2 k 5%, 1/8W | 01121 | BB8225 | 101799 | 1 |
| | R23 | RESISTOR, Variable 10 k 20%, 1/2W | 80294 | 3339W-1-103 | 100026 | 1 |

## REPLACEABLE PARTS LIST

TITLE A4, 500 MHz DECADE & GATE PC ASSEMBLY #05331301 (Cont'd)

| ITEM | REF | COMPONENT DESCRIPTION | MFR'S CODE | MANUFACTURER'S PART NUMBER | SD STOCK NUMBER | T/Q |
|---|---|---|---|---|---|---|
| | R24 | RESISTOR, CC<br>150 Ω 5%, 1/8W | 01121 | BB1515 | 101702 | 2 |
| | R25 | Same as R2 | | | | |
| | R26 | RESISTOR, CC<br>22 Ω 5%, 1/8W | 01121 | BB2205 | 101706 | 1 |
| | R27 | Same as R24 | | | | |
| | R28 | RESISTOR, CC<br>1.8 k 5%, 1/8W | 01121 | BB1825 | 101712 | 1 |
| | R29 | RESISTOR, CC<br>3.3 k 5%, 1/8W | 01121 | BB3325 | 101713 | 2 |
| | R30 | RESISTOR, CC<br>10 Ω 5%, 1/4W | 01121 | CB1005 | 101557 | 1 |
| | R31 | RESISTOR, CC<br>1.2 k 5%, 1/8W | 01121 | BB1225 | 101969 | 1 |
| | R32 | RESISTOR, CC<br>10 Ω 5%, 1/8W | 01121 | BB1005 | 101834 | 1 |
| | R33 | RESISTOR, CC<br>51 Ω 5%, 1/8W | 01121 | BB5105 | 101815 | 1 |
| | R34 | RESISTOR, CC<br>240 k 5%, 1/8W | 01121 | BB2445 | 101954 | 1 |
| | R35 | RESISTOR, CC<br>47 k 5%, 1/8W | 01121 | BB4735 | 101694 | 2 |
| | R36 | RESISTOR, CC<br>510 k 5%, 1/8W | 01121 | BB5145 | 101956 | 1 |
| | R37 | Same as R35 | | | | |
| | R38 | RESISTOR, CC<br>470 Ω 5%, 1/8W | 01121 | BB4715 | 101709 | 1 |
| | R39 | RESISTOR, CC<br>22 k 5%, 1/4W | 01121 | CB2235 | 101572 | 1 |
| | R40 | RESISTOR, CC<br>10 k 5%, 1/8W | 01121 | BB1035 | 101697 | 3 |
| | R41 | Same as R29 | | | | |
| | R42 | RESISTOR, Variable<br>1 k 20%, 1/2W | 80294 | 3339W-1-102 | 102129 | 1 |
| | R43 | Same as R2 | | | | |
| | R44 | Same as R40 | | | | |
| | R45 | Same as R40 | | | | |
| | R46 | Same as R2 | | | | |
| | R47 | RESISTOR, CC<br>100 Ω 5%, 1/8W | 01121 | BB1015 | 101701 | 2 |

## REPLACEABLE PARTS LIST

TITLE A4, 500 MHz DECADE & GATE PC ASSEMBLY #05331301 (Cont'd)

| ITEM | REF | COMPONENT DESCRIPTION | MFR'S CODE | MANUFACTURER'S PART NUMBER | SD STOCK NUMBER | T/Q |
|---|---|---|---|---|---|---|
| | R48 | Same as R47 | | | | |
| | R49 | RESISTOR, CC<br>560 Ω 5%, 1/8W | 01121 | BB5615 | 101710 | 7 |
| | R50 | RESISTOR, CC<br>560 Ω 5%, 1/4W | 01121 | CB5615 | 101583 | 1 |
| | R51 | Same as R2 | | | | |
| | R52 | RESISTOR, CC<br>1 k 5%, 1/4W | 01121 | CB1025 | 101569 | 1 |
| | R53<br>thru<br>R57 | Same as R2 | | | | |
| | R58 | Same as R49 | | | | |
| | R59 | Same as R49 | | | | |
| | R60 | Same as R2 | | | | |
| | R61 | Same as R2 | | | | |
| | R62 | Same as R49 | | | | |
| | R63 | Same as R2 | | | | |
| | R64 | Same as R49 | | | | |
| | R65 | Same as R2 | | | | |
| | R66 | Same as R49 | | | | |
| | R67 | Same as R2 | | | | |
| | R68 | Same as R49 | | | | |
| | R69 | RESISTOR, CC<br>33 k 5%, 1/8W | 01121 | BB3335 | 101693 | 1 |
| | R70 | Same as R2 | | | | |
| | R71 | Same as R2 | | | | |
| | U1 | INTEGRATED CIRCUIT<br>Operational Amplifier | 27014 | LM301AH | 025745 | 1 |
| | U2 | INTEGRATED CIRCUIT, ECL<br>Dual D M-S Flip-Flop | 04713 | MC10231L | 045227 | 1 |
| | U3 | INTEGRATED CIRCUIT, ECL SSI<br>4-3 3 Input NOR Gate | 04713 | MC10106P | 103168 | 1 |
| | U4 | INTEGRATED CIRCUIT, ECL<br>Quad ECL/TTL Translator | 04713 | MC10124L | 045228 | 2 |
| | U5 | INTEGRATED CIRCUIT, ECL<br>Quad 2-Input NOR Gate | 04713 | MC10102P | 103025 | 1 |
| | U6 | INTEGRATED CIRCUIT, ECL MSI<br>Decade Counter 550 MHz | 52648 | SP635D | 045229 | 1 |

## REPLACEABLE PARTS LIST

TITLE **A4, 500 MHz DECADE & GATE PC ASSEMBLY #05331301 (Cont'd)**

| ITEM | REF | COMPONENT DESCRIPTION | MFR'S CODE | MANUFACTURER'S PART NUMBER | SD STOCK NUMBER | T/Q |
|---|---|---|---|---|---|---|
| | U7 | INTEGRATED CIRCUIT, ECL<br>Quad ECL/TTL Translator | 04713 | MC10125L | 045226 | 1 |
| | U8 | INTEGRATED CIRCUIT, ECL SSI<br>Triple Line Receiver | 04713 | MC10216L | 045276 | 1 |
| | U9 | Same as U4 | | | | |
| | U10 | INTEGRATED CIRCUIT, TTL SSI<br>Quad 2-Input OR Gate | 04713 | MC3003P | 025767 | 1 |
| | U11 | INTEGRATED CIRCUIT, TTL SSI<br>Quad 2-Input NAND Gate | 01295 | SN74S00N | 025785 | 1 |
| | U12 | INTEGRATED CIRCUIT<br>Resistor Module 4-12k | 52542 | 045008 | 045008 | 1 |
| | | SOCKET, IC Pin | 00779 | 7-330808-4 | 101281 | 16 |
| | | WASHER, Mylar | 86928 | 5622-9-7 | 100921 | 7 |
| | | CONNECTOR, PC | 00779 | 86090-4 | 100565 | 1 |
| | | ASSEMBLY, Coaxial Cable | 52542 | 055272 | 055272 | 1 |
| | | CONNECTOR, RF | 91836 | 875-9 | 106707 | 1 |
| | | EXTRACTOR, Hot Stamped A4 | 52542 | 03954204 | 03954202 | 1 |
| | | EXTRACTOR | 51495 | 1743 | 100865 | 1 |
| | | ROLL PIN | 73957 | 50-094-0250 | 100752 | 2 |
| | | BOARD, PC | 52542 | 053313 | 053313 | 1 |

## REPLACEABLE PARTS LIST

TITLE A6, IF INTEGRATOR PC ASSEMBLY #05336901 Rev E (Figure 7-8 & 7-9)

| ITEM | REF | COMPONENT DESCRIPTION | MFR'S CODE | MANUFACTURER'S PART NUMBER | SD STOCK NUMBER | T/Q |
|---|---|---|---|---|---|---|
| | C1 | CAPACITOR, Ceramic<br>.05 μF +80-20%, 10V | 71590 | UK10-503 | 100122 | 4 |
| | C2 | CAPACITOR, Tant<br>4.7 μF 10%, 10V | 56289 | 150D475X9010A2 | 100295 | 1 |
| | C3 thru C5 | Same as C1 | | | | |
| | C6 | CAPACITOR, Ceramic<br>.01 μF 20%, 100V | 04222 | 3429100C103M | 117570 | 1 |
| | U1 | INTEGRATED CIRCUIT, TTL SSI<br>Quad 2-Input OR Gates | 01295 | SN7432N | 045257 | 3 |
| | U2 | INTEGRATED CIRCUIT, TTL SSI<br>Quad 2-Input AND Gate | 01295 | SN7408N | 103093 | 2 |
| | U3 | INTEGRATED CIRCUIT, TTL SSI<br>Quad 2-Input NOR Gate | 04713 | MC3002P | 025739 | 2 |
| | U4 | Same as U1 | | | | |
| | U5 | Same as U3 | | | | |
| | U6 thru U9 | INTEGRATED CIRCUIT, TTL SSI<br>Dual D Flip-Flop | 01295 | SN7474N | 025241 | 4 |
| | U10 | Same as U1 | | | | |
| | U11 | Same as U2 | | | | |
| | U13 thru U15 | INTEGRATED CIRCUIT, TTL SSI<br>Dual 4-Input NOR Gate W/Strobe | 01295 | SN7425N | 045296 | 4 |
| | U16 thru U23 | INTEGRATED CIRCUIT, TTL MSI<br>Sync BCD Up/Down Counter | 01295 | SN74LS192N | 103106 | 8 |
| | U24 | INTEGRATED CIRCUIT, TTL SSI<br>Triple 3-Input AND Gate | 04713 | MC3006P | 045219 | 1 |
| | | EXTRACTOR | 51495 | 1743 | 100865 | 1 |
| | | EXTRACTOR, Hot Stamped A6 | 52542 | 03984206 | 03984206 | 1 |
| | | ROLL PIN | 73957 | 50-094-0250 | 100752 | 2 |
| | | BOARD, PC | 52542 | 053369 | 053369 | 1 |

## REPLACEABLE PARTS LIST

| TITLE | A8, TIMEBASE PC ASSEMBLY #05337901 Rev D (Figure 7-10 & 7-11) | | | | | |
|---|---|---|---|---|---|---|
| ITEM | REF | COMPONENT DESCRIPTION | MFR'S CODE | MANUFACTURER'S PART NUMBER | SD STOCK NUMBER | T/Q |
| | C1 | CAPACITOR, Ceramic<br>.01 µF +80-20%, 100V | 91418 | TA110 | 117570 | 2 |
| | C2 thru C9 | CAPACITOR, Ceramic<br>.05 µF +80-20%, 10V | 71590 | UK10-503 | 100122 | 8 |
| | C10 | CAPACITOR, Tant<br>4.7 µF 10%, 35V | 56289 | 150D475X9035B2 | 100071 | 1 |
| | C11 | Same as C1 | | | | |
| | C12 | CAPACITOR, DM<br>22 pF 5%, 500V | 72136 | DM15ED220J0 | 100068 | 1 |
| | C13 | CAPACITOR, Ceramic<br>.001 µF 20%, 50V | 71590 | CW15C102M | 100251 | 1 |
| | CR1 | DIODE, Signal 50V | 03508 | 1N4151 | 100385 | 2 |
| | CR2 | Same as CR1 | | | | |
| | Q1 | TRANSISTOR, SINPN | 07263 | 2N4275 | 102716 | 2 |
| | Q2 | Same as Q1 | | | | |
| | R1 | RESISTOR, CC<br>10 k 5%, 1/4W | 01121 | CB1035 | 101570 | 3 |
| | R2 | RESISTOR, CC<br>680 Ω 5%, 1/4W | 01121 | CB6815 | 101669 | 2 |
| | R3 | RESISTOR, CC<br>12 k 5%, 1/4W | 01121 | CB1235 | 101565 | 2 |
| | R4 | RESISTOR, CC<br>470 Ω 5%, 1/4W | 01121 | CB4715 | 101625 | 2 |
| | R5 | Same as R1 | | | | |
| | R6 | Same as R1 | | | | |
| | R7 | Same as R2 | | | | |
| | R8 | Same as R3 | | | | |
| | R9 | Same as R4 | | | | |
| | R10 | RESISTOR, CC<br>22 k 5%, 1/4W | 01121 | CB2235 | 101572 | 2 |
| | R11 | Same as R10 | | | | |
| | U1 thru U3 | INTEGRATED CIRCUIT, TTL SSI<br>Dual 4-Input NOR Gate W/Strobe | 01295 | SN7425N | 045296 | 3 |
| | U4 | INTEGRATED CIRCUIT, TTL SSI<br>Dual D Flip-Flop | 01295 | SN74LS74N | 103132 | 1 |
| | U5 | INTEGRATED CIRCUIT, TTL MSI<br>Presettable BCD Counter | 01295 | SN74LS196N | 103164 | 1 |

## REPLACEABLE PARTS LIST

TITLE A8, TIMEBASE PC ASSEMBLY #05337901 (Cont'd)

| ITEM | REF | COMPONENT DESCRIPTION | MFR'S CODE | MANUFACTURER'S PART NUMBER | SD STOCK NUMBER | T/Q |
|---|---|---|---|---|---|---|
| | U6 | INTEGRATED CIRCUIT, TTL SSI<br>8-Input NAND Gate | 01295 | SN7430N | 025726 | 1 |
| | U7 | INTEGRATED CIRCUIT, TTL SSI<br>Quad 2-Input OR Gate | 01295 | SN7432N | 045257 | 1 |
| | U8<br>thru<br>U13 | INTEGRATED CIRCUIT, TTL MSI<br>Syn BCD Up/Down Counter | 01295 | SN74LS192N | 103106 | 6 |
| | U14 | INTEGRATED CIRCUIT, TTL SSI<br>Quad 2-Input AND Gate | 01295 | SN7408N | 103093 | 3 |
| | U15 | INTEGRATED CIRCUIT, TTL SSI<br>Quad 2-Input NAND Gate | 01295 | SN74132N | 045270 | 1 |
| | U16 | INTEGRATED CIRCUIT, TTL SSI<br>Dual AND/OR Inverter | 01295 | SN7451N | 025707 | 1 |
| | U17 | Same as U14 | | | | |
| | U18 | Same as U14 | | | | |
| | U19 | INTEGRATED CIRCUIT, TTL SSI<br>Quad 2-Input EX/OR Gate | 01295 | SN74LS86 | 103975 | 1 |
| | U20 | INTEGRATED CIRCUIT, TTL SSI<br>Dual Retriggerable 1-Shot Multivibrator | 04713 | SN74LS123 | 103976 | 1 |
| | U21 | INTEGRATED CIRCUIT, TTL SSI<br>Dual D Flip-Flop | 01295 | SN7474N | 025241 | 1 |
| | | EXTRACTOR | 51495 | 1743 | 100865 | 1 |
| | | EXTRACTOR, Hot Stamped A8 | 52542 | 03984208 | 03984208 | 1 |
| | | ROLL PIN | 73957 | 50-094-0250 | 100752 | 2 |
| | | BOARD, PC | 52542 | 053379 | 053379 | 1 |

## REPLACEABLE PARTS LIST

TITLE **A9, 10 kHz GENERATOR PC ASSEMBLY #05334201 Rev B (Figure 7-12 & 7-13)**

| ITEM | REF | COMPONENT DESCRIPTION | MFR'S CODE | MANUFACTURER'S PART NUMBER | SD STOCK NUMBER | T/Q |
|---|---|---|---|---|---|---|
| | C1 | CAPACITOR, Ceramic<br>1000 pF 20%, 50V | 71590 | CW15C102M | 100251 | 12 |
| | C2 | CAPACITOR, Ceramic<br>1 μF 20%, 25V | 56289 | 4C02105X0250B3 | 100176 | 1 |
| | C3 | CAPACITOR, Tant<br>4.7 μF 10%, 35V | 56289 | 150D475X9035B2 | 100071 | 2 |
| | C4 thru C9 | CAPACITOR, Ceramic<br>.05 μF +80-20%, 10V | 71590 | UK10-503 | 100122 | 9 |
| | C10 | Same as C3 | | | | |
| | C11 thru C13 | Same as C4 | | | | |
| | C14 thru C24 | Same as C1 | | | | |
| | CR1 | DIODE, Signal 70V | 28480 | 5082-2800 | 100442 | 2 |
| | CR2 | Same as CR1 | | | | |
| | R1 | RESISTOR, CC<br>560 Ω 5%, 1/4W | 01121 | CB5615 | 101583 | 2 |
| | R2 | Same as R1 | | | | |
| | R3 thru R7 | RESISTOR, CC<br>47 k 5%, 1/4W | 01121 | BB4735 | 101694 | 5 |
| | R8 thru R17 | RESISTOR, CC<br>560 Ω 5%, 1/8W | 01121 | BB5615 | 101710 | 10 |
| | R18 | RESISTOR, CC<br>22 Ω 5%, 1/4W | 01121 | CB2205 | 101706 | 2 |
| | R19 | Same as R18 | | | | |
| | U1 | INTEGRATED CIRCUIT, TTL SSI<br>Dual D Flip-Flop | 01295 | SN7474N | 025241 | 1 |
| | U2 | INTEGRATED CIRCUIT, TTL MSI<br>Presettable 8-Input Counter | 01295 | SN74LS197N | 103165 | 2 |
| | U3 | Same as U2 | | | | |
| | U4 | INTEGRATED CIRCUIT, TTL SSI<br>Dual 4-Input NOR Gate W/Strobe | 01295 | SN7425N | 045296 | 1 |
| | U5 | INTEGRATED CIRCUIT, TTL MSI<br>Sync Binary Up/Down Counter | 01295 | SN74LS193N | 103162 | 2 |
| | U6 | Same as U5 | | | | |

## REPLACEABLE PARTS LIST

TITLE A9, 10 kHz GENERATOR PC ASSEMBLY #05334201 (Cont'd)

| ITEM | REF | COMPONENT DESCRIPTION | MFR'S CODE | MANUFACTURER'S PART NUMBER | SD STOCK NUMBER | T/Q |
|---|---|---|---|---|---|---|
| | U7 | INTEGRATED CIRCUIT, ECL<br>Quad ECL/TTL Translator | 04713 | MC10125L | 045226 | 1 |
| | U8 | INTEGRATED CIRCUIT, ECL<br>Quad TTL/ECL Translator | 04713 | MC10124L | 045228 | 2 |
| | U9 | INTEGRATED CIRCUIT, ECL<br>Quad 2-Input NOR Gate | 04713 | MC10102P | 103025 | 4 |
| | U10 | INTEGRATED CIRCUIT, ECL<br>Dual 4-Input OR/NOR Gate | 04713 | MC10109P | 103026 | 1 |
| | U11 | Same as U9 | | | | |
| | U12 | INTEGRATED CIRCUIT, ECL<br>Dual D M-S Flip-Flop | 04713 | MC10131L | 045239 | 2 |
| | U13 | INTEGRATED CIRCUIT, ECL<br>Dual D M-S Flip-Flop | 04713 | MC10231L | 045227 | 3 |
| | U14 | Same as U13 | | | | |
| | U15 | Same as U12 | | | | |
| | U16 | Same as U9 | | | | |
| | U17 | INTEGRATED CIRCUIT, ECL SSI<br>Triple Line Receiver | 04713 | MC10216L | 045276 | 1 |
| | U18 | INTEGRATED CIRCUIT, ECL MSI<br>4-Bit Counter 150 MHz | 04713 | MC10178P | 103273 | 1 |
| | U19 | Same as U13 | | | | |
| | U20 | Same as U9 | | | | |
| | U21 | Same as U8 | | | | |
| | U22 thru U27 | INTEGRATED CIRCUIT<br>Resistor Module | 52542 | 055066 | 055066 | 7 |
| | U28 | INTEGRATED CIRCUIT<br>Resistor Module 4-5k | 52542 | 027867 | 027867 | 1 |
| | U29 | Same as U22 | | | | |
| | | EXTRACTOR | 51495 | 1743 | 100865 | 1 |
| | | EXTRACTOR, Hot Stamped A9 | 52542 | 03984209 | 03984209 | 1 |
| | | ROLL PIN | 73957 | 50-094-0250 | 100752 | 2 |
| | | JUMPER, Molded | 50210 | L-2007-1 | 102879 | 2 |
| | | BOARD, PC | 52542 | 053342 | 053342 | 1 |

# REPLACEABLE PARTS LIST

TITLE A10, N COMPUTER PC ASSEMBLY #05736401 Rev D (Figure 7-14 & 7-15)

| ITEM | REF | COMPONENT DESCRIPTION | MFR'S CODE | MANUFACTURER'S PART NUMBER | SD STOCK NUMBER | T/Q |
|---|---|---|---|---|---|---|
| | C1 | CAPACITOR, Tant<br>4.7 µF 10%, 25V | 31433 | K4R7W25K | 102609 | 3 |
| | C2 | CAPACITOR, Tant<br>15 µF 10%, 20V | 56289 | 150D156X9020B2 | 100211 | 1 |
| | C3 | CAPACITOR, Ceramic<br>1000 pF 10%, 100V | 72982 | 8121-100W5R102K | 102620 | 4 |
| | C4 | CAPACITOR, Ceramic<br>.1 µF 20%, 50V | 56289 | 5C023104X0500C5 | 100178 | 2 |
| | C5 | Same as C4 | | | | |
| | C6 | Same as C1 | | | | |
| | C7 thru C9 | CAPACITOR, Ceramic<br>.05 µF +80-20%, 10V | 71590 | UK10-503 | 100122 | 4 |
| | C10 | Same as C1 | | | | |
| | C11 | Same as C7 | | | | |
| | C12 thru C14 | Same as C3 | | | | |
| | CR1 thru CR3 | DIODE, Signal 50V | 03508 | 1N4151 | 100385 | 3 |
| | Q1 | TRANSISTOR, SINPN 15V | 07263 | PN3646 | 101369 | 2 |
| | Q2 thru Q5 | TRANSISTOR, SIPNP 12V | 07263 | PN3640 | 101357 | 4 |
| | Q6 | Same as Q1 | | | | |
| | R1 | RESISTOR, CC<br>1 k 5%, 1/4W | 01121 | CB1025 | 101569 | 1 |
| | R2 | RESISTOR, CC<br>1 k 5%, 1/8W | 01121 | BB1025 | 101711 | 4 |
| | R3 | RESISTOR, CC<br>12 k 5%, 1/8W | 01121 | BB1235 | 101975 | 1 |
| | R4 | RESISTOR, CC<br>5.6 k 5%, 1/8W | 01121 | BB5625 | 101715 | 1 |
| | R5 | RESISTOR, CC<br>10 k 5%, 1/8W | 01121 | BB1035 | 101697 | 5 |
| | R6 | RESISTOR, CC<br>22 k 5%, 1/8W | 01121 | BB2235 | 101797 | 3 |
| | R7 | RESISTOR, CC<br>560 Ω 5%, 1/4W | 01121 | CB5615 | 101583 | 1 |

## REPLACEABLE PARTS LIST

TITLE A10, N COMPUTER PC ASSEMBLY #05736401 (Cont'd)

| ITEM | REF | COMPONENT DESCRIPTION | MFR'S CODE | MANUFACTURER'S PART NUMBER | SD STOCK NUMBER | T/Q |
|---|---|---|---|---|---|---|
| | R8 | RESISTOR, CC<br>100 Ω 5%, 1/8W | 01121 | BB1015 | 101701 | 1 |
| | R9 | Same as R2 | | | | |
| | R10<br>thru<br>R12 | RESISTOR, CC<br>2.2 k 5%, 1/8W | 01121 | BB2225 | 101719 | 4 |
| | R13 | RESISTOR, CC<br>4.7 k 5%, 1/8W | 01121 | BB4725 | 101792 | 4 |
| | R14 | Same as R2 | | | | |
| | R15 | RESISTOR, CC<br>560 Ω 5%, 1/8W | 01121 | BB5615 | 101710 | 7 |
| | R16 | Same as R15 | | | | |
| | R17 | Same as R2 | | | | |
| | R18 | Same as R6 | | | | |
| | R19 | RESISTOR, CC<br>33 k 5%, 1/8W | 01121 | BB3335 | 101693 | 1 |
| | R20 | Same as R5 | | | | |
| | R21 | Same as R13 | | | | |
| | R22 | Same as R13 | | | | |
| | R23 | Same as R10 | | | | |
| | R24<br>thru<br>R26 | Same as R15 | | | | |
| | R27 | Same as R6 | | | | |
| | R28 | RESISTOR, CC<br>47 k 5%, 1/8W | 01121 | BB4735 | 101694 | 1 |
| | R29 | Same as R13 | | | | |
| | R30 | RESISTOR, CC<br>470 k 5%, 1/8W | 01121 | BB4745 | 101955 | 1 |
| | R31 | RESISTOR, CC<br>15 k 5%, 1/8W | 01121 | BB1535 | 101698 | 1 |
| | R32<br>thru<br>R34 | Same as R5 | | | | |
| | R35 | Same as R15 | | | | |
| | R36 | Same as R15 | | | | |
| | U1<br>thru<br>U3 | INTEGRATED CIRCUIT, TTL SSI<br>Dual D Flip-Flip | 01295 | SN7474N | 025241 | 6 |

## REPLACEABLE PARTS LIST

TITLE A10, N COMPUTER PC ASSEMBLY #05736401 (Cont'd)

| ITEM | REF | COMPONENT DESCRIPTION | MFR'S CODE | MANUFACTURER'S PART NUMBER | SD STOCK NUMBER | T/Q |
|---|---|---|---|---|---|---|
| | U4 | INTEGRATED CIRCUIT, CMOS<br>12-Bit Binary Counter | 04713 | MC14040BCP | 117143 | 1 |
| | U5 | INTEGRATED CIRCUIT, TTL SSI<br>Dual One Shot Multi Vibrator | 01295 | SN74123N | 045209 | 2 |
| | U6 | Same as U1 | | | | |
| | U7 | INTEGRATED CIRCUIT, TTL MSI<br>Presettable Binary Counter | 01295 | SN74LS197N | 103165 | 2 |
| | U8 | Same as U1 | | | | |
| | U9 | INTEGRATED CIRCUIT, CMOS<br>Programmable Binary Down Counter | 04713 | MC14526BCP | 117144 | 2 |
| | U10 | INTEGRATED CIRCUIT, TTL SSI<br>Quad 2-Input NAND Gate | 01295 | SN7400N | 019705 | 2 |
| | U11 | Same as U1 | | | | |
| | U12 | INTEGRATED CIRCUIT, TTL MSI<br>Presettable BCD Counter | 01295 | SN74LS196N | 103164 | 2 |
| | U13 | Same as U10 | | | | |
| | U14 | Same as U9 | | | | |
| | U15 | INTEGRATED CIRCUIT, TTL SSI<br>Triple 3-Input AND Gate | 04713 | MC3006P | 045219 | 1 |
| | U16 | INTEGRATED CIRCUIT, TTL SSI<br>Quad 2-Input AND Gate | 01295 | SN7408N | 103093 | 2 |
| | U17 | Same as U12 | | | | |
| | U18 | Same as U7 | | | | |
| | U19 | INTEGRATED CIRCUIT, LIN MSC<br>Differential Voltage Comparator | 01295 | SN72311P | 103943 | 1 |
| | U21 | INTEGRATED CIRCUIT<br>W/Heatsink Assembly | 52542 | 067940 | 067940 | 2 |
| | U22 | INTEGRATED CIRCUIT, ECL<br>Dual E-Input OR/NOR Gate | 04713 | MC10109L | 103026 | 1 |
| | U23 | INTEGRATED CIRCUIT, ECL<br>Quad ECL/TTL Translator | 04713 | MC10125L | 045226 | 1 |
| | U24 | Same as U16 | | | | |
| | U25 | Same as U21 | | | | |
| | U26 | INTEGRATED CIRCUIT, ECL SSI<br>Triple Line Receiver | 04713 | MC10216L | 045276 | 1 |
| | U27 | INTEGRATED CIRCUIT, ECL<br>Dual D M-S Flip-Flop | 04713 | MC10131L | 045239 | 1 |
| | U28 | INTEGRATED CIRCUIT, ECL<br>Quad ECL/TTL Translator | 04713 | MC10124L | 045228 | 1 |

## REPLACEABLE PARTS LIST

TITLE A10, N COMPUTER PC ASSEMBLY #05736401 (Cont'd)

| ITEM | REF | COMPONENT DESCRIPTION | MFR'S CODE | MANUFACTURER'S PART NUMBER | SD STOCK NUMBER | T/Q |
|---|---|---|---|---|---|---|
| | U29 | INTEGRATED CIRCUIT<br>Resistor Module 4 x 560Ω | 52542 | 055066 | 055066 | 2 |
| | U30 | Same as U29 | | | | |
| | U31 | INTEGRATED CIRCUIT<br>Resistor Module 4 x 5k | 52542 | 027867 | 027867 | 1 |
| | | HEATSINK | 13103 | 6011B | 103224 | 2 |
| | | EXTRACTOR, Hot Stamped A10 | 52542 | 03984210 | 03984210 | 1 |
| | | EXTRACTOR | 51495 | 1743 | 100865 | 1 |
| | | ROLL PIN | 73957 | 50-049-0250 | 100752 | 2 |
| | | BOARD, PC | 52542 | 057364 | 057364 | 1 |

## REPLACEABLE PARTS LIST

| TITLE | A11, FUNCTION PC ASSEMBLY #05338601 Rev F (Figure 7-16 & 7-17) | | | | | |
|---|---|---|---|---|---|---|
| ITEM | REF | COMPONENT DESCRIPTION | MFR'S CODE | MANUFACTURER'S PART NUMBER | SD STOCK NUMBER | T/Q |
| | C1 | CAPACITOR, Ceramic .01 μF +80-20%, 100V | 91418 | TA110 | 117570 | 1 |
| | C2 | CAPACITOR, Ceramic .05 μF +80-20%, 10V | 71590 | UK10-503 | 100122 | 7 |
| | C3 | CAPACITOR, Tant 15 μF 10%, 20V | 56289 | 150D156X9020B2 | 100211 | 1 |
| | C4 | CAPACITOR, Tant 4.7 μF 10%, 25V | 31433 | K4R7W25K | 102609 | 1 |
| | C5 | CAPACITOR, Tant 8.2 μF 10%, 15V | 31433 | K8R2W15K | 102605 | 1 |
| | C6 | CAPACITOR, Ceramic .1 μF +80-20%, 10V | 71590 | UK10-104 | 100120 | 2 |
| | C7 | CAPACITOR, Ceramic .001 μF 20%, 50V | 71590 | CW15C102M | 100251 | 2 |
| | C8 | Same as C7 | | | | |
| | C9 | CAPACITOR, DM 470 pF 5%, 300V | 72136 | DM15FC471JO | 100221 | 1 |
| | C10 | Same as C6 | | | | |
| | C11 | CAPACITOR, Tant 39 μF 10%, 10V | 56289 | 150D396X9010B2 | 100183 | 1 |
| | C12 | CAPACITOR, Tant 4.7 μF 10%, 35V | 56289 | 150D475X9035B2 | 100071 | 1 |
| | C13 thru C18 | Same as C2 | | | | |
| | CR1 thru CR4 | DIODE, Signal 50V | 03508 | 1N4151 | 100385 | 4 |
| | Q1 | TRANSISTOR, SINPN 15V | 07263 | PN3646 | 101369 | 2 |
| | Q2 | Same as Q1 | | | | |
| | Q3 | TRANSISTOR, SIPNP 30V | 04713 | MPS-A65 | 117349 | 1 |
| | R1 | RESISTOR, CC 4.7 k 5%, 1/4W | 01121 | CB4725 | 101598 | 2 |
| | R2 | RESISTOR, CC 22 k 5%, 1/4W | 01121 | CB2235 | 101572 | 7 |
| | R3 | RESISTOR, CC 10 k 5%, 1/4W | 01121 | CB1035 | 101570 | 5 |
| | R4 | RESISTOR, CC 5.1 M 5%, 1/4W | 01121 | CB5155 | 101692 | 2 |
| | R5 | Same as R3 | | | | |

## REPLACEABLE PARTS LIST

TITLE A11, FUNCTION PC ASSEMBLY #05338601 (Cont'd)

| ITEM | REF | COMPONENT DESCRIPTION | MFR'S CODE | MANUFACTURER'S PART NUMBER | SD STOCK NUMBER | T/Q |
|---|---|---|---|---|---|---|
| | R6 | RESISTOR, CC<br>1 k 5%, 1/8W | 01121 | BB1025 | 101711 | 2 |
| | R7 | RESISTOR, CC<br>10 Ω 5%, 1/8W | 01121 | BB1005 | 101834 | 1 |
| | R8 | Same as R3 | | | | |
| | R9 | RESISTOR, CC<br>1 k 5%, 1/4W | 01121 | CB1025 | 101569 | 6 |
| | R10 | Same as R1 | | | | |
| | R11 | Same as R3 | | | | |
| | R12 | RESISTOR, CC<br>470 Ω 5%, 1/4W | 01121 | CB4715 | 101625 | 3 |
| | R13 | Same as R12 | | | | |
| | R14 | Same as R3 | | | | |
| | R15 | RESISTOR, CC<br>470 Ω 5%, 1/8W | 01121 | BB4715 | 101709 | 1 |
| | R16 | RESISTOR, CC<br>560 Ω 5%, 1/4W | 01121 | CB5615 | 101583 | 1 |
| | R17 | RESISTOR, CC<br>22 Ω 5%, 1/4W | 01121 | CB2205 | 101566 | 1 |
| | R18 | Same as R2 | | | | |
| | R19 | Same as R2 | | | | |
| | R20 | Same as R9 | | | | |
| | R21 | Same as R2 | | | | |
| | R22 thru R25 | Same as R9 | | | | |
| | R26 thru R28 | Same as R2 | | | | |
| | R29 | Same as R12 | | | | |
| | R30 | Same as R6 | | | | |
| | U1 | INTEGRATED CIRCUIT, TTL SSI<br>Triple 3-Input AND Gate | 04713 | MC3006P | 045219 | 2 |
| | U2 | INTEGRATED CIRCUIT, TTL SSI<br>Dual One-Shot Multi Vibrator | 01295 | SN74123N | 045209 | 3 |
| | U3 | INTEGRATED CIRCUIT, TTL SSI<br>Hex Inverter Open Collector 15V | 01295 | SN7416N | 045230 | 2 |
| | U4 | INTEGRATED CIRCUIT, TTL SSI<br>Quad 2-Input NOR Gate | 04713 | MC3002P | 025739 | 1 |

## REPLACEABLE PARTS LIST

TITLE **A11, FUNCTION PC ASSEMBLY #05338601 (Cont'd)**

| ITEM | REF | COMPONENT DESCRIPTION | MFR'S CODE | MANUFACTURER'S PART NUMBER | SD STOCK NUMBER | T/Q |
|---|---|---|---|---|---|---|
| | U5 | INTEGRATED CIRCUIT, TTL SSI<br>Hex Inverter | 01295 | SN7404N | 025779 | 1 |
| | U6 | INTEGRATED CIRCUIT, TTL SSI<br>Dual D Flip-Flop | 01295 | SN7474N | 025241 | 1 |
| | U7 | INTEGRATED CIRCUIT, TTL MSI<br>Presettable Binary Counter | 01295 | SN74LS197N | 103165 | 1 |
| | U8 | INTEGRATED CIRCUIT, TTL SSI<br>Quad 2-Input OR Gate | 01295 | SN7432N | 045257 | 3 |
| | U9 | Same as U8 | | | | |
| | U10 | INTEGRATED CIRCUIT, TTL SSI<br>Quad 2-Input NAND Gate | 01295 | SN7400N | 019705 | 2 |
| | U11 | Same as U3 | | | | |
| | U12 | Same as U2 | | | | |
| | U13 | Same as U8 | | | | |
| | U14 | INTEGRATED CIRCUIT, LIN MSC<br>Wide Range Timer | 18324 | NE555V | 045208 | 2 |
| | U15 | INTEGRATED CIRCUIT, TTL SSI<br>Schmitt Inverter | 01295 | SN74LS14 | 117083 | 1 |
| | U16 | INTEGRATED CIRCUIT, TTL SSI<br>Quad 2-Input AND Gate | 01295 | SN7408N | 103093 | 2 |
| | U17 | Same as U16 | | | | |
| | U18 | Same as U10 | | | | |
| | U19 | Same as U1 | | | | |
| | U20 | INTEGRATED CIRCUIT, TTL SSI<br>Hex Buffer Open Collector 15V | 01295 | SN7417N | 106629 | 1 |
| | U21 | Same as U14 | | | | |
| | U22 | Same as U2 | | | | |
| | | EXTRACTOR | 51495 | 1743 | 100865 | 1 |
| | | EXTRACTOR, Hot Stamped A11 | 52542 | 03984211 | 03984211 | 1 |
| | | ROLL PIN | 73957 | 50-094-0250 | 100752 | 2 |
| | | BOARD, PC | 52542 | 053386 | 053386 | 1 |

## REPLACEABLE PARTS LIST

TITLE **A12, 20 MHz AMP PC ASSEMBLY #05341201 Rev F (Figure 7-18 & 7-19)**

| ITEM | REF | COMPONENT DESCRIPTION | MFR'S CODE | MANUFACTURER'S PART NUMBER | SD STOCK NUMBER | T/Q |
|---|---|---|---|---|---|---|
| | C1 | CAPACITOR, Ceramic<br>.05 μF +80-20%, 600V | 91418 | TYPE B | 100074 | 1 |
| | C2 | CAPACITOR, DM<br>100 pF 5%, 500V | 72136 | DM15FD101JO | 100173 | 1 |
| | C3 | CAPACITOR, Ceramic<br>.001 μF 20%, 50V | 71590 | CW15C102M | 100251 | 1 |
| | C4 | CAPACITOR, Tant<br>4.7 μF 10%, 25V | 31433 | K4R7W25K | 102609 | 3 |
| | C5 | CAPACITOR, Tant<br>22 μF 20%, 20V | 31433 | T140B225M025AS | 100067 | 1 |
| | C6<br>thru<br>C8 | CAPACITOR, Ceramic<br>1 μF 20%, 25V | 56289 | 4C02105X0250B3 | 100176 | 3 |
| | C9 | CAPACITOR, Tant<br>8.2 μF 10%, 15V | 31433 | K8R2W15K | 102605 | 3 |
| | C10 | CAPACITOR, Ceramic<br>.1 μF +80-20%, 10V | 71590 | UK10-104 | 100120 | 3 |
| | C11 | CAPACITOR, DM<br>10 pF 5%, 500V | 72136 | DM15CD100JO | 100253 | 2 |
| | C12 | Same as C10 | | | | |
| | C13 | Same as C11 | | | | |
| | C14 | Same as C10 | | | | |
| | C15 | CAPACITOR, Ceramic DP<br>.01 μF 20%, 100V | 04222 | 3429100C103M | 117570 | 3 |
| | C16 | Same as C15 | | | | |
| | C17 | Same as C4 | | | | |
| | C18 | Same as C15 | | | | |
| | C19 | Same as C9 | | | | |
| | C20 | CAPACITOR, Ceramic<br>.05 μF +80-20%, 10V | 71590 | UK10-503 | 100122 | 2 |
| | C21 | Same as C9 | | | | |
| | C22 | Same as C4 | | | | |
| | C23 | Same as C20 | | | | |
| | CR1<br>thru<br>CR5 | DIODE, Signal 50V | 03508 | 1N4151 | 100385 | 5 |
| | J1 | RECEPTICAL, RF Rectangular | 98291 | 51-053-0000 | 103173 | 1 |
| | Q1 | TRANSISTOR, JFET N-Channel | 01295 | 2N5248 | 101375 | 2 |
| | Q2 | Same as Q1 | | | | |

## REPLACEABLE PARTS LIST

TITLE A12, 20 MHz AMP PC ASSEMBLY #05341201 (Cont'd)

| ITEM | REF | COMPONENT DESCRIPTION | MFR'S CODE | MANUFACTURER'S PART NUMBER | SD STOCK NUMBER | T/Q |
|---|---|---|---|---|---|---|
| | Q3 | TRANSISTOR, SINPN 12V | 02735 | 2N5179 | 101388 | 1 |
| | Q4 | TRANSISTOR, SINPN 40V | 07263 | 2N3904 | 101377 | 2 |
| | Q5 | Same as Q4 | | | | |
| | Q6 | TRANSISTOR, SIPNP 12V | 07263 | PN3640-18 | 101357 | 1 |
| | Q7 | TRANSISTOR, SINPN 15V | 07263 | PN3646 | 101369 | 1 |
| | R1 | RESISTOR, CC<br>10 k 5%, 1/4W | 01121 | CB1025 | 101570 | 1 |
| | R2 | RESISTOR, CC<br>1 M 5%, 1/4W | 01121 | CB1055 | 101605 | 3 |
| | R3 | RESISTOR, CC<br>6.8 k 5%, 1/4W | 01121 | CB6825 | 101544 | 1 |
| | R4 | Same as R2 | | | | |
| | R5 | Same as R2 | | | | |
| | R6 | RESISTOR, CC<br>5.6 k 5%, 1/4W | 01121 | CB5625 | 101584 | 2 |
| | R7 | RESISTOR, CC<br>470 Ω 5%, 1/4W | 01121 | CB4715 | 101625 | 1 |
| | R8 | RESISTOR, CC<br>270 Ω 5%, 1/4W | 01121 | CB2715 | 101542 | 1 |
| | R9 | RESISTOR, CC<br>220 Ω 5%, 1/4W | 01121 | CB2215 | 101566 | 1 |
| | R10 | RESISTOR, CC<br>47 Ω 5%, 1/4W | 01121 | CB4705 | 101560 | 1 |
| | R11 | RESISTOR, CC<br>2.2 k 5%, 1/4W | 01121 | CB2225 | 101562 | 3 |
| | R12 | Same as R11 | | | | |
| | R13 | RESISTOR, Variable<br>1 k 20%, 1/2W | 80294 | 3339W-1-102 | 102129 | 1 |
| | R14 | RESISTOR, CC<br>1 k 5%, 1/4W | 01121 | CB1025 | 101569 | 8 |
| | R15 | RESISTOR, CC<br>150 Ω 5%, 1/4W | 01121 | CB1515 | 101615 | 1 |
| | R16 | RESISTOR, CC<br>330 Ω 5%, 1/4W | 01121 | CB3315 | 101536 | 2 |
| | R17 | RESISTOR, CC<br>4.7 k 5%, 1/4W | 01121 | CB4725 | 101598 | 2 |
| | R18 | RESISTOR, CC<br>3.3 k 5%, 1/4W | 01121 | CB3325 | 101559 | 1 |
| | R19 | RESISTOR, CC<br>180 Ω 5%, 1/4W | 01121 | CB1815 | 101668 | 1 |

## REPLACEABLE PARTS LIST

TITLE A12, 20 MHz AMP PC ASSEMBLY #05341201 (Cont'd)

| ITEM | REF | COMPONENT DESCRIPTION | MFR'S CODE | MANUFACTURER'S PART NUMBER | SD STOCK NUMBER | T/Q |
|---|---|---|---|---|---|---|
| | R20 | RESISTOR, CC<br>3.9 k 5%, 1/4W | 01121 | CB3925 | 101601 | 1 |
| | R21 | RESISTOR, CC<br>5.1 k 5%, 1/4W | 01121 | CB5125 | 101541 | 1 |
| | R22 | Same as R11 | | | | |
| | R23 | Same as R16 | | | | |
| | R24 | RESISTOR, CC<br>82 Ω 5%, 1/8W | 01121 | BB8205 | 101800 | 1 |
| | R25 thru R31 | Same as R14 | | | | |
| | R32 | Same as R17 | | | | |
| | U1 | INTEGRATED CIRCUIT,<br>Linear Amp 50 MHz | 04713 | MC1590G | 025788 | 1 |
| | U2 | INTEGRATED CIRCUIT, TTL SSI<br>Dual 4-Input NAND Gate | 01295 | SN7420N | 025713 | 3 |
| | U3 | Same as U2 | | | | |
| | U4 | INTEGRATED CIRCUIT, TTL<br>Programmed ROM | 52542 | 055123 | 055123 | 1 |
| | U5 | INTEGRATED CIRCUIT, DTL<br>Quad 2-Input AND Gate | 04713 | MC1806P | 025733 | 1 |
| | U6 | INTEGRATED CIRCUIT, DTL<br>Quad 2-Input NAND Gate | 01295 | SN15846N | 019716 | 1 |
| | U7 | INTEGRATED CIRCUIT, TTL SSI<br>Quad 2-Input AND Gate | 01295 | SN7408N | 103093 | 1 |
| | U8 | INTEGRATED CIRCUIT, TTL SSI<br>Quad 2-Input OR Gate | 01295 | SN7432N | 045257 | 2 |
| | U9 | INTEGRATED CIRCUIT, TTL SSI<br>Quad 2-Input Exclusive OR Gate | 04713 | MC3021P | 025789 | 2 |
| | U10 | Same as U2 | | | | |
| | U11 | INTEGRATED CIRCUIT, TTL SSI<br>Quad 2-Input NAND Gate | 01295 | SN7400N | 019705 | 1 |
| | U12 | Same as U9 | | | | |
| | U13 | Same as U8 | | | | |
| | U14 | INTEGRATED CIRCUIT, TTL SSI<br>Hex Inverter Open Collector 15V | 01295 | SN7416N | 045230 | 1 |
| | U15 thru U17 | INTEGRATED CIRCUIT<br>Resistor Module 4-12k | 52542 | 045008 | 045008 | 3 |

## REPLACEABLE PARTS LIST

TITLE A12, 20 MHz AMP PC ASSEMBLY #05341201 (Cont'd)

| ITEM | REF | COMPONENT DESCRIPTION | MFR'S CODE | MANUFACTURER'S PART NUMBER | SD STOCK NUMBER | T/Q |
|---|---|---|---|---|---|---|
| | | CIRCUIT, Shield 20 MHz Amp | 52542 | 055031 | 055031 | 1 |
| | | SWAGE, Spacer 4-40 x 1/2 | 06540 | 9537B-B-0440-3A | 100024 | 2 |
| | | WASHER, Split-Lock #4 | 96906 | MS35338-135 | 100711 | 4 |
| | | SCREW, PHMS 4-40 x 1/4 | 96906 | MS51957-13 | 10062604 | 2 |
| | | SCREW, PHMS 4-40 x 1/2 | 96906 | MS51957-17 | 10062608 | 2 |
| | | EXTRACTOR | 51495 | 1743 | 100865 | 2 |
| | | EXTRACTOR, Hot Stamped A12 | 52542 | 03984212 | 03984212 | 1 |
| | | ROLL PIN | 73957 | 50-094-0250 | 100752 | 2 |
| | | JUMPER, Molded | 50210 | L-2007-1 | 102879 | 1 |
| | | BOARD, PC | 52542 | 053412 | 053412 | 1 |

## REPLACEABLE PARTS LIST

TITLE A13, DISPLAY PC ASSEMBLY #05326301 Rev B (Figure 7-20 & 7-21)

| ITEM | REF | COMPONENT DESCRIPTION | MFR'S CODE | MANUFACTURER'S PART NUMBER | SD STOCK NUMBER | T/Q |
|---|---|---|---|---|---|---|
| | DS1 thru DS6 | LAMP, Incandescant 18V | 71744 | CM7220 | 101141 | 6 |
| | DS7 thru DS17 | LED, 7-Segment | 50522 | MAN4610 | 10317201 | 11 |
| | R1 thru R87 | RESISTOR, CC 270 Ω 5%, 1/8W | 01121 | BB2715 | 101703 | 87 |
| | U1 thru U11 | INTEGRATED CIRCUIT, TTL MSI 4 to 7 Line Decoder/Driver | 01295 | SN74LS247N | 103166 | 11 |
| | U12 | INTEGRATED CIRCUIT, TTL MSI 4 to 10 Line Decoder/Driver | 01295 | SN74145N | 025754 | 1 |
| | XDS7 thru XDS17 | SOCKET, 14-Pin | 73803 | C83-14-02 | 117040 | 11 |
| | | BLOCK, Annunciator | 52542 | 053405 | 053405 | 1 |
| | | FILM, Annunciator Legend | 52542 | 053448 | 053448 | 1 |
| | | SPACER, Swage | 71279 | 1247-11 | 100539 | 2 |
| | | SCREW, PHMS 2-56 x 5/16 | 96906 | MS51957-4 | 10062605 | 2 |
| | | BOARD, PC | 52542 | 053263 | 053263 | 1 |

## REPLACEABLE PARTS LIST

| TITLE | A14, N IF ACTO MODULE ASSEMBLY #055369 Rev $B_4$ (Figure 7-22) | | | | | |
|---|---|---|---|---|---|---|
| **ITEM** | **REF** | **COMPONENT DESCRIPTION** | **MFR'S CODE** | **MANUFACTURER'S PART NUMBER** | **SD STOCK NUMBER** | **T/Q** |
| 1 | A14 | ASSEMBLY, N IF PC | 52542 | 05324601 | 05324601 | 1 |
| 2 | | CASTING, Mod. Comp Side | 52542 | 055293 | 055293 | 1 |
| 3 | | CASTING, Mod. Circuit Side | 52542 | 055292 | 055292 | 1 |
| 4 | | RAIL, ACTO Mod. Mounting | 52542 | 053961 | 053961 | 1 |
| 5 | J1 | RECEPTICAL, RF | 98291 | 51-043-3200 | 101251 | 1 |
| 6 | | STUD, 1/4 turn | 71286 | 551-8 | 103257 | 2 |
| 7 | | RETAINER | 71286 | 553-1 | 100770 | 2 |
| 8 | | BRAID, RFI | 07700 | 20-41210 | 103274 | A/R |
| 9 | | SCREW, PHMS 4-40 x 9/16 | 96906 | MS51957-120 | 100835 | 3 |
| 10 | | SCREW, PHMS 4-40 x 1/4 | 96906 | MS51957-13 | 10062604 | 4 |
| 11 | | WASHER, Split-Lock #4 | 96906 | MS35338-135 | 100711 | 10 |
| 12 | | WASHER, Flat #4 | 96906 | MS15795-803 | 100703 | 4 |
| 13 | | SCREW, PHMS 4-40 x 5/8 | 96906 | MS51957-18 | 10062610 | 3 |

## REPLACEABLE PARTS LIST

TITLE A14, N IF PC ASSEMBLY #05324601 Rev J (Figure 7-23 & 7-24)

| ITEM | REF | COMPONENT DESCRIPTION | MFR'S CODE | MANUFACTURER'S PART NUMBER | SD STOCK NUMBER | T/Q |
|---|---|---|---|---|---|---|
| | C1 | CAPACITOR, Ceramic<br>1000 pF 20%, 50V | 71590 | CW15C102M | 100251 | 15 |
| | C2 | CAPACITOR, Ceramic<br>6.8 pF 5%, 1000V | 56289 | 10TCC-V68 | 106490 | 2 |
| | C3 | CAPACITOR, Variable<br>5.5 - 18 pF | 72982 | 538-001A5.5-18 | 100136 | 7 |
| | C4 | Same as C3 | | | | |
| | C5 | Same as C1 | | | | |
| | C6 | CAPACITOR, Ceramic<br>1 µF 20%, 25V | 56289 | 5CZ5U105X0050C5 | 100176 | 7 |
| | C7 | Same as C1 | | | | |
| | C8 | CAPACITOR, Ceramic<br>.1 µF 20%, 50V | 56289 | 5C023104X0500C5 | 100178 | 10 |
| | C9 | Same as C8 | | | | |
| | C10 | Same as C3 | | | | |
| | C11 | Same as C2 | | | | |
| | C12 | Same as C3 | | | | |
| | C13 | Same as C1 | | | | |
| | C14 | Same as C6 | | | | |
| | C15 | Same as C1 | | | | |
| | C16 | Same as C8 | | | | |
| | C17 | Same as C8 | | | | |
| | C18 | Same as C3 | | | | |
| | C19 | Same as C1 | | | | |
| | C20 | Same as C3 | | | | |
| | C21 | Same as C1 | | | | |
| | C22 | Same as C6 | | | | |
| | C23 | Same as C1 | | | | |
| | C24 | Same as C8 | | | | |
| | C25 | Same as C6 | | | | |
| | C26 | Same as C6 | | | | |
| | C27 | Same as C3 | | | | |
| | C28 thru C30 | Same as C1 | | | | |
| | C31 | Same as C6 | | | | |
| | C32 | Same as C6 | | | | |

## REPLACEABLE PARTS LIST

**TITLE** **A14, N IF PC ASSEMBLY #05324601 (Cont'd)**

| ITEM | REF | COMPONENT DESCRIPTION | MFR'S CODE | MANUFACTURER'S PART NUMBER | SD STOCK NUMBER | T/Q |
|---|---|---|---|---|---|---|
| | C33 | Same as C1 | | | | |
| | C34 | Same as C1 | | | | |
| | C35 | CAPACITOR, Ceramic .05 µF +80-20%, 10V | 71590 | UK10-503 | 100122 | 6 |
| | C36 | CAPACITOR, DM 180 pF 5%, 500V | 72136 | DM15FD181JO | 100237 | 1 |
| | C37 | Same as C35 | | | | |
| | C38 | Same as C35 | | | | |
| | C39 | Same as C6 | | | | |
| | C40 | Same as C8 | | | | |
| | C41 | CAPACITOR, Ceramic DP .01 µF 20%, 100V | 04222 | 3429100C103M | 117570 | 2 |
| | C42 | Same as C8 | | | | |
| | C43 | Same as C41 | | | | |
| | C44 | CAPACITOR, Tant 39 µF 10%, 10V | 56289 | 150D396X9010B2 | 100183 | 1 |
| | C45 thru C47 | Same as C35 | | | | |
| | C48 | Same as C8 | | | | |
| | C49 | Same as C8 | | | | |
| | C50 | Same as C1 | | | | |
| | C51 | Same as C1 | | | | |
| | C52 | CAPACITOR, DM 560 pF 5%, 300V | 72136 | DM15FC561JO | 100222 | 1 |
| | CR1 | DIODE, Signal 70V | 28480 | 5082-2800 | 100442 | 1 |
| | L1 | INDUCTOR, Fixed 10 µH 10% | 72259 | WEE-WEE-10 | 101317 | 1 |
| | L2 | INDUCTOR, Fixed 100 µH 5% | 72259 | WEE-100 | 101306 | 5 |
| | L3 | INDUCTOR, Fixed 2.2 µH 5% | 32159 | SSD-2.2 5% | 10130901 | 1 |
| | L4 | INDUCTOR, Fixed 1.8 µH 5% | 32159 | SSD-1.8 5% | 10318701 | 1 |
| | L5 | Same as L2 | | | | |
| | L6 | INDUCTOR, Fixed 1.5 µH 5% | 32159 | SSD-1.5 5% | 10132601 | 5 |
| | L7 | Same as L6 | | | | |
| | L8 | Same as L2 | | | | |
| | L9 | Same as L6 | | | | |
| | L10 | Same as L6 | | | | |
| | L11 | Same as L2 | | | | |
| | L12 | Same as L6 | | | | |

## REPLACEABLE PARTS LIST

TITLE **A14, N IF PC ASSEMBLY #05324601 (Cont'd)**

| ITEM | REF | COMPONENT DESCRIPTION | MFR'S CODE | MANUFACTURER'S PART NUMBER | SD STOCK NUMBER | T/Q |
|---|---|---|---|---|---|---|
| | L13 | Same as L2 | | | | |
| | L14 | INDUCTOR, Fixed 2.7 μH 10% | 72259 | WEE-2.7 | 101299 | 1 |
| | L15 | INDUCTOR, Fixed 270 μH 10% | 72259 | WEE-WEE-270 | 117094 | 1 |
| | L16 | INDUCTOR, Bead Shielding | 52542 | 112420 | 112420 | 2 |
| | L17 | Same as L16 | | | | |
| | Q1 thru Q3 | TRANSISTOR, MOSFET Dual Gate | 04713 | MFE121 | 101413 | 3 |
| | Q4 thru Q6 | TRANSISTOR, SIPNP 40V | 04713 | 2N3906 | 101378 | 3 |
| | R1 | RESISTOR, CC 82 Ω 5%, 1/4W | 01121 | CB8205 | 101629 | 1 |
| | R2 | RESISTOR, CC 270 k 5%, 1/4W | 01121 | CB2745 | 101769 | 4 |
| | R3 | RESISTOR, CC 3.9 k 5%, 1/4W | 01121 | CB3925 | 101601 | 1 |
| | R4 | Same as R2 | | | | |
| | R5 | RESISTOR, CC 750 k 5%, 1/4W | 01121 | CB7545 | 101585 | 2 |
| | R6 | RESISTOR, CC 1.2 k 5%, 1/4W | 01121 | CB1225 | 101581 | 2 |
| | R7 | RESISTOR, CC 1.8 k 5%, 1/4W | 01121 | CB1825 | 101602 | 5 |
| | R8 | Same as R7 | | | | |
| | R9 | RESISTOR, CC 120 k 5%, 1/4W | 01121 | CB1245 | 101580 | 1 |
| | R10 | RESISTOR, CC 330 Ω 5%, 1/4W | 01121 | CB3315 | 101536 | 1 |
| | R11 | Same as R7 | | | | |
| | R12 | Same as R7 | | | | |
| | R13 | Same as R2 | | | | |
| | R14 | Same as R5 | | | | |
| | R15 | Same as R6 | | | | |
| | R16 | Same as R7 | | | | |
| | R17 | RESISTOR, CC 33 Ω 5%, 1/4W | 01121 | CB3305 | 101731 | 1 |
| | R18 | RESISTOR, CC 5.6 k 5%, 1/4W | 01121 | CB5625 | 101584 | 2 |

## REPLACEABLE PARTS LIST

TITLE A14, N IF PC ASSEMBLY #05324601 (Cont'd)

| ITEM | REF | COMPONENT DESCRIPTION | MFR'S CODE | MANUFACTURER'S PART NUMBER | SD STOCK NUMBER | T/Q |
|---|---|---|---|---|---|---|
| | R19 | RESISTOR, CC<br>220 Ω 5%, 1/4W | 01121 | CB2215 | 101566 | 1 |
| | R20 | RESISTOR, CC<br>51 Ω 5%, 1/4W | 01121 | CB5105 | 101672 | 2 |
| | R21 | RESISTOR, CC<br>2.7 k 5%, 1/4W | 01121 | CB2725 | 101599 | 1 |
| | R22 | RESISTOR, CC<br>2.2 k 5%, 1/4W | 01121 | CB2225 | 101562 | 2 |
| | R23 | Same as R22 | | | | |
| | R24 | RESISTOR, CC<br>47 Ω 5%, 1/4W | 01121 | CB4705 | 101560 | 1 |
| | R25 | Same as R20 | | | | |
| | R26 | Same as R18 | | | | |
| | R27 | RESISTOR, CC<br>1 k 5%, 1/4W | 01121 | CB1025 | 101569 | 5 |
| | R28 | RESISTOR, Variable<br>1 k 20%, 1/2W | 80294 | 3329H-1-102 | 101919 | 1 |
| | R29 | RESISTOR, CC<br>15 k 5%, 1/4W | 01121 | CB1535 | 101552 | 1 |
| | R30<br>thru<br>R32 | Same as R27 | | | | |
| | R33 | RESISTOR, CC<br>100 k 5%, 1/4W | 01121 | CB1045 | 101558 | 1 |
| | R34 | RESISTOR, CC<br>220 k 5%, 1/4W | 01121 | CB2245 | 101610 | 1 |
| | R35 | RESISTOR, Variable<br>500 Ω 20%, 1/2W | 80294 | 3339H-1-501 | 102163 | 1 |
| | R36 | Same as R27 | | | | |
| | R37 | Same as R2 | | | | |
| | R38 | RESISTOR, CC<br>4.7 k 5%, 1/4W | 01121 | CB4725 | 101598 | 1 |
| | R39 | RESISTOR, CC<br>1.5 k 5%, 1/4W | 01121 | CB1525 | 101577 | 1 |
| | U1 | INTEGRATED CIRCUIT<br>Linear Amp 50 MHz | 04713 | MC1590G | 025788 | 1 |
| | U2 | INTEGRATED CIRCUIT, LIN MSC<br>Bal Mod & Demod | 04713 | MC1495G | 103180 | 1 |
| | U3 | INTEGRATED CIRCUIT, TTL SSI<br>4 x 2-Input NAND Gate | 01295 | SN74132N | 045270 | 1 |
| | | BOARD, PC | 52542 | 053246 | 053246 | 1 |

# REPLACEABLE PARTS LIST

**TITLE** A15, SEARCH OSCILLATOR ACTO MODULE ASSEMBLY #055370 Rev $B_5$ (Figure 7-25)

| ITEM | REF | COMPONENT DESCRIPTION | MFR'S CODE | MANUFACTURER'S PART NUMBER | SD STOCK NUMBER | T/Q |
|---|---|---|---|---|---|---|
| 1 | A15 | ASSEMBLY, Search Oscillator PC | 52542 | 05322801 | 05322801 | 1 |
| 2 | | CASTING, Module Component Side | 52542 | 055293 | 055293 | 1 |
| 3 | | CASTING, Module Circuit Side | 52542 | 055295 | 055295 | 1 |
| 4 | | RAIL, ACTO Module Mtg. | 52542 | 053961 | 053961 | 1 |
| 5 | J1,J2 | RECEPTICAL, RF | 98291 | 51-043-4300 | 101251 | 2 |
| 6 | | STUD, 1/4 turn | 71286 | 551-8 | 103257 | 2 |
| 7 | | RETAINER | 71286 | 553-1 | 100770 | 2 |
| 9 | | SCREW, PHMS 4-40 x 9/16 | 96906 | MS51957-120 | 100835 | 3 |
| 10 | | SCREW, PHMS 4-40 x 1/4 | 96906 | MS51957-13 | 10062604 | 4 |
| 11 | | WASHER, Split-Lock #4 | 96906 | MS35338-135 | 100711 | 10 |
| 12 | | WASHER, Flat #4 | 96906 | MS15795-803 | 100703 | 4 |
| 13 | | SCREW, PHMS 4-40 x 5/8 | 96906 | MS51957-19 | 10062610 | 3 |

## REPLACEABLE PARTS LIST

TITLE A15, SEARCH OSCILLATOR PC ASSEMBLY #05322801 Rev M (Figure 7-26 & 7-27)

| ITEM | REF | COMPONENT DESCRIPTION | MFR'S CODE | MANUFACTURER'S PART NUMBER | SD STOCK NUMBER | T/Q |
|---|---|---|---|---|---|---|
| | C1 | CAPACITOR, Ceramic<br>.05 μF +80-20%, 10V | 71590 | UK10-503 | 100122 | 2 |
| | C2 | CAPACITOR, Ceramic<br>.01 μF 20%, 100V | 04222 | 3429100C103M | 117570 | 4 |
| | C3 | CAPACITOR, Ceramic<br>.001 μF 20%, 50V | 71590 | CW15C102M | 100251 | 1 |
| | C4 | CAPACITOR, Ceramic<br>.1 μF 20%, 50V | 56289 | 5C023104X0500C5 | 100178 | 26 |
| | C5 | Same as C4 | | | | |
| | C6 | Same as C2 | | | | |
| | C7 | Same as C4 | | | | |
| | C8 | Same as C2 | | | | |
| | C9 | Same as C4 | | | | |
| | C10 | Same as C4 | | | | |
| | C11 | CAPACITOR, Variable<br>15 - 60 pF | 72982 | 538-011F15-60 | 100234 | 1 |
| | C12 | CAPACITOR, DM<br>200 pF 5%, 500V | 72136 | DM15FD201JO | 102576 | 1 |
| | C13 | CAPACITOR, DM<br>2000 pF 5%, 500V | 72136 | DM19FD202JO | 100117 | 1 |
| | C14 | Same as C4 | | | | |
| | C15 | CAPACITOR, DM<br>33 pF 5%, 500V | 72136 | DM15ED330JO | 100175 | 3 |
| | C16 | CAPACITOR, Ceramic<br>.01 μF 10%, 50V | 32159 | G504BX103K | 100374 | 2 |
| | C17 | Same as C4 | | | | |
| | C18 | Same as C4 | | | | |
| | C19 | Same as C1 | | | | |
| | C20<br>thru<br>C25 | Same as C4 | | | | |
| | C26 | Same as C15 | | | | |
| | C27<br>thru<br>C32 | Same as C4 | | | | |
| | C33 | Same as C16 | | | | |
| | C34 | CAPACITOR, DM<br>22 pF 5%, 500V | 72136 | DM15ED220JO | 100068 | 1 |
| | C35 | Same as C4 | | | | |

## REPLACEABLE PARTS LIST

TITLE A15, SEARCH OSCILLATOR PC ASSEMBLY #05322801 (Cont'd)

| ITEM | REF | COMPONENT DESCRIPTION | MFR'S CODE | MANUFACTURER'S PART NUMBER | SD STOCK NUMBER | T/Q |
|---|---|---|---|---|---|---|
| | C36 | Same as C4 | | | | |
| | C37 | Same as C2 | | | | |
| | C38 | Same as C4 | | | | |
| | C39 | Same as C4 | | | | |
| | C40 | Same as C15 | | | | |
| | C41 | Same as C4 | | | | |
| | C42 | Same as C4 | | | | |
| | C43 | CAPACITOR, Tant 3.3 μF 10%, 15V | 56289 | 150D335X9015A2 | 100204 | 1 |
| | CR1 thru CR12 | DIODE, Signal 50V | 03508 | 1N4151 | 100385 | 12 |
| | Q1 | TRANSISTOR, SINPN | 04713 | MPS-A12 | 101396 | 1 |
| | Q2 | TRANSISTOR, SIPNP 40V | 04713 | 2N3906 | 101378 | 5 |
| | Q3 | TRANSISTOR, JFET N-Channel | 04713 | 2N5459 | 101384 | 1 |
| | Q4 | TRANSISTOR, SINPN 15V | 07263 | PN4275 | 102716 | 2 |
| | Q5 | Same as Q4 | | | | |
| | Q6 thru Q8 | Same as Q2 | | | | |
| | Q9 | TRANSISTOR, Selected | 52542 | 033392 | 033392 | 1 |
| | Q10 | TRANSISTOR, JFET N-Channel | 01295 | 2N4393 | 101417 | 2 |
| | Q11 | Same as Q2 | | | | |
| | Q12 | Same as Q10 | | | | |
| | Q13 | TRANSISTOR, SINPN 15V | 07263 | PN3646 | 101369 | 1 |
| | R1 | Not Used | | | | |
| | R2 | RESISTOR, CC 180 k 5%, 1/4W | 01121 | CB1845 | 101623 | 1 |
| | R3 | RESISTOR, Variable 1 k 20%, 1/2W | 80294 | 3329H-1-102 | 101919 | 1 |
| | R4 | RESISTOR, CC 8.2 k 5%, 1/4W | 01121 | CB8225 | 101595 | 2 |
| | R5 | Same as R4 | | | | |
| | R6 | RESISTOR, CC 10 Ω 5%, 1/4W | 01121 | CB1005 | 101557 | 1 |
| | R7 | RESISTOR, CC 470 Ω 5%, 1/4W | 01121 | CB4715 | 101625 | 1 |
| | R8 | RESISTOR, Variable 5 k 20%, 1/2W | 80294 | 3329H-1-502 | 101859 | 1 |

## REPLACEABLE PARTS LIST

TITLE A15, SEARCH OSCILLATOR PC ASSEMBLY #05322801 (Cont'd)

| ITEM | REF | COMPONENT DESCRIPTION | MFR'S CODE | MANUFACTURER'S PART NUMBER | SD STOCK NUMBER | T/Q |
|---|---|---|---|---|---|---|
| | R9 | RESISTOR, CC<br>3.9 k 5%, 1/4W | 01121 | CB3925 | 101601 | 1 |
| | R10 | RESISTOR, CC<br>22 k 5%, 1/4W | 01121 | CB2235 | 101572 | 4 |
| | R11 | RESISTOR, CC<br>15 k 5%, 1/4W | 01121 | CB1535 | 101552 | 2 |
| | R12 | RESISTOR, CC<br>100 k 5%, 1/4W | 01121 | CB1045 | 101558 | 2 |
| | R13 | RESISTOR, CC<br>220 k 5%, 1/4W | 01121 | CB2245 | 101610 | 2 |
| | R14 | Same as R13 | | | | |
| | R15 | RESISTOR, CC<br>56 k 5%, 1/4W | 01121 | CB5635 | 101670 | 1 |
| | R16 | RESISTOR, CC<br>16 k 5%, 1/4W | 01121 | CB1635 | 101593 | 1 |
| | R17 | RESISTOR, CC<br>1.5 k 5%, 1/4W | 01121 | CB1525 | 101577 | 1 |
| | R18 | RESISTOR, CC<br>3.3 k 5%, 1/4W | 01121 | CB3325 | 101559 | 3 |
| | R19 | RESISTOR, CC<br>2.7 k 5%, 1/4W | 01121 | CB2725 | 101599 | 2 |
| | R20 | Same as R10 | | | | |
| | R21 | Same as R18 | | | | |
| | R22 | Same as R10 | | | | |
| | R23 | Same as R18 | | | | |
| | R24 | RESISTOR, CC<br>1.8 k 5%, 1/4W | 01121 | CB1825 | 101602 | 1 |
| | R25 | Same as R19 | | | | |
| | R26 | RESISTOR, CC<br>5.6 k 5%, 1/4W | 01121 | CB5625 | 101584 | 2 |
| | R27 | Same as R10 | | | | |
| | R28 | Same as R12 | | | | |
| | R29 | RESISTOR, CC<br>130 k 5%, 1/4W | 01121 | CB1245 | 101603 | 1 |
| | R30 | RESISTOR, Variable<br>20 k 10%, 1/2W | 80294 | 3329H-1-203 | 101942 | 2 |
| | R31 | Same as R11 | | | | |
| | R32 | RESISTOR, CC<br>1 M 5%, 1/4W | 01121 | CB1055 | 101605 | 2 |

# REPLACEABLE PARTS LIST

TITLE A15, SEARCH OSCILLATOR PC ASSEMBLY #05322801 (Cont'd)

| ITEM | REF | COMPONENT DESCRIPTION | MFR'S CODE | MANUFACTURER'S PART NUMBER | SD STOCK NUMBER | T/Q |
|---|---|---|---|---|---|---|
| | R33 | RESISTOR, CC<br>10 k 5%, 1/4W | 01121 | CB1035 | 101570 | 8 |
| | R34 | Same as R33 | | | | |
| | R35 | RESISTOR, CC<br>470 k 5%, 1/4W | 01121 | CB4745 | 101630 | 2 |
| | R36 | RESISTOR, Variable<br>500 k 5%, 1/2W | 11236 | 340PC504B | 102054 | 1 |
| | R37 | Same as R35 | | | | |
| | R38 | Same as R33 | | | | |
| | R39 | Same as R33 | | | | |
| | R40 | RESISTOR, CC<br>39 k 5%, 1/4W | 01121 | CB3935 | 101561 | 3 |
| | R41 | Same as R40 | | | | |
| | R42 | Same as R33 | | | | |
| | R43 | RESISTOR, CC<br>120 k 5%, 1/4W | 01121 | CB1245 | 101580 | 1 |
| | R44 | RESISTOR, Variable<br>10 k 20%, 1/2W | 80294 | 3329H-1-103 | 101916 | 1 |
| | R45 | Same as R40 | | | | |
| | R46 | RESISTOR, CC<br>1 k 5%, 1/4W | 01121 | CB1025 | 101569 | 1 |
| | R47 | Same as R33 | | | | |
| | R48 | RESISTOR, CC<br>4.7 k 5%, 1/4W | 01121 | CB4725 | 101598 | 1 |
| | R49 | RESISTOR, CC<br>510 Ω 5%, 1/4W | 01121 | CB5115 | 101616 | 1 |
| | R50 | Same as R32 | | | | |
| | R51 | RESISTOR, CC<br>150 Ω 5%, 1/4W | 01121 | CB1515 | 101615 | 1 |
| | R52 | Same as R26 | | | | |
| | R53 | RESISTOR, CC<br>6.8 k 5%, 1/4W | 01121 | CB6825 | 101544 | 1 |
| | R54 | RESISTOR, CC<br>430 k 5%, 1/4W | 01121 | CB4345 | 101755 | 1 |
| | R55 | RESISTOR, MF<br>22.6 k 1%, 1/8W | 19701 | MF5C-D-2262-F | 102140 | 2 |
| | R56 | RESISTOR, CC<br>27 k 5%, 1/4W | 01121 | CB2735 | 101587 | 1 |
| | R57 | Same as R30 | | | | |

## REPLACEABLE PARTS LIST

TITLE A15, SEARCH OSCILLATOR PC ASSEMBLY #05322801 (Cont'd)

| ITEM | REF | COMPONENT DESCRIPTION | MFR'S CODE | MANUFACTURER'S PART NUMBER | SD STOCK NUMBER | T/Q |
|---|---|---|---|---|---|---|
| | R58 | Same as R55 | | | | |
| | R59 | Same as R33 | | | | |
| | R60 | Not Used | | | | |
| | R61 | Not Used | | | | |
| | R62 | Same as R33 | | | | |
| | U1 | INTEGRATED CIRCUIT<br>Operational Amplifier | 27014 | LM201AH | 025758 | 2 |
| | U2 | INTEGRATED CIRCUIT<br>Operational Amplifier | 27014 | LM301AH | 025745 | 6 |
| | U3 | INTEGRATED CIRCUIT, LIN AMP<br>Voltage Follower | 27014 | LM302H | 025721 | 1 |
| | U4 | Same as U2 | | | | |
| | U5 | INTEGRATED CIRCUIT, TTL MSI<br>Phase Frequency Detector | 04713 | MC4044P | 045238 | 1 |
| | U6 | Same as U1 | | | | |
| | U7 thru U10 | Same as U2 | | | | |
| | VR1 | DIODE, Zener 4.3V | 03877 | 1N749A | 100419 | 1 |
| | | LUG, Terminal | 88245 | 2000B | 100482 | 2 |
| | | BOARD, PC | 52542 | 053228 | 053228 | 1 |

## REPLACEABLE PARTS LIST

TITLE A16, LO/SHIFTER ACTO MODULE ASSEMBLY #057167 Rev $D_4$ (Figure 7-28)

| ITEM | REF | COMPONENT DESCRIPTION | MFR'S CODE | MANUFACTURER'S PART NUMBER | SD STOCK NUMBER | T/Q |
|---|---|---|---|---|---|---|
| 1 | A16 | ASSEMBLY, LO/Shifter PC | 52542 | 05710401 | 05710401 | 1 |
| 2 | | CASTING, Mod. Component Side | 52542 | 055296 | 055296 | 1 |
| 3 | | CASTING, Mod. Circuit Side | 52542 | 05529701 | 05529701 | 1 |
| 4 | | RAIL, ACTO Module Mounting | 52542 | 053961 | 053961 | 1 |
| 5 | J1,J2 | RECEPTICAL, RF | 98291 | 51-043-4300 | 101251 | 2 |
| 6 | | STUD, 1/4 Turn | 71286 | 551-8 | 103257 | 2 |
| 7 | | RETAINER | 71286 | 553-1 | 100770 | 2 |
| 8 | | BRAID, RFI | 07700 | 20-41210 | 103274 | A/R |
| 9 | | SCREW, PHMS 4-40 x 9/16 | 96906 | MS51957-120 | 100835 | 3 |
| 10 | | SCREW, PHMS 4-40 x 1/4 | 96906 | MS51957-13 | 10062604 | 4 |
| 11 | | WASHER, Split-Lock #4 | 96906 | MS35338-135 | 100711 | 10 |
| 12 | | WASHER, Flat #4 | 96906 | MS15795-803 | 100703 | 4 |
| 13 | L11 | BEAD, Ferrite | 52542 | 112420 | 112420 | 1 |
| 14 | | SCREW, PHMS 4-40 x 5/8 | 96906 | MS51957-18 | 10062610 | 3 |
| 15 | C48,C49 | CAPACITOR, Ceramic<br>.001 µF 20%, 50V | 71590 | CW15C102M | 100251 | 2 |

## REPLACEABLE PARTS LIST

TITLE A16, LO/SHIFTER PC ASSEMBLY #05710401 Rev H (Figure 7-29 & 7-30)

| ITEM | REF | COMPONENT DESCRIPTION | MFR'S CODE | MANUFACTURER'S PART NUMBER | SD STOCK NUMBER | T/Q |
|---|---|---|---|---|---|---|
| | C1 | CAPACITOR, Tant<br>15 µF 10%, 20V | 56289 | 150D156X9020B2 | 100211 | 3 |
| | C2 | Same as C1 | | | | |
| | C3 | CAPACITOR, Tant<br>100 µF 10%, 20V | 56289 | 150D107X9020S2 | 100208 | 1 |
| | C4 | CAPACITOR, Chip<br>13 pF 10%, 500V | 29990 | ATC100B100KC500 | 117044 | 1 |
| | C5 | CAPACITOR, Chip<br>2 pF 10%, 500V | 29990 | ATC100B2R0DC500 | 103184 | 2 |
| | C6 | CAPACITOR, Chip<br>5000 pF 125V | 32159 | R-2180 SPECIAL | 100297 | 2 |
| | C7 | Same as C5 | | | | |
| | C8 | CAPACITOR, Ceramic<br>1000 pF 20%, 50V | 71590 | CW15C102M | 100251 | 11 |
| | C9 | CAPACITOR, Ceramic<br>.1 µF 20%, 50V | 56289 | 5C023104X0500C5 | 100178 | 10 |
| | C10 | Same as C8 | | | | |
| | C11 | Same as C8 | | | | |
| | C12 | CAPACITOR, Chip<br>5.1 pF 500V | 29990 | ATC100B5R1CC500 | 103047 | 1 |
| | C13 | CAPACITOR, Ceramic<br>.05 µF +80-20%, 10V | 71590 | UK10-503 | 100122 | 4 |
| | C14 | Same as C6 | | | | |
| | C15 | Same as C8 | | | | |
| | C16 | Same as C9 | | | | |
| | C17 | Same as C8 | | | | |
| | C18 | Same as C9 | | | | |
| | C19 | Same as C9 | | | | |
| | C20 | Same as C8 | | | | |
| | C21 | Same as C13 | | | | |
| | C22 | CAPACITOR, Ceramic<br>1 µF 20%, 25V | 56289 | 4C02105X0250B3 | 100176 | 2 |
| | C23 | Same as C1 | | | | |
| | C24 thru C26 | Same as C9 | | | | |
| | C27 | Same as C22 | | | | |
| | C28 | Same as C8 | | | | |
| | C29 | Same as C9 | | | | |

## REPLACEABLE PARTS LIST

**TITLE** A16, LO/SHIFTER PC ASSEMBLY #05710401 (Cont'd)

| ITEM | REF | COMPONENT DESCRIPTION | MFR'S CODE | MANUFACTURER'S PART NUMBER | SD STOCK NUMBER | T/Q |
|---|---|---|---|---|---|---|
| | C30 | Same as C8 | | | | |
| | C31 thru C33 | CAPACITOR, DM<br>5 pF 500V | 72136 | DM15CD050DO | 100218 | 3 |
| | C34 | CAPACITOR, Ceramic<br>.1 μF +80-20%, 10V | 71590 | UK10-104 | 100120 | 2 |
| | C35 | Same as C9 | | | | |
| | C36 | CAPACITOR, DM<br>120 pF 5%, 500V | 72136 | DM15FD121JO | 100223 | 1 |
| | C37 | Same as C13 | | | | |
| | C38 | CAPACITOR, Tant<br>56 μF 10%, 6V | 56289 | 150D566X9006D2 | 100225 | 2 |
| | C39 | CAPACITOR, DM<br>180 pF 5%, 500V | 72136 | DM15FD181JO | 100237 | 1 |
| | C40 | Same as C13 | | | | |
| | C41 | Same as C38 | | | | |
| | C42 | Not Used | | | | |
| | C43 | Same as C8 | | | | |
| | C44 | Same as C9 | | | | |
| | C45 | Same as C8 | | | | |
| | C46 | Same as C8 | | | | |
| | C47 | Same as C34 | | | | |
| | CR1 | DIODE, Cap | 04713 | SMV1266 | 100453 | 1 |
| | CR2 | DIODE, Signal 70V | 28480 | 5082-2800 | 100442 | 2 |
| | CR3 | Same as CR2 | | | | |
| | L1 | INDUCTOR, Wire Loop | 52542 | 067636 | 067636 | 1 |
| | L2 | INDUCTOR, Fixed .15 μH 20% | 72259 | DD-0.15 | 101311 | 1 |
| | L3 | INDUCTOR, Fixed 1.0 μH 20% | 99800 | 1537-12 | 101312 | 1 |
| | L4 | INDUCTOR, Fixed .15 μH 20% | 72259 | WEE-0.15 | 101304 | 1 |
| | L5 | INDUCTOR, Fixed 100 μH 5% | 72259 | WEE-100 | 101306 | 2 |
| | L6 | INDUCTOR, Fixed 270 μH 5% | 72259 | WEE-270 | 101302 | 2 |
| | L7 | Same as L5 | | | | |
| | L8 | Same as L6 | | | | |
| | L9 | INDUCTOR, Ferrite Bead | 02114 | 56-590-65/20-3B | 100686 | 2 |
| | L10 | Same as L9 | | | | |
| | Q1 | TRANSISTOR, SIPNP | 04713 | 2N4959 | 101391 | 1 |
| | Q2 | TRANSISTOR, SIPNP | 04713 | MM4049 | 101408 | 1 |

## REPLACEABLE PARTS LIST

TITLE A16, LO/SHIFTER PC ASSEMBLY #05710401 (Cont'd)

| ITEM | REF | COMPONENT DESCRIPTION | MFR'S CODE | MANUFACTURER'S PART NUMBER | SD STOCK NUMBER | T/Q |
|---|---|---|---|---|---|---|
| | Q3 | TRANSISTOR, SINPN 30V | 07263 | PN3643 | 101358 | 1 |
| | Q4 | TRANSISTOR, SIPNP 40V | 04713 | 2N3906 | 101378 | 2 |
| | Q5 | Same as Q4 | | | | |
| | Q6 | TRANSISTOR, SIPNP 20V | 04713 | 2N5109 | 106591 | 2 |
| | Q7 | TRANSISTOR, SINPN 15V | 04713 | 2N3009 | 103388 | 2 |
| | Q8 | Same as Q6 | | | | |
| | Q9 | Same as Q7 | | | | |
| | Q10 | TRANSISTOR, SINPN 40V | 04713 | 2N3904 | 101377 | 2 |
| | Q11 | Same as Q10 | | | | |
| | R1 | RESISTOR, CC<br>10 k 5%, 1/4W | 01121 | CB1035 | 101570 | 3 |
| | R2 | RESISTOR, CC<br>1.5 k 5%, 1/4W | 01121 | CB1525 | 101577 | 3 |
| | R3 | RESISTOR, CC<br>330 Ω 5%, 1/4W | 01121 | CB3315 | 101536 | 5 |
| | R4 | RESISTOR, CC<br>1 k 5%, 1/4W | 01121 | CB1025 | 101569 | 9 |
| | R5 | RESISTOR, CC<br>560 Ω 5%, 1/4W | 01121 | CB5615 | 101583 | 4 |
| | R6 | RESISTOR, CC<br>3.3 k 5%, 1/4W | 01121 | CB3325 | 101559 | 2 |
| | R7 | Same as R6 | | | | |
| | R8 | RESISTOR, CC<br>82 Ω 5%, 1/4W | 01121 | CB8205 | 101629 | 3 |
| | R9 | Same as R8 | | | | |
| | R10 | RESISTOR, CC<br>270 Ω 5%, 1/4W | 01121 | CB2715 | 101542 | 5 |
| | R11<br>thru<br>R14 | Same as R3 | | | | |
| | R15 | Same as R5 | | | | |
| | R16 | Same as R5 | | | | |
| | R17 | Same as R4 | | | | |
| | R18<br>thru<br>R21 | Same as R10 | | | | |
| | R22<br>thru<br>R25 | RESISTOR, CC<br>47 Ω 5%, 1/4W | 01121 | CB4705 | 101560 | 4 |

## REPLACEABLE PARTS LIST

TITLE A16, LO/SHIFTER PC ASSEMBLY #05710401 (Cont'd)

| ITEM | REF | COMPONENT DESCRIPTION | MFR'S CODE | MANUFACTURER'S PART NUMBER | SD STOCK NUMBER | T/Q |
|---|---|---|---|---|---|---|
| | R26 | Same as R4 | | | | |
| | R27 | Same as R2 | | | | |
| | R28 | Same as R4 | | | | |
| | R29 | RESISTOR, CC<br>5.6 k 5%, 1/4W | 01121 | CB5625 | 101584 | 2 |
| | R30 | RESISTOR, CC<br>680 Ω 5%, 1/4W | 01121 | CB6815 | 101669 | 2 |
| | R31 | Same as R4 | | | | |
| | R32 | Same as R2 | | | | |
| | R33 | Same as R4 | | | | |
| | R34 | Same as R29 | | | | |
| | R35 | Same as R30 | | | | |
| | R36 | Same as R4 | | | | |
| | R37 | Same as R5 | | | | |
| | R38 | RESISTOR, CC<br>6.8 k 5%, 1/4W | 01121 | CB6825 | 101544 | 2 |
| | R39 | RESISTOR, CC<br>22 k 5%, 1/4W | 01121 | CB2235 | 101572 | 2 |
| | R40 | Same as R1 | | | | |
| | R41 | Same as R4 | | | | |
| | R42 | RESISTOR, CC<br>130 Ω 5%, 1/4W | 01121 | CB1315 | 101627 | 3 |
| | R43 | Same as R4 | | | | |
| | R44 | Same as R38 | | | | |
| | R45 | Same as R39 | | | | |
| | R46 | Same as R1 | | | | |
| | R47 | Same as R42 | | | | |
| | R48 | RESISTOR, CC<br>100 Ω 5%, 1/4W | 01121 | CB1015 | 101609 | 2 |
| | R49 | RESISTOR, CC<br>15 Ω 5%, 1/4W | 01121 | CB1505 | 101764 | 2 |
| | R50 | Same as R42 | | | | |
| | R51 | Same as R48 | | | | |
| | R52 | RESISTOR, CC<br>18 Ω 5%, 1/4W | 01121 | CB1805 | 101727 | 1 |
| | R53 | Not Used | | | | |
| | R54 | Same as R8 | | | | |

## REPLACEABLE PARTS LIST

TITLE A16, LO/SHIFTER PC ASSEMBLY #05710401 (Cont'd)

| ITEM | REF | COMPONENT DESCRIPTION | MFR'S CODE | MANUFACTURER'S PART NUMBER | SD STOCK NUMBER | T/Q |
|---|---|---|---|---|---|---|
| | R55<br>thru<br>R57 | RESISTOR, CC<br>180 Ω 5%, 1/4W | 01121 | CB1814 | 101668 | 3 |
| | R58 | RESISTOR, Variable<br>1 k 20%, 1/2W | 80294 | 3339P-1-102 | 102167 | 2 |
| | R59 | Same as R58 | | | | |
| | U1 | INTEGRATED CIRCUIT<br>Voltage Regulator 12V | 04713 | MC78L12ACP | 117013 | 1 |
| | U2 | INTEGRATED CIRCUIT, ECL<br>D Master-Slave Flip-Flop | 04713 | MC1690L | 103182 | 2 |
| | U3 | Same as U2 | | | | |
| | U4 | INTEGRATED CIRCUIT, ECL<br>Quad Gate | 04713 | MC10101L | 025791 | 1 |
| | U5 | INTEGRATED CIRCUIT, LIN MSC<br>Bal Mod/Demod | 04713 | MC1495G | 103180 | 3 |
| | U6 | Same as U5 | | | | |
| | U7 | INTEGRATED CIRCUIT, ECL<br>Dual 4-Input Gate | 04713 | MC1660L | 025777 | 1 |
| | | TERMINAL, Swage | 88245 | 2000B1 | 100482 | 2 |
| | | JUMPER, Molded | 50210 | L-2007-1 | 102879 | 6 |
| | | BOARD, PC | 52542 | 057104 | 057104 | 1 |

# REPLACEABLE PARTS LIST

| TITLE | | A17, LOCK IF ACTO MODULE ASSEMBLY #055367 Rev $B_5$ (Figure 7-31) | | | | |
|---|---|---|---|---|---|---|
| ITEM | REF | COMPONENT DESCRIPTION | MFR'S CODE | MANUFACTURER'S PART NUMBER | SD STOCK NUMBER | T/Q |
| 1 | A17 | ASSEMBLY, Lock IF PC | 52542 | 05321801 | 05321801 | 1 |
| 2 | | CASTING, Mod. Component Side | 52542 | 055290 | 055290 | 1 |
| 3 | | CASTING, Mod. Circuit Side | 52542 | 055289 | 055289 | 1 |
| 4 | | RAIL, ACTO Mod Mtg. | 52542 | 053961 | 053961 | 1 |
| 5 | J1 | RECEPTICAL, RF | 98291 | 51-043-4300 | 101251 | 1 |
| 6 | | STUD, 1/4 Turn | 71286 | 5S1-8 | 103257 | 2 |
| 7 | | RETAINER | 71286 | 5S3-1 | 100770 | 2 |
| 8 | | BRAID, RFI | 07700 | 20-41110 | 103274 | A/R |
| 9 | | SCREW, PHMS 4-40 x 9/16 | 96906 | MS51957-120 | 100835 | 3 |
| 10 | | SCREW, PHMS 4-40 x 1/4 | 96906 | MS51957-13 | 10062604 | 4 |
| 11 | | WASHER, Split-Lock #4 | 96906 | MS35338-135 | 100711 | 10 |
| 12 | | WASHER, Flat #4 | 96906 | MS15795-803 | 100703 | 4 |
| 13 | | SCREW, PHMS 4-40 x 5/8 | 96906 | MS51957-18 | 10062610 | 3 |

## REPLACEABLE PARTS LIST

| TITLE | A17, LOCK IF PC ASSEMBLY #05321801 Rev F (Figure 7-32 & 7-33) | | | | | |
|---|---|---|---|---|---|---|
| **ITEM** | **REF** | **COMPONENT DESCRIPTION** | **MFR'S CODE** | **MANUFACTURER'S PART NUMBER** | **SD STOCK NUMBER** | **T/Q** |
| | C1 | CAPACITOR, Ceramic<br>1000 pF 20%, 50V | 71590 | CW15C102M | 100251 | 13 |
| | C2 | CAPACITOR, Ceramic<br>1 µF 20%, 25V | 56289 | 5CZ5U105X0050C5 | 100176 | 5 |
| | C3 | CAPACITOR, Variable<br>5.5-18 pF | 72982 | 538-011A5.5-18 | 100136 | 9 |
| | C4 | Same as C3 | | | | |
| | C5 | Same as C1 | | | | |
| | C6 | CAPACITOR, Ceramic<br>.1 µF 20%, 50V | 56289 | 5C023104X0500C5 | 100178 | 5 |
| | C7 | Same as C1 | | | | |
| | C8 | Not Used | | | | |
| | C9 | Same as C2 | | | | |
| | C10 | Same as C3 | | | | |
| | C11 | CAPACITOR, Ceramic<br>6.8 pF 1000V | 56289 | 10TCC-V68 | 106490 | 2 |
| | C12 | Same as C3 | | | | |
| | C13 | Same as C1 | | | | |
| | C14 | Same as C6 | | | | |
| | C15 | Same as C1 | | | | |
| | C16 | Not Used | | | | |
| | C17 | Same as C2 | | | | |
| | C18 | Same as C3 | | | | |
| | C19 | Same as C11 | | | | |
| | C20 | Same as C3 | | | | |
| | C21 | Same as C1 | | | | |
| | C22 | Same as C6 | | | | |
| | C23 | Same as C1 | | | | |
| | C24 | Not Used | | | | |
| | C25 | Same as C2 | | | | |
| | C26 | Same as C3 | | | | |
| | C27<br>thru<br>C29 | Same as C1 | | | | |
| | C30 | Same as C2 | | | | |
| | C31 | CAPACITOR, DP Ceramic<br>.01 µF 20%, 100V | 04222 | 3429100C103M | 117570 | 5 |
| | C32 | Same as C1 | | | | |

## REPLACEABLE PARTS LIST

TITLE A17, LOCK IF PC ASSEMBLY #05321801 (Cont'd)

| ITEM | REF | COMPONENT DESCRIPTION | MFR'S CODE | MANUFACTURER'S PART NUMBER | SD STOCK NUMBER | T/Q |
|---|---|---|---|---|---|---|
| | C33 | Same as C3 | | | | |
| | C34 | CAPACITOR, Variable 2.0 - 8 pF | 72982 | 538-011A2.0-8 | 117156 | 1 |
| | C35 | Same as C3 | | | | |
| | C36 | Same as C1 | | | | |
| | C37 | Same as C31 | | | | |
| | C38 | Same as C31 | | | | |
| | C39 | CAPACITOR, Ceramic .05 µF +80-20%, 10V | 71590 | UK10-503 | 100122 | 5 |
| | C40 | Same as C31 | | | | |
| | C41 | Same as C1 | | | | |
| | C42 thru C48 | CAPACITOR, DM 33 pF 5%, 500V | 72136 | DM15ED330JO | 100175 | 7 |
| | C49 thru C52 | Same as C39 | | | | |
| | C53 | Same as C6 | | | | |
| | C54 | Same as C6 | | | | |
| | C55 | Same as C31 | | | | |
| | CR1 thru CR3 | DIODE, Signal 50V | 03508 | 1N4151 | 100385 | 3 |
| | DL1 | ASSEMBLY, Delay Line | 52542 | 057669 | 057669 | 1 |
| | L1 | INDUCTOR, Fixed 10 µH 10% | 72259 | WEE-WEE-10 | 101317 | 1 |
| | L2 | INDUCTOR, Fixed 2.2 µH 5% | 78526 | SSD-2.2 5% | 10130901 | 1 |
| | L3 | INDUCTOR, Fixed 1.8 µH 5% | 78526 | SSD-1.8 5% | 10138701 | 3 |
| | L4 | INDUCTOR, Fixed 100 µH 5% | 72259 | WEE-100 | 101306 | 4 |
| | L5 | INDUCTOR, Fixed 1.5 µH 5% | 78526 | SSD-1.5 5% | 10132601 | 5 |
| | L6 | Same as L5 | | | | |
| | L7 | Same as L4 | | | | |
| | L8 | Same as L5 | | | | |
| | L9 | Same as L5 | | | | |
| | L10 | Same as L4 | | | | |
| | L11 | Same as L5 | | | | |
| | L12 | Same as L4 | | | | |
| | L13 | INDUCTOR, Fixed 2.7 µH 10% | 72259 | WEE-2.7 | 102199 | 1 |

## REPLACEABLE PARTS LIST

TITLE A17, LOCK IF PC ASSEMBLY #05321801 (Cont'd)

| ITEM | REF | COMPONENT DESCRIPTION | MFR'S CODE | MANUFACTURER'S PART NUMBER | SD STOCK NUMBER | T/Q |
|---|---|---|---|---|---|---|
| | L14 | Same as L3 | | | | |
| | L15 | Same as L3 | | | | |
| | L16 | INDUCTOR, Fixed 6.8 μH 10% | 72259 | WEE-6.8 | 101300 | 2 |
| | L17 | Same as L16 | | | | |
| | L18 | INDUCTOR, Bead Shielding | 52542 | 112420 | 112420 | 2 |
| | L19 | Same as L18 | | | | |
| | Q1 thru Q3 | TRANSISTOR, MOSFET Dual Gate | 04713 | MFE121 | 101413 | 3 |
| | Q4 | TRANSISTOR, JFET P-Channel | 04713 | 2N3993 | 103347 | 1 |
| | Q5 thru Q8 | TRANSISTOR, SINPN 15V | 04713 | PN3646 | 101369 | 4 |
| | Q9 | TRANSISTOR, JFET N-Channel | 27014 | 2N3954 | 102717 | 1 |
| | Q10 | TRANSISTOR, SIPNP 12V | 07263 | PN3640-18 | 101357 | 1 |
| | R1 | RESISTOR, CC 82 Ω 5%, 1/4W | 01121 | CB8205 | 101629 | 2 |
| | R2 | RESISTOR, CC 270 k 5%, 1/4W | 01121 | CB2745 | 101769 | 6 |
| | R3 | RESISTOR, CC 3.9 k 5%, 1/4W | 01121 | CB3925 | 101601 | 1 |
| | R4 | Same as R2 | | | | |
| | R5 | RESISTOR, CC 750 k 5%, 1/4W | 01121 | CB7545 | 101585 | 3 |
| | R6 | RESISTOR, CC 560 Ω 5%, 1/4W | 01121 | CB5615 | 101583 | 3 |
| | R7 | RESISTOR, CC 1.8 k 5%, 1/4W | 01121 | CB1825 | 101602 | 5 |
| | R8 | Same as R7 | | | | |
| | R9 | Same as R2 | | | | |
| | R10 | Same as R5 | | | | |
| | R11 | Not Used | | | | |
| | R12 | Same as R7 | | | | |
| | R13 | Same as R7 | | | | |
| | R14 | Same as R2 | | | | |
| | R15 | Same as R5 | | | | |
| | R16 | Not Used | | | | |
| | R17 | Same as R7 | | | | |

# REPLACEABLE PARTS LIST

TITLE A17, LOCK IF PC ASSEMBLY #05321801 (Cont'd)

| ITEM | REF | COMPONENT DESCRIPTION | MFR'S CODE | MANUFACTURER'S PART NUMBER | SD STOCK NUMBER | T/Q |
|---|---|---|---|---|---|---|
| | R18 | RESISTOR, CC<br>33 Ω 5%, 1/4W | 01121 | CB3305 | 101731 | 4 |
| | R19 | RESISTOR, CC<br>22 k 5%, 1/4W | 01121 | CB2235 | 101572 | 1 |
| | R20 | RESISTOR, Variable<br>100 k 20%, 1/2W | 80294 | 3339H-1-104 | 102298 | 1 |
| | R21 | RESISTOR, CC<br>100 k 5%, 1/4W | 01121 | CB1045 | 101558 | 2 |
| | R22 | RESISTOR, CC<br>150 Ω 5%, 1/4W | 01121 | CB1515 | 101615 | 1 |
| | R23 | RESISTOR, CC<br>1.5 k 5%, 1/4W | 01121 | CB1525 | 101577 | 2 |
| | R24 | Same as R23 | | | | |
| | R25 | RESISTOR, CC<br>1 k 5%, 1/4W | 01121 | CB1025 | 101569 | 3 |
| | R26 | RESISTOR, CC<br>150 k 5%, 1/4W | 01121 | CB1545 | 101604 | 1 |
| | R27 | RESISTOR, Variable<br>5 k 20%, 1/2W | 80294 | 3339H-1-502 | 102099 | 3 |
| | R28 | RESISTOR, CC<br>2.7 k 5%, 1/4W | 01121 | CB2725 | 101599 | 2 |
| | R29 | Same as R21 | | | | |
| | R30 | RESISTOR, CC<br>220 Ω 5%, 1/4W | 01121 | CB2215 | 101566 | 2 |
| | R31 | Same as R28 | | | | |
| | R32 | RESISTOR, CC<br>5.6 k 5%, 1/4W | 01121 | CB5625 | 101584 | 1 |
| | R33 | Same as R30 | | | | |
| | R34 | Same as R6 | | | | |
| | R35 | Same as R27 | | | | |
| | R36 | Same as R6 | | | | |
| | R37 | RESISTOR, CC<br>330 Ω 5%, 1/4W | 01121 | CB3315 | 101536 | 6 |
| | R38 | Same as R37 | | | | |
| | R39 | Same as R1 | | | | |
| | R40 | RESISTOR, CC<br>130 Ω 5%, 1/4W | 01121 | CB1314 | 101627 | 1 |
| | R41<br>thru<br>R44 | Same as R37 | | | | |

## REPLACEABLE PARTS LIST

TITLE A17, LOCK IF PC ASSEMBLY #05321801 (Cont'd)

| ITEM | REF | COMPONENT DESCRIPTION | MFR'S CODE | MANUFACTURER'S PART NUMBER | SD STOCK NUMBER | T/Q |
|---|---|---|---|---|---|---|
| | R45 | RESISTOR, CC<br>5.1 k 5%, 1/4W | 01121 | CB5125 | 101541 | 2 |
| | R46 | RESISTOR, CC<br>100 Ω 5%, 1/4W | 01121 | CB1015 | 101609 | 1 |
| | R47 | Same as R25 | | | | |
| | R48 | Same as R45 | | | | |
| | R49 | Same as R27 | | | | |
| | R50 | RESISTOR, CC<br>8.2 k 5%, 1/4W | 01121 | CB8225 | 101595 | 1 |
| | R51 | RESISTOR, CC<br>2.2 k 5%, 1/4W | 01121 | CB2225 | 101562 | 2 |
| | R52 | RESISTOR, CC<br>3 k 5%, 1/4W | 01121 | CB3025 | 101548 | 1 |
| | R53 | Same as R25 | | | | |
| | R54 | Same as R51 | | | | |
| | R55 | RESISTOR, CC<br>470 Ω 5%, 1/4W | 01121 | CB4715 | 101625 | 1 |
| | R56 | Same as R2 | | | | |
| | R57 | Same as R2 | | | | |
| | R58 thru R60 | Same as R18 | | | | |
| | RT1 | THERMISTOR, 1 k | 83186 | 31 D 10 | 117404 | 2 |
| | RT2 | Same as RT1 | | | | |
| | U1 | INTEGRATED CIRCUIT<br>Linear Amp 40 dB 50 MHz | 04713 | MC1590G | 025788 | 1 |
| | U2 | INTEGRATED CIRCUIT<br>Operational Amplifier | 27014 | LM301AH | 025745 | 1 |
| | U3 | INTEGRATED CIRCUIT, ECL<br>Exclusive OR/NOR Gate | 04713 | MC10107P | 103179 | 1 |
| | U4 | INTEGRATED CIRCUIT<br>Linear Amp Voltage Follower | 27014 | LM302H | 025721 | 1 |
| | VR1 | DIODE, Zener 5.1V | 03877 | 1N751A | 100378 | 1 |
| | | TERMINAL, Swage | 88245 | 2000B1 | 100482 | 4 |
| | | SCREW, PHMS 4-40 x 5/16 | 96906 | MS51957-14 | 10062605 | 1 |
| | | WASHER, Split-Lock #4 | 96906 | MS15795-135 | 100711 | 1 |
| | | BEAD, Glass | | By Description | 102838 | 2 |
| | | BOARD, PC | 52542 | 053218 | 053218 | 1 |

# REPLACEABLE PARTS LIST

TITLE A22, 500 MHz PRE AMPLIFIER PC ASSEMBLY #06748401 Rev E (Figure 7-34 & 7-35)

| ITEM | REF | COMPONENT DESCRIPTION | MFR'S CODE | MANUFACTURER'S PART NUMBER | SD STOCK NUMBER | T/Q |
|---|---|---|---|---|---|---|
| | C1 | CAPACITOR, DP Ceramic .01 µF 20%, 100V | 04222 | 3429100C103M | 117570 | 6 |
| | C2 | Same as C1 | | | | |
| | C3 | CAPACITOR, DP Ceramic 27 pF 5%, 100V | 96733 | DB44BY270J | 117640 | 1 |
| | C4 thru C7 | Same as C1 | | | | |
| | C8 | CAPACITOR, DM 390 pF 5%, 500V | 72136 | DM15FD391JO | 100170 | A/R |
| | CR1 thru CR3 | DIODE, Signal 50V | 03508 | 1N4151 | 100385 | 3 |
| | L1 | INDUCTOR, Fixed 1000 µH 10% | 72259 | WEE-1000 | 101303 | 1 |
| | L2 | INDUCTOR, Fixed 470 µH 5% | 72259 | WEE-470 | 101297 | 1 |
| | L3 | INDUCTOR, Fixed .15 µH 10% | 72259 | DD-0.15 | 101311 | A/R |
| | Q1 | TRANSISTOR, SINPN 15V | 04713 | BFR 90 | 103948 | 1 |
| | R1 | RESISTOR, CC 2.2 k 5%, 1/8W | 01121 | BB2225 | 101719 | 1 |
| | R2 | RESISTOR, CC 2.2 k 5%, 1/4W | 01121 | CB2225 | 101562 | 1 |
| | R3 | RESISTOR, CC 510 Ω 5%, 1/4W | 01121 | CB5115 | 101616 | 1 |
| | R4 | RESISTOR, CC 22 Ω 5%, 1/4W | 01121 | CB2205 | 101696 | 1 |
| | R5 | RESISTOR, CC 68 Ω 5%, 1/8W | 01121 | BB6805 | 101700 | 1 |
| | | CABLE, Input | 52542 | 057442 | 057442 | 1 |
| | | CABLE, Output | 52542 | 057443 | 057443 | 1 |
| | | BOARD, PC | 52542 | 067484 | 067484 | 1 |

## REPLACEABLE PARTS LIST

TITLE A29, ACTO EXTENDER ASSEMBLY #05502801 Rev A (Figure 7-75)

| ITEM | REF | COMPONENT DESCRIPTION | MFR'S CODE | MANUFACTURER'S PART NUMBER | SD STOCK NUMBER | T/Q |
|---|---|---|---|---|---|---|
| 1 | | BOARD, PC | 52542 | 055028 | 055028 | 1 |
| 2 | | BRACKET, ACTO Extender | 52542 | 055326 | 055326 | 1 |
| 3 | | CONNECTOR, PC Edge 10-pos | 05574 | 2VK10D/1-2 | 101253 | 1 |
| 5 | | WASHER, Flat #6 | 86928 | 5710-23-10 | 100662 | 4 |
| 6 | | SUTD, 1-4 turn | 71286 | 551-8 | 103257 | 2 |
| 7 | | RETAINER | 71286 | 553-1 | 100770 | 2 |
| 8 | | SCREW, PHMS 6-32 x 3/8 | 96906 | MS51957-28 | 10063206 | 4 |
| 9 | | WASHER, Split-Lock #6 | 96906 | MS35338-136 | 100712 | 4 |
| | | **A28, DIGITAL EXTENDER ASSEMBLY #05502901 Rev A (Figure 7-76)** | | | | |
| 1 | | BOARD, PC | 52542 | 055029 | 055029 | 1 |
| 2 | | CONNECTOR, PC Edge 18 pos. | 05574 | 2VK18D/4-12 | 103190 | 2 |

## REPLACEABLE PARTS LIST

| TITLE | | OPTION 04, FINAL ASSEMBLY #055500 Rev A (Figure 7-48) | | | | |
|---|---|---|---|---|---|---|
| ITEM | REF | COMPONENT DESCRIPTION | MFR'S CODE | MANUFACTURER'S PART NUMBER | SD STOCK NUMBER | T/Q |
| | | DELETE | | | | |
| 10 | | PLATE, BCD & Remote Cover | 52542 | 055229 | 055229 | 1 |
| 11 | W1,2,3 | JUMPER, 22 GA | 55210 | L-2007-1 | 102879 | 3 |
| | | ADD | | | | |
| 22 | | ASSEMBLY, BCD Remote Cable w/A2A5J1 and A2A5J2 | 52542 | 055499 | 055499 | 1 |
| 23 | A2A5P1 | PLUG, W/Hood 50-pin | 02660 | 57-30500 | 101157 | 1 |
| 24 | A2A5P2 | PLUG, W/Hood 36-pin | 02660 | 57-30360 | 101158 | 1 |
| 27 | | WASHER, Split-Lock #2 | 96906 | MS35337-77 | 100661 | 4 |
| 28 | | SCREW, PHMS 2-56 x 1/4 | 96906 | MS51957-3 | 10062504 | 4 |

## REPLACEABLE PARTS LIST

TITLE OPTION 04, BCD & REMOTE CABLE ASSEMBLY #055499 Rev A (Figure 7-49)

| ITEM | REF | COMPONENT DESCRIPTION | MFR'S CODE | MANUFACTURER'S PART NUMBER | SD STOCK NUMBER | T/Q |
|---|---|---|---|---|---|---|
| 1 | A2 | ASSEMBLY, BCD Output PC | 52542 | 05344604 | 05344604 | 1 |
| 2 | A5 | ASSEMBLY, RemotePC | 52542 | 05339001 | 05339001 | 1 |
| 3 | | CABLE, BCD-Remote | 52542 | 055498 | 055498 | 1 |
| 4 | | TIE, Cable | 06383 | SSTIM | 100753 | 2 |
| 5 | | TIE, Anchor | 06383 | TMIS4C | 102747 | 2 |
| 6 | | SCREW, PHMS 4-40 x 1/4 | 96906 | MS51957-13 | 10062604 | 2 |
| 7 | | WASHER, Split-Lock #4 | 96906 | MS35338-135 | 100711 | 2 |
| 8 | | NUT, Hex 4-40 | 96906 | NAS671C4 | 100622 | 2 |

## REPLACEABLE PARTS LIST

TITLE OPTION 04, A2 BCD OUTPUT PC ASSEMBLY #05344604 Rev B (Figure 7-51 & 7-52)

| ITEM | REF | COMPONENT DESCRIPTION | MFR'S CODE | MANUFACTURER'S PART NUMBER | SD STOCK NUMBER | T/Q |
|---|---|---|---|---|---|---|
| | C1 | CAPACITOR, Ceramic<br>.05 μF +80-20%, 10V | 71590 | UK10-503 | 100122 | 2 |
| | C2 | Same as C1 | | | | |
| | Q1 | TRANSISTOR, SINPN 15V | 07263 | PN3646 | 101369 | 2 |
| | Q2 | Same as Q1 | | | | |
| | R1 | RESISTOR, CC<br>5.1 k 5%, 1/4W | 01121 | CB5125 | 101541 | 2 |
| | R2 | RESISTOR, CC<br>3.3 k 5%, 1/4W | 01121 | CB3325 | 101559 | 2 |
| | R3 | RESISTOR, CC<br>6.8 k 5%, 1/4W | 01121 | CB2435 | 101554 | 1 |
| | R4 | Same as R2 | | | | |
| | R5 | RESISTOR, CC<br>4.7 k 5%, 1/4W | 01121 | CB4726 | 101598 | 2 |
| | R6 | Same as R1 | | | | |
| | R7 | Same as R5 | | | | |
| | R8 | RESISTOR, CC<br>2.2 k 5%, 1/4W | 01121 | CB2225 | 101562 | 2 |
| | R9 | Same as R8 | | | | |
| | R10 | RESISTOR, CC<br>12 k 5%, 1/4W | 01121 | CB1235 | 101565 | 1 |
| | U1<br>thru<br>U9 | INTEGRATED CIRCUIT, TTL SSI<br>Hex Inverter | 01295 | SN7417N | 106629 | 9 |
| | U10<br>thru<br>U22 | INTEGRATED CIRCUIT<br>Resistor Module 4-5 k 20% | 52542 | 027867 | 027867 | 13 |
| | W1 | JUMPER, Molded | 55210 | L-2007-1 | 102879 | 1 |
| | | EXTRACTOR, Hot Stamped A2 | 52542 | 03984202 | 03984202 | 1 |
| | | EXTRACTOR | 51495 | 1743 | 100865 | 1 |
| | | ROLL PIN | 73957 | 50-094-0250 | 100752 | 2 |
| | | BOARD, PC | 52542 | 053446 | 053446 | 1 |

## REPLACEABLE PARTS LIST

TITLE OPTION 04, A5 REMOTE PC ASSEMBLY #05339001 Rev B (Figure 7-53 & 7-54)

| ITEM | REF | COMPONENT DESCRIPTION | MFR'S CODE | MANUFACTURER'S PART NUMBER | SD STOCK NUMBER | T/Q |
|---|---|---|---|---|---|---|
| | C1 | CAPACITOR, Ceramic<br>.05 µF +80-20%, 10V | 71590 | UK10-503 | 100122 | 1 |
| | C2 | CAPACITOR, Ceramic<br>.001 µF 20%, 50V | 71590 | CW15C102M | 100251 | 1 |
| | R1 | RESISTOR, CC<br>1 k 5%, 1/4W | 01121 | CB1025 | 101569 | 2 |
| | R2 thru R4 | RESISTOR, CC<br>12 k 5%, 1/4W | 01121 | CB1235 | 101565 | 3 |
| | R5 | RESISTOR, CC<br>10 k 5%, 1/4W | 01121 | CB1035 | 101570 | 1 |
| | R6 | Same as R1 | | | | |
| | U1 | INTEGRATED CIRCUIT, TTL SSI<br>Hex Inverter | 01295 | SN7416N | 045230 | 2 |
| | U2 thru U5 | INTEGRATED CIRCUIT, TTL SSI<br>4 3-State Bus Buffer | 01295 | SN74126N | 045298 | 4 |
| | U6 | Same as U1 | | | | |
| | U7 thru U9 | INTEGRATED CIRCUIT<br>Resistor Module 4-12 k 20% | 52542 | 045008 | 045008 | 3 |
| | | EXTRACTOR, Hot Stamped A5 | 52542 | 03984205 | 03984205 | 1 |
| | | EXTRACTOR | 51495 | 1743 | 100865 | 1 |
| | | ROLL PIN | 73957 | 50-094-0250 | 100752 | 2 |
| | | BOARD, PC | 52542 | 053390 | 053390 | 1 |

## REPLACEABLE PARTS LIST

TITLE OPTION 05, IEEE 488 FINAL ASSEMBLY #057359 Rev D (Figure 7-56)

| ITEM | REF | COMPONENT DESCRIPTION | MFR'S CODE | MANUFACTURER'S PART NUMBER | SD STOCK NUMBER | T/Q |
|---|---|---|---|---|---|---|
| | | **DELETE** | | | | |
| | | PLATE, BCD/REMOTE Cover (P/O Rear Panel) | 52542 | 055229 | 055229 | 1 |
| | | **ADD** | | | | |
| 9 | | ASSEMBLY, Cable Option 05 | 52542 | 057362 | 057263 | 1 |
| 26 | | SCREW, FHMS 2-56 x 1/4 | 96906 | NAS662C24R4 | 10070004 | 2 |
| 27 | | SCREW, PHMS 2-56 x 7/16 | 96906 | MS51957-3 | 10062507 | 2 |
| 28 | | SCREW, PHMS 6-32 x 5/16 | 96906 | MS51057-27 | 10063205 | 3 |
| 30 | | WASHER, Split-Lock #2 | 96906 | MS35337-77 | 100661 | 2 |
| 31 | | WASHER, Split-Lock #6 | 96906 | MS35338-136 | 100712 | 3 |
| 32 | | WASHER, Flat #6 | 96906 | MS15795-805 | 100704 | 3 |
| 33 | | NUT, Hex 2-56 | 96906 | MS35649-224 | 100636 | 2 |
| 35 | A21 | ASSEMBLY, Sample Rate & Control PC | 52542 | 05788601 | 05788601 | 1 |
| 38 | | SCREW, PHMS 6-32 x 3/4 | 96906 | MS51957-32 | 10063212 | 2 |
| 39 | | WASHER, Flat #6 | 96906 | MS15795-805 | 100704 | 2 |
| 40 | | NUT, Hex 6-32 | 96906 | MS35649-264 | 100706 | 2 |
| 41 | | WASHER, Flat #6 | 86928 | 5710-23-10 | 100662 | 2 |

## REPLACEABLE PARTS LIST

TITLE OPTION 05, IEEE 488 CABLE ASSEMBLY #057362 Rev $B_2$ (Figure 7-55)

| ITEM | REF | COMPONENT DESCRIPTION | MFR'S CODE | MANUFACTURER'S PART NUMBER | SD STOCK NUMBER | T/Q |
|---|---|---|---|---|---|---|
| 1 | | HARNESS, Cable | 52542 | 057363 | 057363 | 1 |
| 2 | A2 | ASSEMBLY, IEEE 488 BCD Out PC | 52542 | 05725701 | 05725701 | 1 |
| 3 | A5 | ASSEMBLY, IEEE 488 Programming PC | 52542 | 05725601 | 05725601 | 1 |
| 4 | A7 | ASSEMBLY, IEEE 488 Offset PC | 52542 | 05725901 | 05725901 | 1 |
| 5 | A20 | ASSEMBLY, IEEE 488 I/O PC | 52542 | 05725401 | 05725401 | 1 |
| 6 | | TIE, Cable | 06383 | SSTIM | 100753 | 3 |
| | | **OPTION 05, IEEE 488 CABLE HARNESS #057363 Rev $B_2$** | | | | |
| 1 | | CONNECTOR, 24-pin (P/O Rear Panel) | 02660 | 57-20240-2(383) | 117054 | 1 |
| 2 | | PLATE, Connector | 52542 | 057273 | 057273 | 1 |
| 3 | | RETAINER, Connector | 52542 | 057361 | 057361 | 2 |
| 5 | | ASSEMBLY, Switch Plate | 52542 | 057358 | 057358 | 1 |
| 6 | | TIE, Nylon Cable | 06383 | SSTIM | 100753 | A/R |
| 7 | | TIE, Anchor | 06383 | TMIS6 | 102748 | 1 |
| | | **OPTION 05, IEEE 488 SWITCH PLATE ASSEMBLY #057358 Rev B** | | | | |
| 1 | | PLATE, Switch | 52542 | 057268 | 057268 | 1 |
| 2 | S1 - S6 | SWITCH, SPDT Slide | 79727 | GS111SPDTG10 | 117573 | 6 |
| 3 | | RIVET | 12014 | R3484 x 1/8 NICL | 100924 | 12 |

## REPLACEABLE PARTS LIST

TITLE OPTION 05, A2 IEEE 488 BCD OUT PC ASSEMBLY #05725701 Rev D (Figure 7-58 & 7-59)

| ITEM | REF | COMPONENT DESCRIPTION | MFR'S CODE | MANUFACTURER'S PART NUMBER | SD STOCK NUMBER | T/Q |
|---|---|---|---|---|---|---|
| | C1 | CAPACITOR, Tant<br>39 µF 10%, 10V | 56289 | 150D396X9010B2 | 100183 | 1 |
| | C2<br>thru<br>C5 | CAPACITOR, Ceramic<br>.05 µF +80-20%, 10V | 71590 | UK10-503 | 100122 | 4 |
| | U1 | INTEGRATED CIRCUIT, TTL MSI<br>Presettable Binary Counter | 01295 | SN74LS197N | 103165 | 1 |
| | U2 | INTEGRATED CIRCUIT, TTL<br>ROM Programmed | 52542 | 057082 | 057082 | 1 |
| | U3<br>thru<br>U6 | INTEGRATED CIRCUIT, TTL MSI<br>16-1 Selector Invertor | 01295 | SN74150N | 106637 | 4 |
| | U7 | INTEGRATED CIRCUIT, PROM<br>Special Program | 52542 | 067271 | 067271 | 1 |
| | U8<br>thru<br>U10 | Not Used | | | | |
| | U11 | INTEGRATED CIRCUIT<br>Resistor Module 4-12 k 20% | 52542 | 045008 | 045008 | 1 |
| | | EXTRACTOR, Hot Stamped A2 | 52542 | 03984202 | 03984202 | 1 |
| | | EXTRACTOR | 51495 | 1743 | 100865 | 1 |
| | | ROLL PIN | 73957 | 50-094-0250 | 100752 | 2 |
| | | BOARD, PC | 52542 | 057257 | 057257 | 1 |

# REPLACEABLE PARTS LIST

TITLE OPTION 05, A5 IEEE 488 PROGRAMMING PC ASSEMBLY #05725601 Rev B (Figure 7-60 & 7-61)

| ITEM | REF | COMPONENT DESCRIPTION | MFR'S CODE | MANUFACTURER'S PART NUMBER | SD STOCK NUMBER | T/Q |
|---|---|---|---|---|---|---|
| | C1 | CAPACITOR, Tant<br>39 μF 10%, 10V | 56289 | 150D396X9010B2 | 100183 | 1 |
| | C2<br>thru<br>C9 | CAPACITOR, Ceramic<br>.05 μF +80-20%, 10V | 71590 | UK10-503 | 100122 | 8 |
| | U1 | INTEGRATED CIRCXIT, TTL SSI<br>Dual 2-Input NAND Gate | 01295 | SN74LS08N | 103967 | 5 |
| | U2 | INTEGRATED CIRCUIT, TTL SSI<br>Dual D Flip-Flop | 01295 | SN74LS74N | 103132 | 3 |
| | U3 | Same as U2 | | | | |
| | U4 | INTEGRATED CIRCUIT, TTL SSI<br>Hex Inverter | 01295 | SN74LS04N | 103749 | 1 |
| | U5 | Same as U1 | | | | |
| | U6 | INTEGRATED CIRCUIT, TTL SSI<br>Quad 2-Input NAND Gate | 01295 | SN74LS00N | 103130 | 3 |
| | U7 | INTEGRATED CIRCUIT, TTL SSI<br>Hex Inverter | 01295 | SN7416N | 045230 | 1 |
| | U8 | INTEGRATED CIRCUIT, TTL MSI<br>4-10 Line Decoder/Driver | 01295 | SN74145 | 025754 | 1 |
| | U9 | INTEGRATED CIRCUIT, TTL SSI<br>Quad 2-Input NAND Gate | 01295 | SN7426N | 045252 | 2 |
| | U10 | Same as U9 | | | | |
| | U11 | Same as U1 | | | | |
| | U12 | Same as U2 | | | | |
| | U13 | Same as U1 | | | | |
| | U14 | Same as U6 | | | | |
| | U15 | Same as U1 | | | | |
| | U16 | INTEGRATED CIRCUIT, TTL SSI<br>Quad 3-Input NAND Gate | 01295 | SN74LS10N | 103968 | 1 |
| | U17 | Same as U6 | | | | |
| | | EXTRACTOR, Hot Stamped A5 | 52542 | 03984205 | 03984205 | 1 |
| | | EXTRACTOR | 51495 | 1743 | 100865 | 1 |
| | | ROLL PIN | 73957 | 50-094-0250 | 100752 | 2 |
| | | BOARD, PC | 52542 | 057256 | 057256 | 1 |

## REPLACEABLE PARTS LIST

TITLE OPTION 05, A7 IEEE 488 UNIVERSAL OFFSET PC ASSEMBLY #05725901 **(Figure 7-62 & 7-63)**

| ITEM | REF | COMPONENT DESCRIPTION | MFR'S CODE | MANUFACTURER'S PART NUMBER | SD STOCK NUMBER | T/Q |
|---|---|---|---|---|---|---|
| | C1 | CAPACITOR, DM<br>1000 pF 5%, 100V | 72136 | DM15FA102JO | 100243 | 2 |
| | C2 | CAPACITOR, DM<br>330 pF 5%, 100V | 72136 | DM15FD331JO | 100276 | 4 |
| | C3 | Same as C2 | | | | |
| | C4 | Same as C1 | | | | |
| | C5 | Same as C2 | | | | |
| | C6 | Same as C2 | | | | |
| | C7 | CAPACITOR, Tant<br>39 $\mu$F 10%, 10V | 56289 | 150D396X9010B2 | 100183 | 1 |
| | C8 thru C10 | CAPACITOR, Ceramic<br>.05 $\mu$F 10%, 10V | 71590 | UK10-503 | 100122 | 3 |
| | R1 thru R6 | RESISTOR, CC<br>22 k 5%, 1/4W | 01121 | CB2235 | 101572 | 6 |
| | U1 | INTEGRATED CIRCUIT<br>Quad 2-Input Positive OR Gate | 01295 | SN74LS32N | 103972 | 1 |
| | U2 | INTEGRATED CIRCUIT, TTL SSI<br>Dual Trigger One Shot | 01295 | SN74LS123N | 103976 | 3 |
| | U3 | INTEGRATED CIRCUIT, TTL SSI<br>Dual 4-Input NAND Gate | 01295 | SN74LS20N | 103969 | 1 |
| | U4 | INTEGRATED CIRCUIT, TTL SSI<br>2-Input NAND Gate | 01295 | SN74LS08N | 103967 | 2 |
| | U5 | INTEGRATED CIRCUIT, TTL SSI<br>Quad 2-Input NAND Gate | 01295 | SN74LS00N | 103130 | 1 |
| | U6 | Same as U4 | | | | |
| | U7 | Same as U2 | | | | |
| | U8 | INTEGRATED CIRCUIT<br>Dual D Flip-Flop | 01295 | SN74LS74N | 103132 | 2 |
| | U9 | Same as U2 | | | | |
| | U10 | Same as U8 | | | | |
| | | EXTRACTOR, Hot Stamped A7 | 52542 | 03984207 | 03984207 | 1 |
| | | EXTRACTOR | 51495 | 1743 | 100865 | 1 |
| | | ROLL PIN | 73957 | 50-094-0250 | 100752 | 2 |
| | | BOARD, PC | 52542 | 057259 | 057259 | 1 |

## REPLACEABLE PARTS LIST

TITLE OPTION 05, A20 IEEE 488 I/O PC ASSEMBLY #05725401 (Figure 7-64 & 7-65)

| ITEM | REF | COMPONENT DESCRIPTION | MFR'S CODE | MANUFACTURER'S PART NUMBER | SD STOCK NUMBER | T/Q |
|---|---|---|---|---|---|---|
| | C1 | CAPACITOR, Tant<br>47 μF 10%, 20V | 56289 | 150D476X9020R2 | 100186 | 1 |
| | C2 | CAPACITOR, Tant<br>39 μF 10%, 10V | 56289 | 150D396X901B2 | 100183 | 1 |
| | C3 | CAPACITOR, Ceramic<br>.05 μF +80-20%, 10V | 71590 | UK10-503 | 100122 | 4 |
| | C4 | CAPACITOR, Ceramic<br>.001 μF 20%, 50V | 71590 | CW15C102M | 100251 | 1 |
| | C5 thru C7 | Same as C3 | | | | |
| | C8 | CAPACITOR, Ceramic DP<br>.01 μF 20%, 100V | 04222 | 3429100C103M | 117570 | 1 |
| | Q1 | TRANSISTOR, SINPN 15V | 07263 | PN3646 | 101369 | 1 |
| | R1 | RESISTOR, CC<br>6.2 k 5%, 1/4W | 01121 | CB6225 | 101608 | 4 |
| | R2 | RESISTOR, CC<br>3 k 5%, 1/4W | 01121 | CB3025 | 101548 | 4 |
| | R3 | RESISTOR, CC<br>12 k 5%, 1/4W | 01121 | CB1235 | 101565 | 2 |
| | R4 | RESISTOR, CC<br>47 k 5%, 1/4W | 01121 | CB4735 | 101574 | 1 |
| | R5 | RESISTOR, CC<br>22 k 5%, 1/4W | 01121 | CB2235 | 101572 | 2 |
| | R6 | Same as R3 | | | | |
| | R7 | Same as R2 | | | | |
| | R8 | Same as R1 | | | | |
| | R9 | Same as R2 | | | | |
| | R10 | Same as R1 | | | | |
| | R11 | Same as R2 | | | | |
| | R12 | Same as R1 | | | | |
| | R13 | Same as R5 | | | | |
| | U1 thru U3 | INTEGRATED CIRCUIT, TTL SSI<br>4 Bus Driver/Receiver | 04713 | MC3446P | 117021 | 3 |
| | U4 | INTEGRATED CIRCUIT, TTL SSI<br>Hex Inverter | 01295 | SN74LS04N | 103749 | 1 |
| | U5 | INTEGRATED CIRCUIT, TTL SSI<br>Hex S.I. Inverter | 01295 | SN74LS14N | 117083 | 1 |

## REPLACEABLE PARTS LIST

TITLE OPTION 05, A20 IEEE 488 I/O PC ASSEMBLY #05725401 (Cont'd)

| ITEM | REF | COMPONENT DESCRIPTION | MFR'S CODE | MANUFACTURER'S PART NUMBER | SD STOCK NUMBER | T/Q |
|---|---|---|---|---|---|---|
| | U6 thru U8 | INTEGRATED CIRCUIT, TTL SSI<br>Quad 8-Input NAND Gate | 01295 | SN74LS30N | 103971 | 3 |
| | U9 | INTEGRATED CIRCUIT, TTL SSI<br>5 Bit Comparator | 07263 | 93L24PC | 117020 | 1 |
| | U10 | INTEGRATED CIRCUIT, TTL SSI<br>Quad 2-Input Positive OR Gate | 01295 | SN74LS32N | 103972 | 1 |
| | U11 | INTEGRATED CIRCUIT, TTL SSI<br>Quad 2-Input NAND Gate | 01295 | SN74LS08N | 103967 | 2 |
| | U12 | INTEGRATED CIRCUIT, TTL SSI<br>Quad 2-Input NAND Gate | 01295 | SN74LS00N | 103130 | 2 |
| | U13 | Same as U11 | | | | |
| | U14 | Same as U12 | | | | |
| | U15 | INTEGRATED CIRCUIT, TTL SSI<br>Dual Retriggerable One Shot | 01295 | SN74LS123N | 103976 | 1 |
| | U16 | INTEGRATED CIRCUIT<br>Resistor Module 4-12k | 52542 | 045008 | 045008 | 1 |
| | | SPACER, Swage 6-32 x 1/4 | 88245 | 1530 B 1/4 | 100783 | 1 |
| | | BOARD, PC | 52542 | 057254 | 057254 | 1 |

## REPLACEABLE PARTS LIST

TITLE **OPTION 05, A21 SAMPLE RATE & CONTROL PC ASSEMBLY #05788601 Rev E (Figure 7-66 & 7-67)**

| ITEM | REF | COMPONENT DESCRIPTION | MFR'S CODE | MANUFACTURER'S PART NUMBER | SD STOCK NUMBER | T/Q |
|---|---|---|---|---|---|---|
| | C1 | CAPACITOR, Tant<br>4.7 µF 10%, 10V | 56289 | 150D475X9010A2 | 100205 | 1 |
| | C2 | CAPACITOR, Ceramic<br>.1 µF 20%, 50V | 56289 | 5C023104X0500C5 | 100178 | 1 |
| | C3 | CAPACITOR, Ceramic<br>.01 µF 20%, 50V | 71590 | CW15C102M | 100251 | 1 |
| | C4 | CAPACITOR, Ceramic<br>.05 µF +80-20%, 10V | 71590 | UK10-503 | 100122 | 1 |
| | Q1 | TRANSISTOR, SIPNP 40V | 04713 | 2N3906 | 101378 | 2 |
| | Q2 | Same as Q1 | | | | |
| | R1 | RESISTOR, CC<br>4.7 k 5%, 1/4W | 01121 | CB4725 | 101598 | 4 |
| | R2 | Same as R1 | | | | |
| | R3 | RESISTOR, CC<br>22 k 5%, 1/4W | 01121 | CB2235 | 101572 | 1 |
| | R4 | Same as R1 | | | | |
| | R5 | RESISTOR, CC<br>2.7 M 5%, 1/4W | 01121 | CB2755 | 101621 | 1 |
| | R6 | RESISTOR, CC<br>1 k 5%, 1/4W | 01121 | CB1025 | 101569 | 3 |
| | R7 | Same as R1 | | | | |
| | R8 | Same as R6 | | | | |
| | R9 | RESISTOR, CC<br>3.9 k 5%, 1/4W | 01121 | CB3925 | 101601 | 2 |
| | R10 | Same as R9 | | | | |
| | R11 | Same as R6 | | | | |
| | R12 | RESISTOR, CC<br>100 k 5%, 1/4W | 01121 | CB1045 | 101558 | 1 |
| | U1 | INTEGRATED CIRCUIT<br>Wide Range Timer | 18324 | NE555V | 045208 | 1 |
| | U2 | INTEGRATED CIRCUIT, TTL<br>Hex Inverter | 01295 | SN7416N | 045230 | 1 |
| | U3 | INTEGRATED CIRCUIT, TTL SSI<br>Quad 2-Input OR Gate | 01295 | SN7432N | 045257 | 1 |
| | U4 | INTEGRATED CIRCUIT, TTL<br>Monostable Retriggerable MV W/Clear | 01295 | SN74122N | 117392 | 1 |
| | | TERMINAL, Swage | 88245 | 2000B | 100482 | 9 |
| | | SPACER, Swage | 71279 | 1247-11 | 100539 | 2 |
| | | BOARD, PC | 52542 | 057886 | 057886 | 1 |

## REPLACEABLE PARTS LIST

TITLE OPTION 11 #05545201, OPTION 12 #05545202, OPTION 13 #05545203 Rev C (Figure 7-69)

| ITEM | REF | COMPONENT DESCRIPTION | MFR'S CODE | MANUFACTURER'S PART NUMBER | SD STOCK NUMBER | T/Q |
|---|---|---|---|---|---|---|
| | | **DELETE** | | | | |
| | | OSCILLATOR, Timebase PC Assembly | 52542 | 06738102 | 06738201 | 1 |
| | | PLATE, Oscillator Cover | 52542 | 055104 | 055104 | 1 |
| | | PLATE, Cover Transformer & Cap. | 52542 | 055435 | 055435 | 1 |
| | | SCREW, PHMS 6-32 x 5/8 | 96906 | MS51957-18 | 10063210 | 1 |
| | | SCREW, PHMS 6-32 x 1/4 | 96906 | MS51957-26 | 10063204 | 2 |
| | | SCREW, PHMS 6-32 x 5/16 | 96906 | MS51957-32 | 10063212 | 1 |
| | | SCREW, PHMS 4-40 x 1/4 | 96906 | MS51957-13 | 10062604 | 2 |
| | | WASHER, Split-Lock #6 | 96906 | MS35338-136 | 100712 | 4 |
| | | WASHER, Flat #6 | 86928 | 5710-23-10 | 100662 | 1 |
| | | WASHER, Split-Lock #4 | 96906 | MS35338-135 | 100711 | 2 |
| | | NUT, Kep 6-32 | 78189 | 511-061800-01 | 112472 | 2 |
| | | **ADD** | | | | |
| 20 | A26 | ASSEMBLY, H.S. Oscillator Opt. 11 | 52542 | 03342801 | 03342801 | 1 |
| 20 | A26 | ASSEMBLY, H.S. Oscillator Opt. 12 | 52542 | 03342701 | 03342701 | 1 |
| 20 | A26 | ASSEMBLY, H.S. Oscillator Opt. 13 | 52542 | 03342901 | 03342901 | 1 |
| 21 | T2 | TRANSFORMER | 52542 | 019805 | 019805 | 1 |
| 22 | C5 | CAPACITOR, Elect. 500 $\mu$F 50V | 56289 | D45510 | 102592 | 1 |
| 23 | U3 | INTEGRATED CIRCUIT, Voltage Reg. | 04713 | MC7815CT | 103039 | 1 |
| 24 | | SCREW, PHMS 6-32 x 5/16 | 96906 | MS51957-27 | 10063205 | 3 |
| 25 | | SCREW, PHMS 4-40 x 1/4 | 96906 | MS51957-13 | 10062604 | 1 |
| 26 | | SCREW, PHMS 4-40 x 1 | 96906 | MS51957-21 | 10062616 | 2 |
| 27 | | WASHER, Flat #6 | 86928 | 5710-23-10 | 100662 | 1 |
| 28 | | WASHER, Split-Lock #6 | 96906 | MS35338-136 | 100712 | 4 |
| 29 | | WASHER, Flat #4 | 96906 | MS15795-803 | 100703 | 3 |
| 30 | | WASHER, Split-Lock #4 | 96906 | MS35338-135 | 100711 | 3 |
| 33 | | SHIELD, Fan | 52542 | 067502 | 067502 | 1 |
| 35 | | SCREW, PHMS 6-32 x 1/2 | 96906 | MS51957-45 | 10063208 | 1 |

## REPLACEABLE PARTS LIST

| TITLE | OPTION 18, 18 GHz OPERATION #057549 Rev A | | | | | |
|---|---|---|---|---|---|---|
| ITEM | REF | COMPONENT DESCRIPTION | MFR'S CODE | MANUFACTURER'S PART NUMBER | SD STOCK NUMBER | T/Q |
| | | **DELETE** | | | | |
| | J1 | CONNECTOR, SMA Coaxial | 16179 | OSM208ASF | 103934 | 1 |
| | | PANEL, Decorative | 52542 | 055686 | 055686 | 1 |
| | | **ADD** | | | | |
| | J1 | CONNECTOR, Type N (P/O Front Panel) | 16179 | 21011 | 101185 | 1 |
| | | PANEL, Decorative | 52542 | 053426 | 053426 | 1 |
| | | SCREW, FHMS 4-40 x 5/16 | 96906 | MS24693-C3 | 10072005 | 4 |
| | | NUT, Kep 4-40 | 78189 | 511-041800-00 | 100941 | 4 |

## REPLACEABLE PARTS LIST

TITLE OPTION 20 REAR INPUT ASSEMBLY #057379 Rev A (Figure 7-70)

| ITEM | REF | COMPONENT DESCRIPTION | MFR'S CODE | MANUFACTURER'S PART NUMBER | SD STOCK NUMBER | T/Q |
|---|---|---|---|---|---|---|
| | | **DELETE** | | | | |
| | | PLATE, Rear Input Cover | 52542 | 055018 | 055018 | 1 |
| | | CABLE, Semi-Rigit Coaxial | 52542 | 055211 | 055221 | 1 |
| | | SCREW, FHMS 4-40 x 5/16 | 96906 | MS24693-C3 | 10072005 | 4 |
| | | SCREW, PHMS 4-40 x 1/4 | 96906 | MS51957-13 | 10062604 | 2 |
| | | SCREW, PHMS 6-32 x 5/16 | 96906 | MS51957-27 | 10063205 | 2 |
| | | NUT, Kep 4-40 | 78189 | 511-041800-00 | 100741 | 6 |
| | | **ADD** | | | | |
| 15 | | CABLE, Semi-Rigid Coaxial | 52542 | 055696 | 055696 | 1 |
| 16 | | ASSEMBLY, Coaxial Cable w/connectors | 52542 | 055742 | 055742 | 1 |
| 19 | | BRACKET, Connector Mtg. T | 52542 | 055691 | 055691 | 1 |
| 20 | | ASSEMBLY, Coaxial Cable | 52542 | 055357 | 055357 | 1 |
| 21 | | CONNECTOR, T | 98291 | 51-083-0000 | 103759 | 1 |
| 22 | | TERMINATION, BNC 50 Ω | 96906 | MX-554A/U-512 | 102302 | 1 |
| 23 | | PLATE, Rear Adapter | 52542 | 057377 | 057377 | 1 |
| 24 | | PLATE, 5/16 Dia. Hole | 52542 | 117067 | 117067 | 1 |
| 26 | | SCREW, PHMS 6-32 x 7/16 | 96906 | MS51957-29 | 10063207 | 2 |
| 27 | | SCREW, PHMS 4-40 x 1/4 | 96906 | MS51957-13 | 10062604 | 4 |
| 28 | | WASHER, Split-Lock #6 | 96906 | MS35338-136 | 100712 | 2 |
| 29 | | NUT, Kep 4-40 | 78189 | 511-041800-00 | 100941 | 4 |
| 30 | | WASHER, Flat #6 | 96906 | MS15795-805 | 100704 | 2 |
| 31 | | TIE, Cable | 06383 | SSTIM | 100753 | A/R |

## REPLACEABLE PARTS LIST

| TITLE | OPTION 27, 50-60/400 Hz OPERATION ASSEMBLY #055515 Rev $A_2$ (Figure 7-71) | | | | | |
|---|---|---|---|---|---|---|
| **ITEM** | **REF** | **COMPONENT DESCRIPTION** | **MFR'S CODE** | **MANUFACTURER'S PART NUMBER** | **SD STOCK NUMBER** | **T/Q** |
| | | **DELETE** | | | | |
| 7 | B1 | BLOWER, 50-60 Hz | 23936 | 8500 | 100887 | 1 |
| | | **ADD** | | | | |
| 14 | B100 | BLOWER, 50-400 Hz | 92702 | PBC2206F-2-1 | 100037 | 1 |
| 16 | C100 | CAPACITOR, .5 $\mu$F 600V Bathtub | 14655 | MYRT6050 | 100353 | 1 |
| 18 | | CONNECTOR, Male Pin | 27264 | 02-06-2103 | 10282202 | 2 |
| 21 | | SCREW, FHMS 6-32 x 5/16 | 96906 | MS24693-C25 | 10073105 | 2 |
| 23 | | WASHER, Split-Lock #6 | 96906 | MS35338-136 | 100712 | 2 |
| 24 | | NUT, Hex 6-32 | 96906 | MS35649-264 | 100706 | 2 |
| 26 | | CLAMP, Cable 1/8 | 95987 | 1/8J | 100754 | 1 |

## REPLACEABLE PARTS LIST

**TITLE** OPTION 28, IF OFFSET ASSEMBLY #057674 (Figure 7-72)

| ITEM | REF | COMPONENT DESCRIPTION | MFR'S CODE | MANUFACTURER'S PART NUMBER | SD STOCK NUMBER | T/Q |
|---|---|---|---|---|---|---|
| | | **DELETE** | | | | |
| | | PLATE, Cover (P/O Rear Panel) | 52542 | 055229 | 055229 | 1 |
| | | **ADD** | | | | |
| 16 | A7 | ASSEMBLY, Offset PC | 52542 | 057259XX | 057259XX | 1 |
| 20 | J2 | CONNECTOR, Female 36-pin | 02660 | 57-40360 | 101176 | 1 |
| 21 | | CONNECTOR, Male 36-pin | 02660 | 57-30360 | 101158 | 1 |
| 3 | | ASSEMBLY, Rear Panel Test | 52542 | | | Ref |

# REPLACEABLE PARTS LIST

TITLE OPTION 28, A7 OFFSET PC ASSEMBLY #057259XX (Figure 7-73 & 7-74)

| ITEM | REF | COMPONENT DESCRIPTION | MFR'S CODE | MANUFACTURER'S PART NUMBER | SD STOCK NUMBER | T/Q |
|---|---|---|---|---|---|---|
| | C11 | CAPACITOR, Tant<br>39 μF 10%, 10V | 56289 | 150D396X9010B2 | 100183 | 1 |
| | C12 | CAPACITOR, Ceramic<br>.05 μF 10%, 10V | 71590 | UK10-503 | 100122 | 2 |
| | C13 | Same as C11 | | | | |
| | U11 | INTEGRATED CIRCUIT, TTL SSI<br>Quad 2-Input NAND Gate | 01295 | SN74LS08N | 103967 | 1 |
| | U12<br>thru<br>U15 | Programmed IC factory select<br>by specific offset. | 52542 | | | 4 |
| | U18<br>thru<br>U26 | INTEGRATED CIRCUIT<br>Resistor Network 4 x 12k | 52542 | 045008 | 045008 | 9 |
| | XU12<br>thru<br>XU15 | SOCKET, IC 16-pin | 73803 | C83-16-02 | 117041 | 4 |
| | | EXTRACTOR, Hot Stamped A7 | 52542 | 03984207 | 03984207 | 1 |
| | | EXTRACTOR | 51495 | 1743 | 100865 | 1 |
| | | ROLL PIN | 73957 | 50-094-0250 | 100752 | 2 |
| | | BOARD, PC | 52542 | 057259 | 057259 | 1 |

# CHAPTER 7

# DRAWINGS

## 7-1 INTRODUCTION

This chapter contains final assembly and schematic drawings for the Model 6054B Frequency Counter. The schematic diagrams relate to the detailed circuit descriptions located in Chapter 4 of this manual. The parts list contained in Chapter 6 relate to the reference designation callouts on the diagrams. Table 7-1 provides a list by figure number of the drawings, with title, drawing number and manual page number.

### TABLE 7-1 LIST OF DRAWINGS

| Figure No. | Drawing Title | Drawing No. | Page No. |
|---|---|---|---|
| 7-1 | Model 6054B Block Diagram | 057087 | 7-3 |
| 7-2 | A1, Decade MSD PC Assembly | 05394301 | 7-4 |
| 7-3 | A1, Decade MSD Schematic | 7-05394301 | 7-5 |
| 7-4 | A3, Decade LSD PC Assembly | 05394401 | 7-6 |
| 7-5 | A3, Decade LSD Schematic | 7-05394401 | 7-7 |
| 7-6 | A4, 500 MHz Decade & Gate PC Assembly | 05331301 | 7-8 |
| 7-7 | A4, 500 MHz Decade & Gate Schematic | 7-05331301 | 7-9 |
| 7-8 | A6, IF Integrator PC Assembly | 05336901 | 7-10 |
| 7-9 | A6, IF Integrator Schematic | 7-05336901 | 7-11 |
| 7-10 | A8, Timebase PC Assembly | 05337901 | 7-12 |
| 7-11 | A8, Timebase Schematic | 7-05337901 | 7-13 |
| 7-12 | A9, 10 kHz Generator PC Assembly | 05334201 | 7-14 |
| 7-13 | A9, 10 kHz Generator Schematic | 7-05334201 | 7-15 |
| 7-14 | A10, N Computer PC Assembly | 05736401 | 7-16 |
| 7-15 | A10, N Computer Schematic | 7-05736401 | 7-17 |
| 7-16 | A11, Function PC Assembly | 05338601 | 7-18 |
| 7-17 | A11, Function Schematic | 7-05338601 | 7-19 |
| 7-18 | A12, 20 MHz Amplifier PC Assembly | 05341201 | 7-20 |
| 7-19 | A12, 20 MHz Amplifier Schematic | 7-05341201 | 7-21 |
| 7-20 | A13, Display PC Assembly | 05326301 | 7-22 |
| 7-21 | A13, Display Schematic | 7-05326301 | 7-23 |
| 7-22 | A14, N IF ACTO Module Assembly | 055369 | 7-24 |
| 7-23 | A14, N IF PC Assembly | 05324601 | 7-24 |
| 7-24 | A14, N IF Schematic | 7-05324601 | 7-25 |
| 7-25 | A15, Search Oscillator ACTO Module Assemhbly | 055370 | 7-26 |
| 7-26 | A15, Search Oscillator PC Assembly | 05322801 | 7-26 |
| 7-27 | A15, Search Oscillator Schematic | 7-05322801 | 7-27 |
| 7-28 | A16, LO/Shifter ACTO Module Assembly | 057167 | 7-28 |
| 7-29 | A16, LO/Shifter PC Assembly | 05710401 | 7-28 |
| 7-30 | A16, LO/Shifter Schematic | 7-05710401 | 7-29 |
| 7-31 | A17, Lock IF ACTO Module Assembly | 055367 | 7-30 |
| 7-32 | A17, Lock IF PC Assembly | 05321801 | 7-30 |
| 7-33 | A17, Lock IF Schematic | 7-05321801 | 7-31 |

TABLE 7-1 LIST OF DRAWINGS (Cont'd)

| Figure No. | Drawing Title | Drawing No. | Page No. |
|---|---|---|---|
| 7-34 | A22, 500 MHz Pre Amp PC Assembly | 06748401 | 7-32 |
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| 7-36 | Transformer Chassis Assembly | 055116 | 7-33 |
| 7-37 | Time Base Oscillator PC Assembly | 06738201 | 7-33 |
| 7-38 | Diode Assembly | 05389001 | 7-34 |
| 7-39 | Counter PS Regulator Assembly | 05394101 | 7-34 |
| 7-40 | ACTO PS Regulator Assembly | 05393301 | 7-34 |
| 7-41 | Power Supply Schematic | 7-055122 | 7-35 |
| 7-42 | Test Assembly Model 6054B (2 sheets) | 057164 | 7-36 |
| 7-43 | Universal Chassis Assembly (2 sheets) | 057496 | 7-38 |
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| 7-46 | Front Panel Assembly | 057162 | 7-42 |
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| 7-49 | Option 04, BCD Remote Cable Assembly | 055499 | 7-45 |
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| 7-51 | Option 04, A2 BCD Output PC Assembly | 05344604 | 7-46 |
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| 7-53 | Option 04, A5 Remote PC Assembly | 05339001 | 7-48 |
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| 7-58 | Option 05, A2 IEEE 488 BCD Out PC Assembly | 05725701 | 7-54 |
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| 7-60 | Option 05, A5 IEEE 488 Programming PC Assembly | 05725601 | 7-56 |
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| 7-64 | Option 05, A20 IEEE 488 I/O PC Assembly | 05725401 | 7-60 |
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| 7-66 | Option 05, A21 Sample Rate & Control PC Assembly | 05788601 | 7-62 |
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| 7-69 | Option 11, 12 and 13 Assembly | 055452 | 7-65 |
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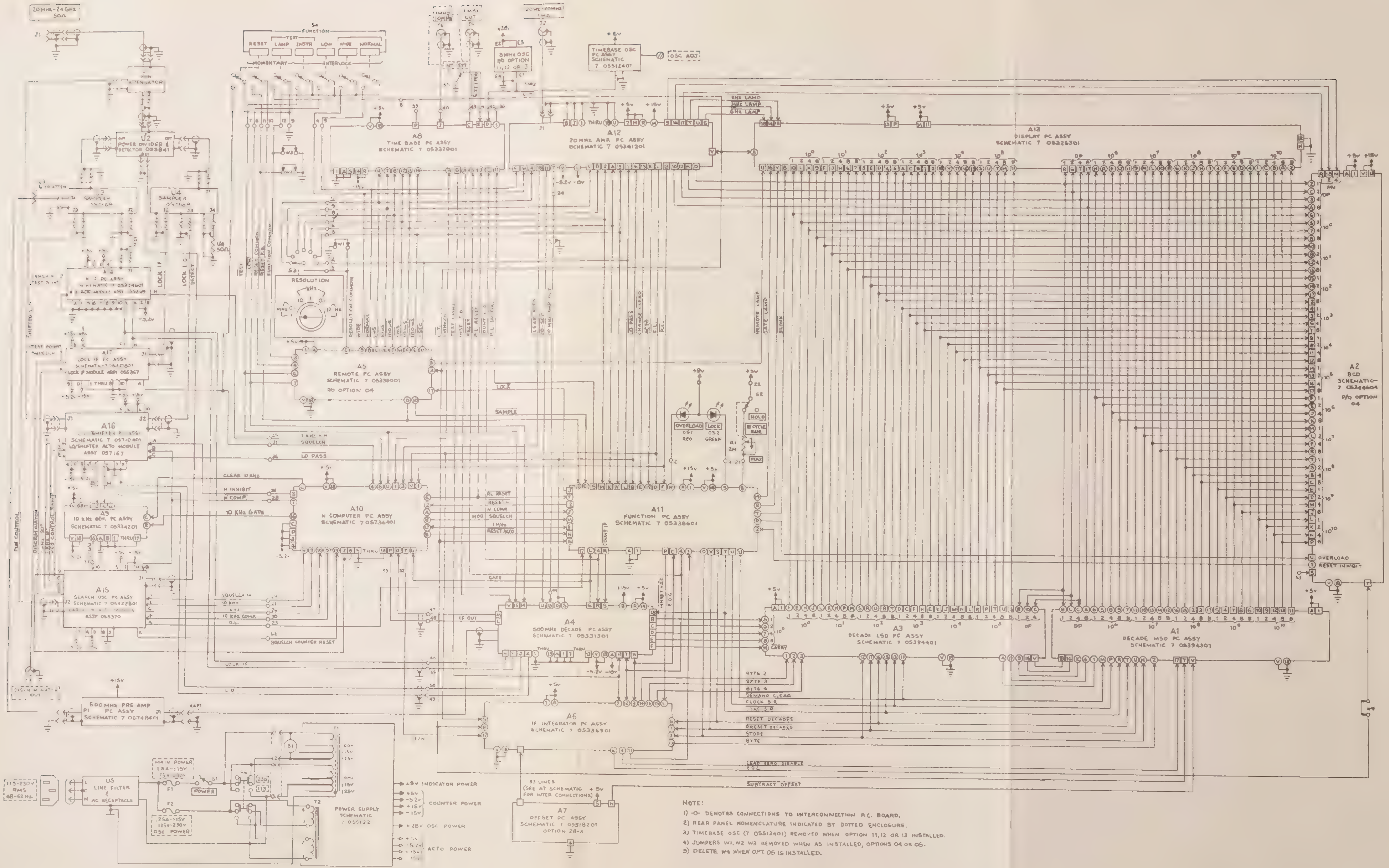
| 7-71 | Option 27, 50-60/400 Hz Operation | 055515 | 7-67 |
| 7-72 | Option 28, Offset Final Assembly | 057674 | 7-68 |
| 7-73 | Option 28, A7 Offset PC Assembly | 057259 | 7-68 |
| 7-74 | Option 28, A7 Offset Schematic | 7-057259 | 7-69 |
| 7-75 | ACTO Extender Assembly | 05502801 | 7-70 |
| 7-76 | Digital Extender Assembly | 05502901 | 7-70 |


20 MHz-24 GHz 50Ω
J1
ATTENUATOR
S4 FUNCTION
TEST
RESET
LAMP
INSTR
LOW
WIDE
NORMAL
MOMENTARY
INTERLOCK
U2 POWER DIVIDER & DETECTOR 055841
U3 SAMPLER
U4 SAMPLER
U4 50Ω
A14
A17 LOCK IF PC ASSY
A16 SHIFTER PC ASSY
A9 10 KHz GEN. PC ASSY SCHEMATIC 7 05334201
A15 SEARCH OSC PC ASSY SCHEMATIC 7 05322801
500 MHz PRE AMP PC ASSY SCHEMATIC 7 0674840
A4P1
8 MHz OSC P/O OPTION 11, 12 OR 13
TIMEBASE OSC PC ASSY SCHEMATIC 7 05512401
OSC ADJ
A8 TIME BASE PC ASSY SCHEMATIC 7 05337001
A12 20 MHz AMP PC ASSY SCHEMATIC 7 05341201
KHz LAMP
MHz LAMP
GHz LAMP
A13 DISPLAY PC ASSY SCHEMATIC 7 05326301
RESOLUTION
S3
A5 REMOTE PC ASSY SCHEMATIC 7 05338001 P/O OPTION 04
LOCK
SAMPLE
OVERLOAD DS1 RED
LOCK DS2 GREEN
HOLD
RECYCLE RATE
MAX
R1 2M
S2
A10 N COMPUTER PC ASSY SCHEMATIC 7 05736401
A11 FUNCTION PC ASSY SCHEMATIC 7 05338601
CLEAR 10 KHz
N INHIBIT
N COMP.
10 KHz GATE
LO PASS
SQUELCH
GATE
IF OUT
LOCK IF
LO
A4 500 MHz DECADE PC ASSY SCHEMATIC 7 05331301
A3 DECADE LSD PC ASSY SCHEMATIC 7 05394401
A1 DECADE MSD PC ASSY SCHEMATIC 7 05394301
A2 BCD SCHEMATIC 7 05344604 P/O OPTION 04
OVERLOAD
RESET INHIBIT
A6 IF INTEGRATOR PC ASSY SCHEMATIC 7 05336901
BYTE 2
BYTE 3
BYTE 4
DEMAND CLEAR
CLOCK S.R.
RESET DECADES
PRESET DECADES
STORE
BYTE
LEAD ZERO DISABLE
EOC
SUBTRACT OFFSET
115-230V RMS 48-62 Hz
U5 LINE FILTER & AC RECEPTACLE
MAIN POWER
F1
F2
POWER
OSC POWER
T1
T2
POWER SUPPLY SCHEMATIC 7 055122
+9V INDICATOR POWER
COUNTER POWER
+28V OSC POWER
ACTO POWER
33 LINES (SEE A7 SCHEMATIC FOR INTER CONNECTIONS)
A7 OFFSET PC ASSY SCHEMATIC 7 05518201 OPTION 28-A
S4

NOTE:

1) -○- DENOTES CONNECTIONS TO INTERCONNECTION P.C. BOARD.
2) REAR PANEL NOMENCLATURE INDICATED BY DOTTED ENCLOSURE.
3) TIMEBASE OSC (7 05512401) REMOVED WHEN OPTION 11, 12 OR 13 INSTALLED.
4) JUMPERS W1, W2 W3 REMOVED WHEN A5 INSTALLED, OPTIONS 04 OR 05.
5) DELETE W4 WHEN OPT. 05 IS INSTALLED.

FIGURE 7-1
MODEL 6054B BLOCK DIAGRAM
SCHEMATIC #7-057087 Rev G

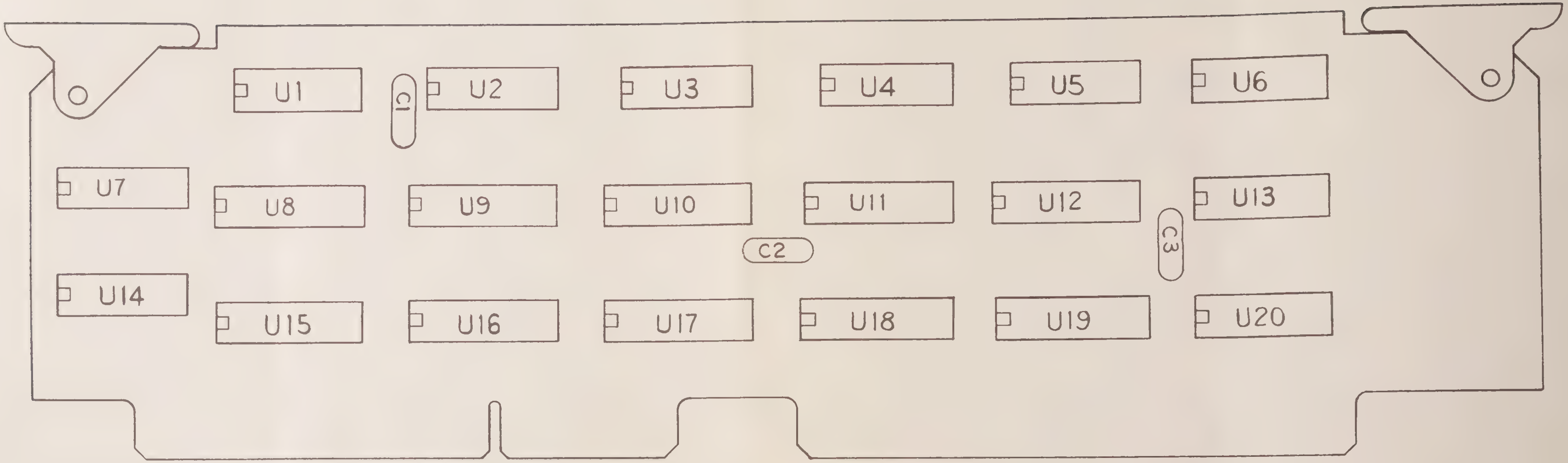

U1
C1
U2
U3
U4
U5
U6
U7
U8
U9
U10
U11
U12
U13
C2
C3
U14
U15
U16
U17
U18
U19
U20

FIGURE 7-2
A1, DECADE MSD PC ASSEMBLY
#05394301 Rev $A_1$

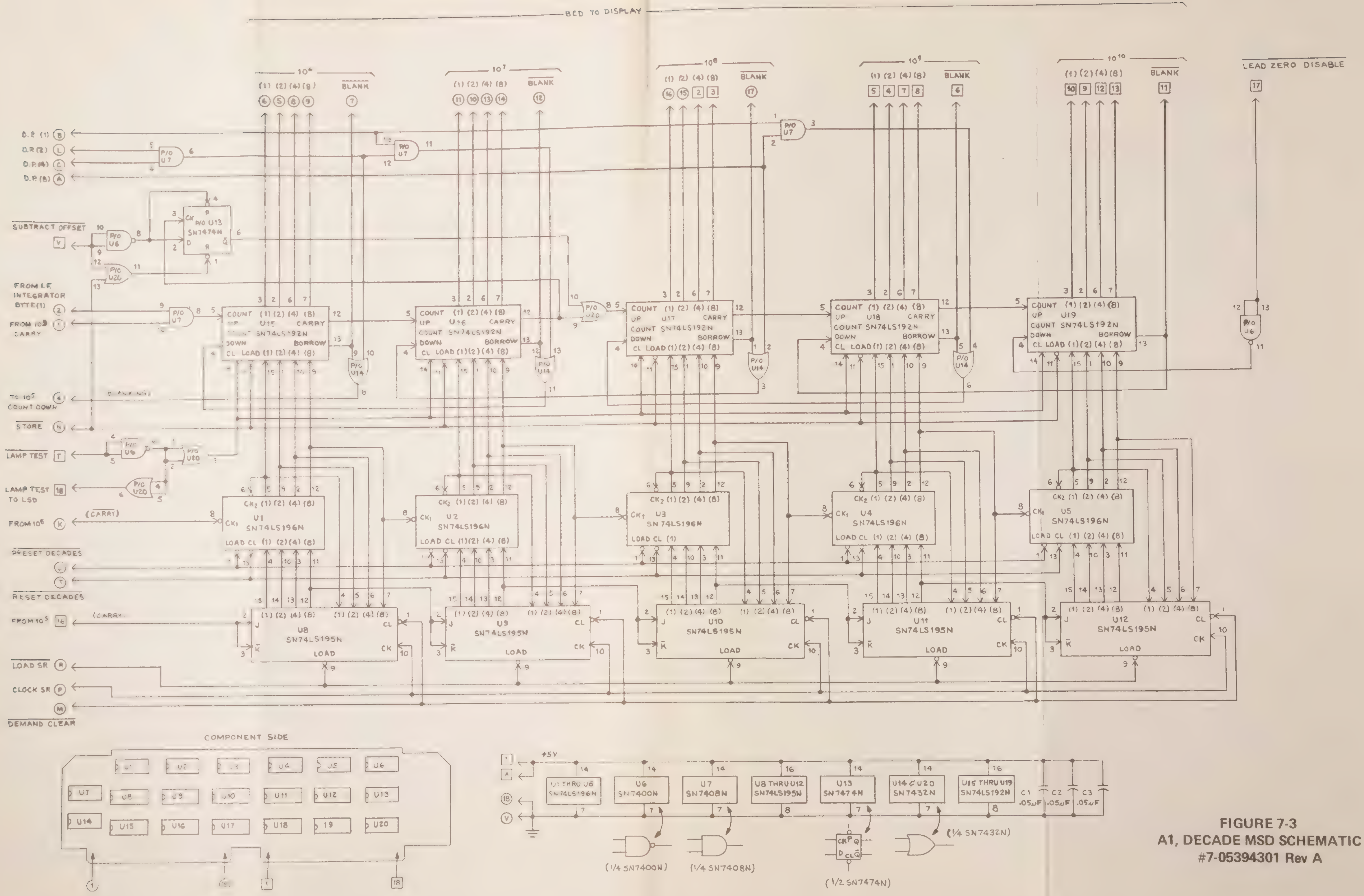

BCD TO DISPLAY
$10^6$
$10^7$
$10^8$
$10^9$
$10^{10}$
(1) (2) (4) (8)
BLANK
LEAD ZERO DISABLE
D.P. (1)
D.P. (2)
D.P. (4)
D.P. (8)
SUBTRACT OFFSET
FROM I.F. INTEGRATOR BYTE (1)
FROM $10^5$ CARRY
TO $10^5$ COUNT DOWN
BLANKING
STORE
LAMP TEST
LAMP TEST TO LSD
FROM $10^6$
(CARRY)
PRESET DECADES
RESET DECADES
FROM $10^5$
LOAD SR
CLOCK SR
DEMAND CLEAR
P/O U6
P/O U7
P/O U13 SN7474N
P/O U14
P/O U20
COUNT UP
COUNT DOWN
CARRY
BORROW
CL LOAD (1) (2) (4) (8)
U15 SN74LS192N
U16 SN74LS192N
U17 SN74LS192N
U18 SN74LS192N
U19 SN74LS192N
$CK_2$ (1) (2) (4) (8)
$CK_1$
U1 SN74LS196N
U2 SN74LS196N
U3 SN74LS196N
U4 SN74LS196N
U5 SN74LS196N
LOAD CL (1) (2) (4) (8)
U8 SN74LS195N
U9 SN74LS195N
U10 SN74LS195N
U11 SN74LS195N
U12 SN74LS195N
J
K̄
CL
CK
LOAD
COMPONENT SIDE
U1 U2 U3 U4 U5 U6
U7 U8 U9 U10 U11 U12 U13
U14 U15 U16 U17 U18 U19 U20
+5V
U1 THRU U5 SN74LS196N
U6 SN7400N
U7 SN7408N
U8 THRU U12 SN74LS195N
U13 SN7474N
U14 & U20 SN7432N
U15 THRU U19 SN74LS192N
C1 .05μF
C2 .05μF
C3 .05μF
(1/4 SN7400N)
(1/4 SN7408N)
(1/2 SN7474N)
(1/4 SN7432N)
CK P Q
D CL Q̄

FIGURE 7-3
A1, DECADE MSD SCHEMATIC
#7-05394301 Rev A

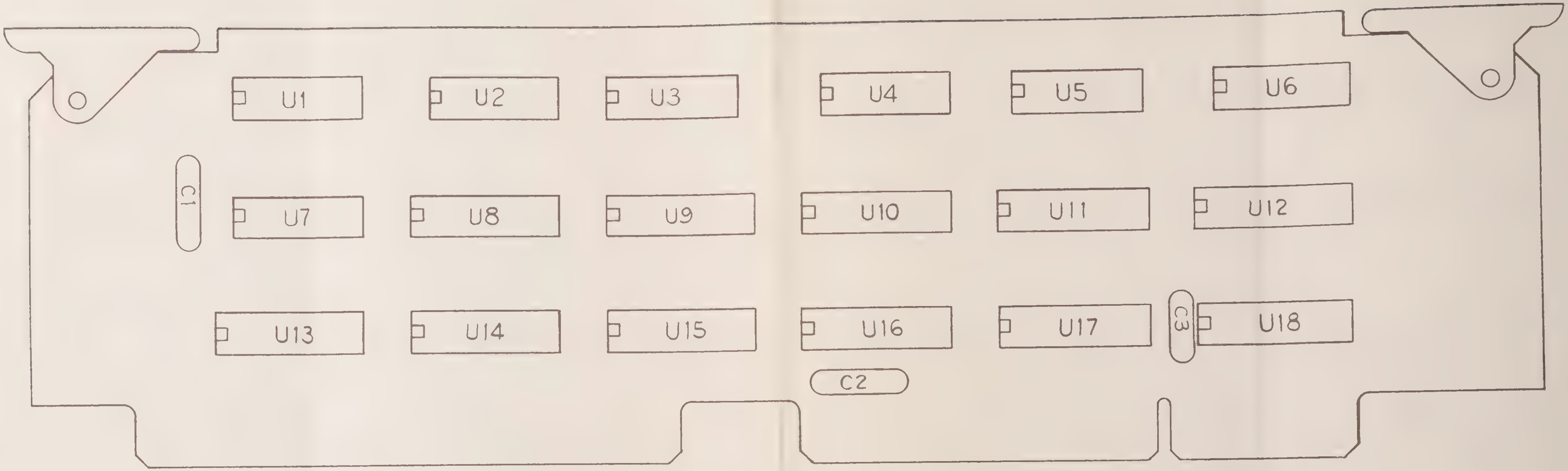

U1
U2
U3
U4
U5
U6
C1
U7
U8
U9
U10
U11
U12
U13
U14
U15
U16
U17
C3
U18
C2

FIGURE 7-4
A3, DECADE LSD PC ASSEMBLY
#05394401 Rev $A_1$

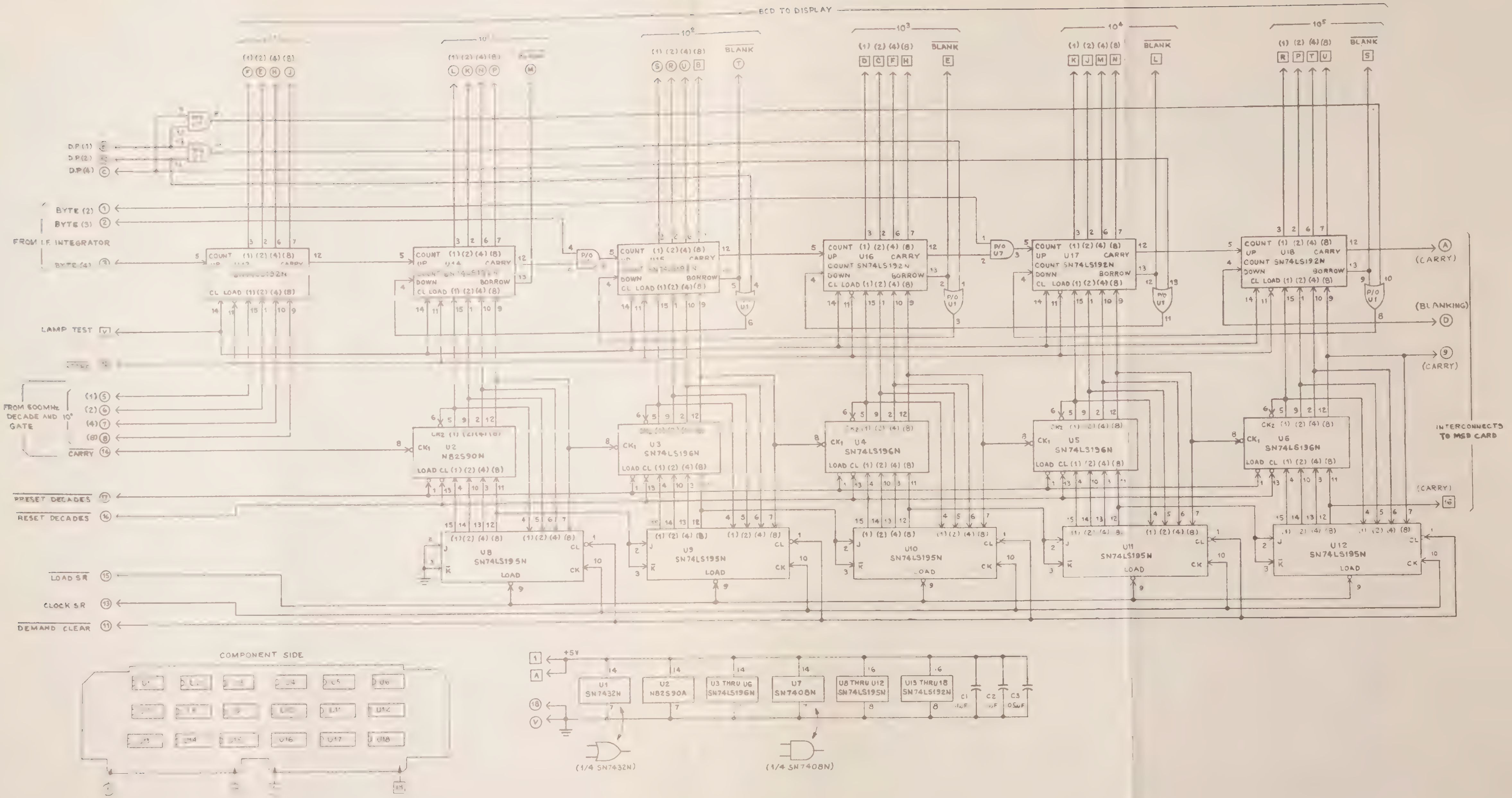

BCD TO DISPLAY
10¹
10²
10³
10⁴
10⁵
(1) (2) (4) (8)
BLANK
D.P.(1)
D.P.(2)
D.P.(4)
BYTE (2)
BYTE (3)
BYTE (4)
FROM I.F. INTEGRATOR
LAMP TEST
FROM 600MHz DECADE AND 10⁹ GATE
CARRY
PRESET DECADES
RESET DECADES
LOAD SR
CLOCK SR
DEMAND CLEAR
COUNT UP
COUNT DOWN
CARRY
BORROW
CL LOAD (1) (2) (4) (8)
U13
U14
U15
U16 SN74LS192N
U17 SN74LS192N
U18 SN74LS192N
P/O U7
P/O U1
CK₁ U2 N82S90N
CK₁ U3 SN74LS196N
CK₁ U4 SN74LS196N
CK₁ U5 SN74LS196N
CK₁ U6 SN74LS196N
LOAD CL (1) (2) (4) (8)
U8 SN74LS195N
U9 SN74LS195N
U10 SN74LS195N
U11 SN74LS195N
U12 SN74LS195N
J
K
CL
CK
LOAD
(CARRY)
(BLANKING)
INTERCONNECTS TO MSD CARD
COMPONENT SIDE
+5V
U1 SN7432N
U2 N82S90A
U3 THRU U6 SN74LS196N
U7 SN7408N
U8 THRU U12 SN74LS195N
U13 THRU 18 SN74LS192N
C1 .1μF
C2 .1μF
C3 .05μF
(1/4 SN7432N)
(1/4 SN7408N)

FIGURE 7-5
A3, DECADE LSD SCHEMATIC
#7-05394401 Rev A

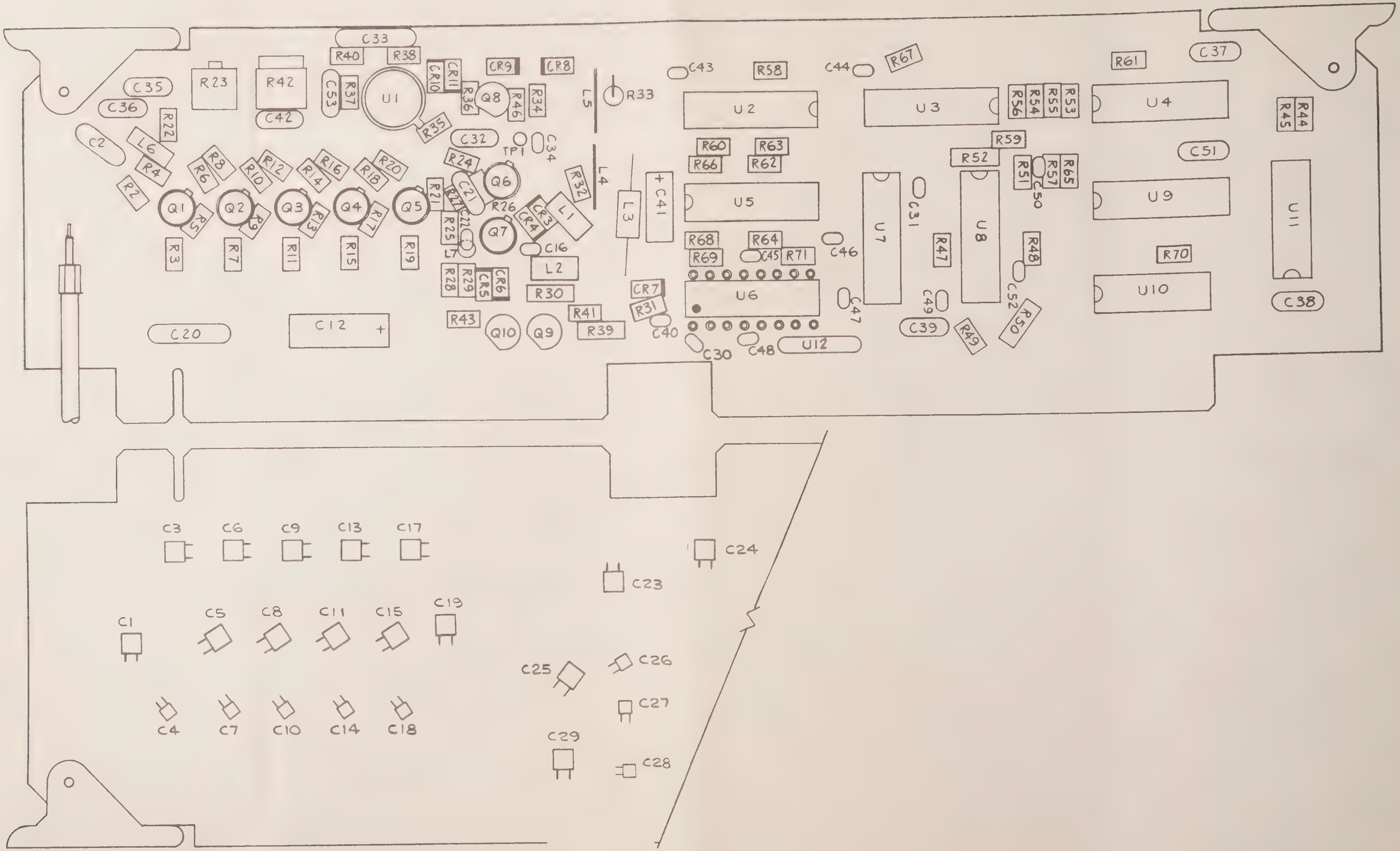
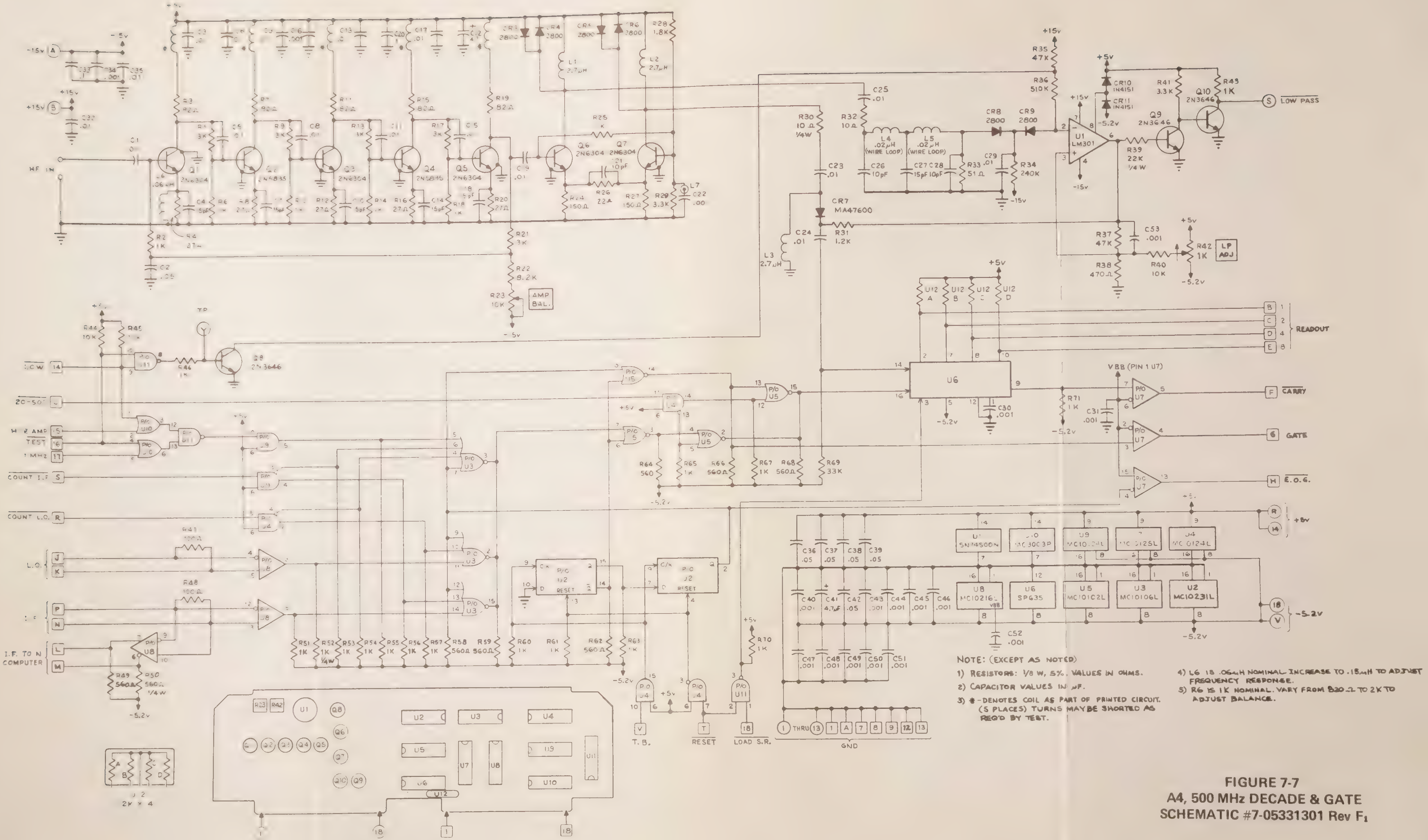

C33
R40
R38
R23
R42
C53
R37
U1
CR10
CR11
CR9
CR8
R36
Q8
R46
R34
L5
R33
C43
R58
C44
R67
R61
C37
C35
C36
C42
R35
C32
TP1
C34
U2
U3
R56
R54
R55
R53
U4
R45
R44
R22
C2
L6
R4
R2
R8
R6
R10
R12
R14
R16
R18
R20
R24
Q6
R21
R27
C21
R26
R32
L4
L1
CR3
CR4
Q1
Q2
Q3
Q4
Q5
R5
R9
R13
R17
R25
C22
Q7
C16
L7
L3
C41
R60
R63
R66
R62
U5
R59
R52
R51
R57
R65
C50
C51
U9
U7
C31
U8
U11
R3
R7
R11
R15
R19
R28
R29
CR5
CR6
L2
R30
R68
R64
R69
C45
R71
C46
R47
R48
R70
CR7
U6
R31
C47
C49
C52
U10
C38
R43
Q10
Q9
R41
R39
C40
C30
C48
U12
C39
R49
R50
C20
C12
C3
C6
C9
C13
C17
C24
C23
C1
C5
C8
C11
C15
C19
C25
C26
C27
C4
C7
C10
C14
C18
C29
C28

FIGURE 7-6
A4, 500 MHz DECADE & GATE PC ASSEMBLY
#05331301 Rev E


-15v A
+15v B
HF IN
Q1 2N6304
Q2 2N5835
Q3 2N6304
Q4 2N5835
Q5 2N6304
Q6 2N6304
Q7 2N6304
CR3 2800
CR4 2800
CR5 2800
CR6 2800
L1 2.7µH
L2 2.7µH
R28 1.8K
R25 1K
R29 3.3K
L7
C22 .001
R21 3K
R22 8.2K
R23 10K
AMP BAL.
-5v
+15v
R35 47K
R36 510K
C25 .01
R30 10Ω 1/4W
R32 10Ω
L4 .02µH (WIRE LOOP)
L5 .02µH (WIRE LOOP)
C26 10pF
C27 15pF
C28 10pF
R33 51Ω
C29 .01
R34 240K
-15v
CR8 2800
CR9 2800
U1 LM301
+5v
CR10 1N4151
CR11 1N4151
-5.2v
R41 3.3K
R45 1K
Q9 2N3646
Q10 2N3646
R39 22K 1/4W
S LOW PASS
C23 .01
CR7 MA47600
C24 .01
L3 2.7µH
R31 1.2K
R37 47K
C53 .001
R38 470Ω
R40 10K
R42 1K
LP ADJ
R44 10K
R46 1K
TP
Q8 2N3646
LCW 14
20-50 U
HI Z AMP 15
TEST 16
1 MHZ 17
COUNT I.F S
COUNT L.O. R
L.O. J K
I.F. P N
I.F. TO N COMPUTER L M
R47 100Ω
R48 100Ω
R49 560Ω
R50 560Ω 1/4W
U12 A
U12 B
U12 C
U12 D
U6
C30 .001
B 1
C 2
D 4
E 8
READOUT
VBB (PIN 1 U7)
R71 1K
C31 .001
F CARRY
G GATE
H E.O.G.
R64 560
R65 1K
R66 560Ω
R67 1K
R68 560Ω
R69 33K
R51 1K
R52 1K 1/4W
R53 1K
R54 1K
R55 1K
R56 1K
R57 1K
R58 560Ω
R59 560Ω
R60 1K
R61 1K
R62 560Ω
R63 1K
R70 1K
P/O U2 RESET
V T.B.
T RESET
18 LOAD S.R.
R 14 +5v
U11 SN74S00N
U10 MC10H03P
U9 MC10124L
U7 MC10125L
U4 MC10124L
U8 MC10216L
U6 SP635
U5 MC10102L
U3 MC10106L
U2 MC10231L
C36 .05
C37 .05
C38 .05
C39 .05
C40 .001
C41 4.7µF
C42 .05
C43 .001
C44 .001
C45 .001
C46 .001
C47 .001
C48 .001
C49 .001
C50 .001
C51 .001
C52 .001
18 V -5.2v
1 THRU 13 1 A 7 8 9 12 13
GND
U12 2K x 4

NOTE: (EXCEPT AS NOTED)

1) RESISTORS: 1/8 W, 5%, VALUES IN OHMS.
2) CAPACITOR VALUES IN µF.
3) * -DENOTES COIL AS PART OF PRINTED CIRCUIT. (5 PLACES) TURNS MAYBE SHORTED AS REQ'D BY TEST.
4) L6 IS .06µH NOMINAL INCREASE TO .15µH TO ADJUST FREQUENCY RESPONSE.
5) R6 IS 1K NOMINAL. VARY FROM 820Ω TO 2K TO ADJUST BALANCE.

FIGURE 7-7
A4, 500 MHz DECADE & GATE
SCHEMATIC #7-05331301 Rev F₁

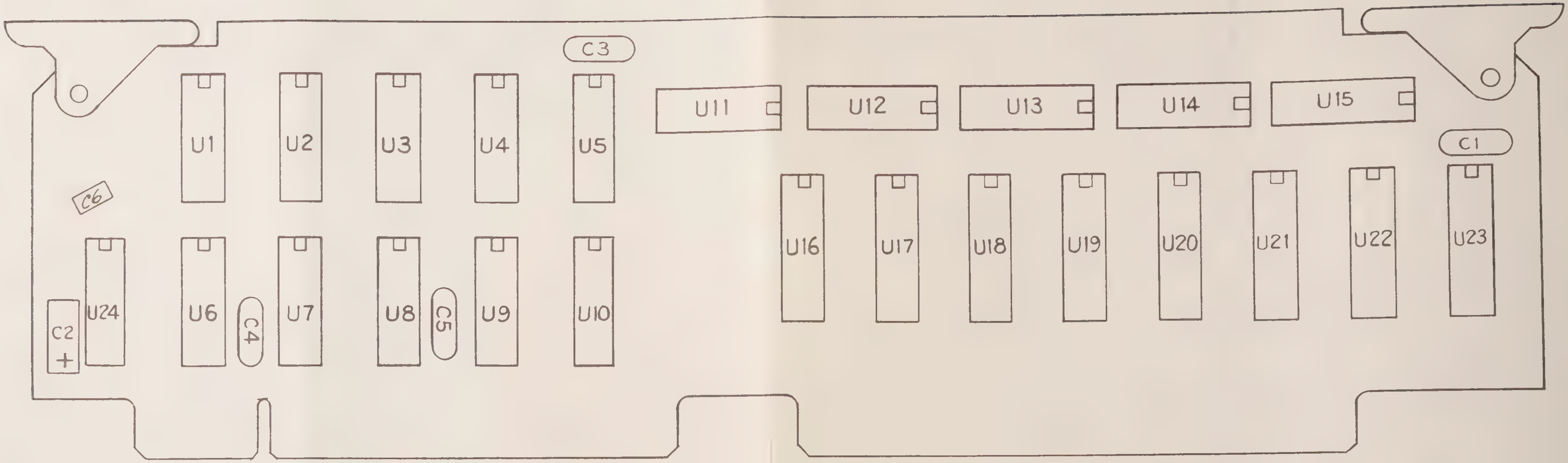

C3
U1
U2
U3
U4
U5
U11
U12
U13
U14
U15
C1
C6
U16
U17
U18
U19
U20
U21
U22
U23
U24
C2
+
U6
C4
U7
U8
C5
U9
U10

FIGURE 7-8
A6, IF INTEGRATOR PC ASSEMBLY
#05336901 Rev $D_1$

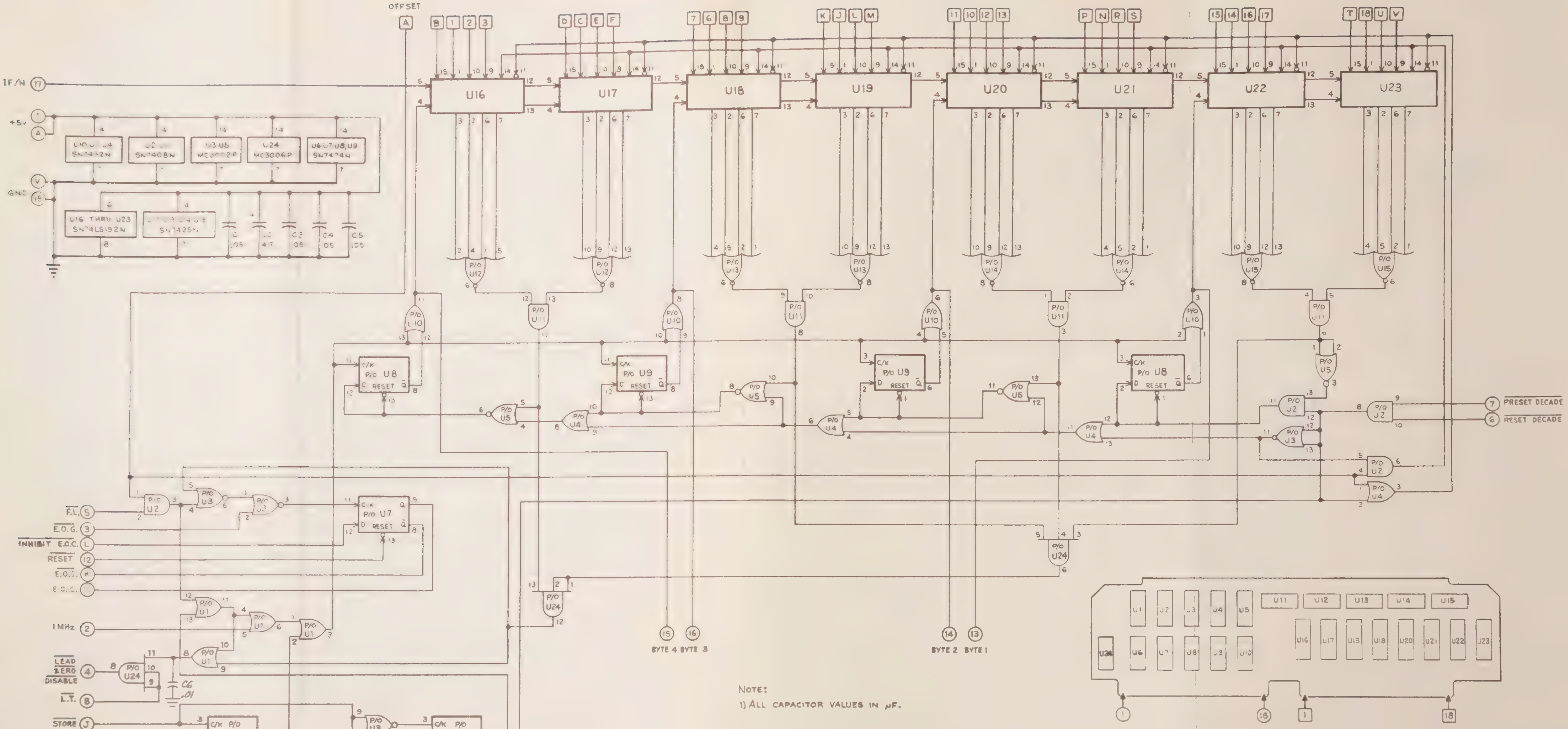

OFFSET
IF/N
+5v
GND
U16
U17
U18
U19
U20
U21
U22
U23
U16 THRU U23 SN74LS192N
U6,U7,U8,U9 SN7474N
U2 U1 SN7408N
U3 U5 MC3002P
U24 MC3006P
F.L.
E.O.G.
INHIBIT E.O.C.
RESET
E.O.C.
1MHz
LEAD ZERO DISABLE
STORE
PRESET DECADE
RESET DECADE
BYTE 4
BYTE 3
BYTE 2
BYTE 1
C6 .01
NOTE:
1) ALL CAPACITOR VALUES IN µF.

FIGURE 7-9
A6, IF INTEGRATOR SCHEMATIC
#7-05336901 Rev D

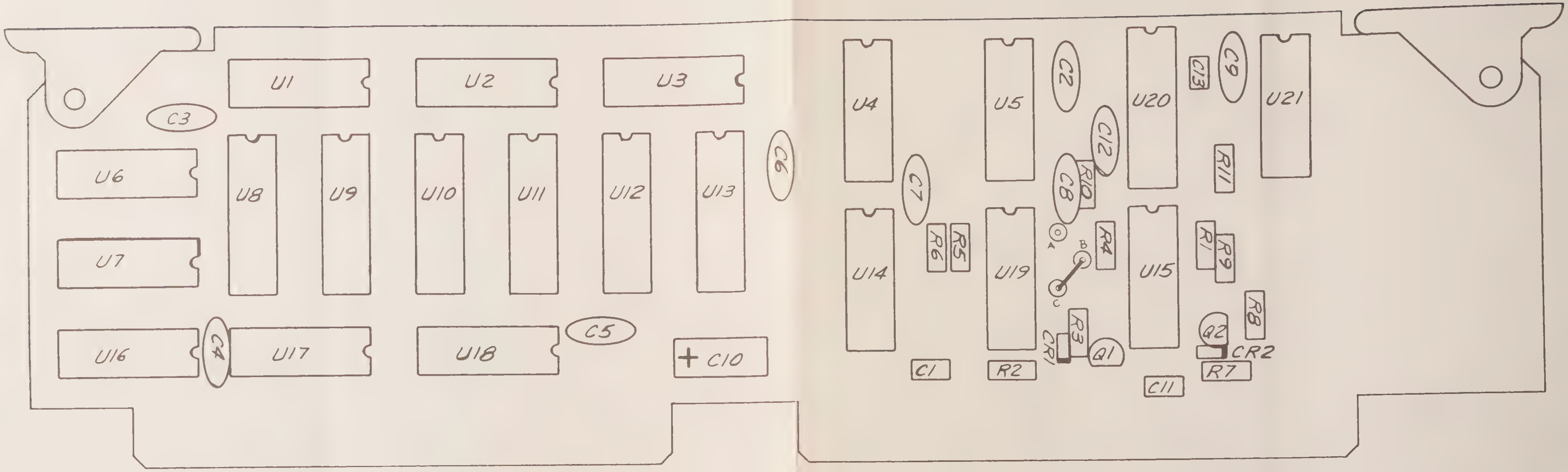
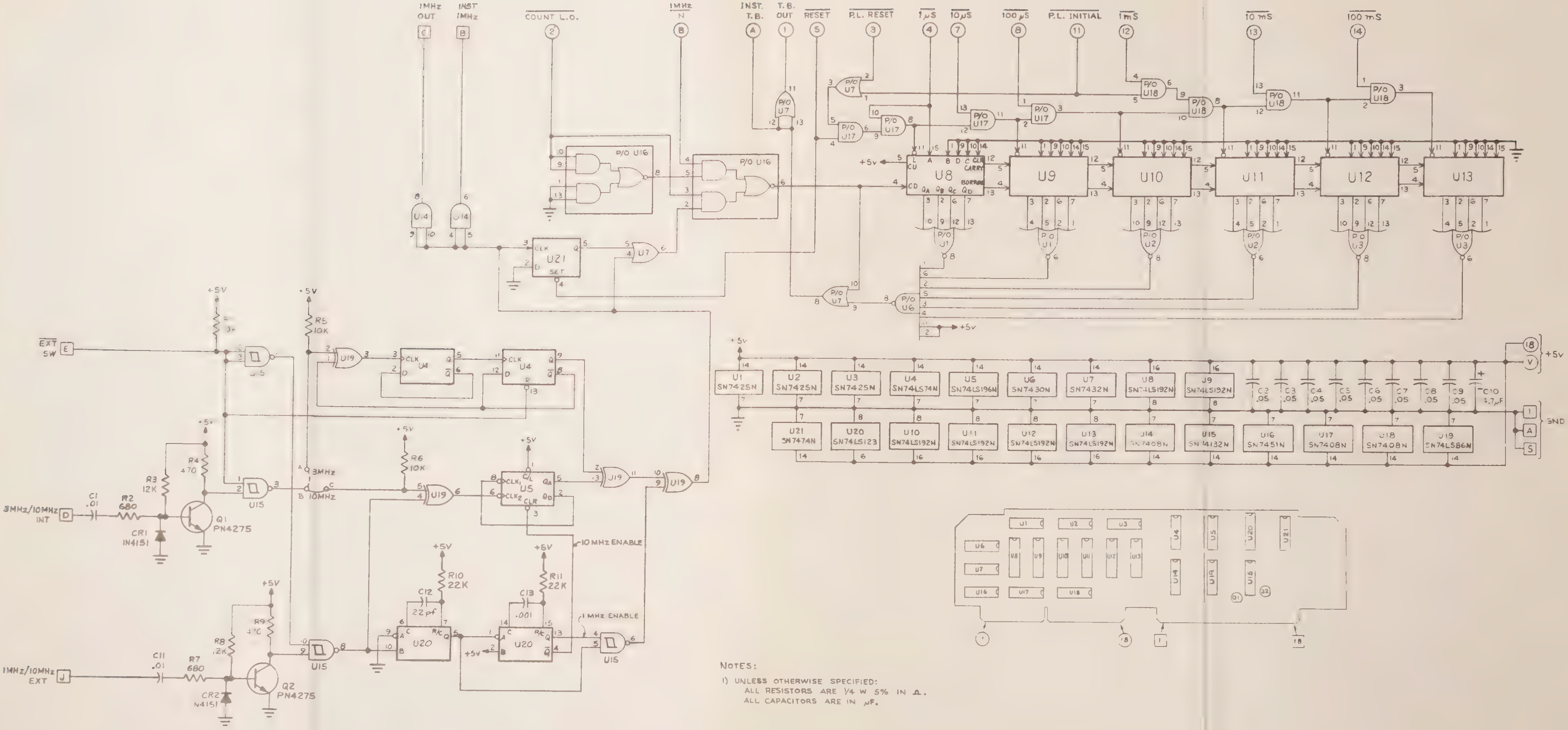

U1
U2
U3
C3
U6
U8
U9
U10
U11
U12
U13
C6
U7
U16
C4
U17
U18
C5
+ C10
U4
U5
C2
U20
C13
C9
U21
C12
C7
C8
R10
R11
U14
R6
R5
A
B
R4
U19
C
U15
R1
R9
R3
CR1
Q1
Q2
R8
CR2
C1
R2
C11
R7

FIGURE 7-10
A8, TIMEBASE PC ASSEMBLY
#05337901 Rev $D_1$


1MHz OUT
INST 1MHz
COUNT L.O.
1MHz N
INST. T.B.
T.B. OUT
RESET
P.L. RESET
1μS
10μS
100μS
P.L. INITIAL
1mS
10mS
100mS
P/O U16
P/O U7
P/O U17
P/O U18
P/O U1
P/O U2
P/O U3
P/O U6
U8
U9
U10
U11
U12
U13
U14
U21
U4
U5
U15
U19
U20
+5V
EXT SW
R5 10K
R6 10K
R4 470
R3 12K
R2 680
C1 .01
3MHz/10MHz INT
CR1 IN4151
Q1 PN4275
3MHz
10MHz
10MHz ENABLE
1MHz ENABLE
R10 22K
R11 22K
C12 22pf
C13 .001
R9 470
R8 12K
R7 680
C11 .01
1MHz/10MHz EXT
CR2 IN4151
Q2 PN4275
U1 SN7425N
U2 SN7425N
U3 SN7425N
U4 SN74LS74N
U5 SN74LS196N
U6 SN7430N
U7 SN7432N
U8 SN74LS192N
U9 SN74LS192N
U21 SN7474N
U20 SN74LS123
U10 SN74LS192N
U11 SN74LS192N
U12 SN74LS192N
U13 SN74LS192N
U14 SN7408N
U15 SN74132N
U16 SN7451N
U17 SN7408N
U18 SN7408N
U19 SN74LS86N
C2 .05
C3 .05
C4 .05
C5 .05
C6 .05
C7 .05
C8 .05
C9 .05
C10 4.7μF
+5v
GND

NOTES:
1) UNLESS OTHERWISE SPECIFIED:
ALL RESISTORS ARE 1/4 W 5% IN Ω.
ALL CAPACITORS ARE IN μF.

FIGURE 7-11
A8, TIMEBASE SCHEMATIC
#7-05337901 Rev E

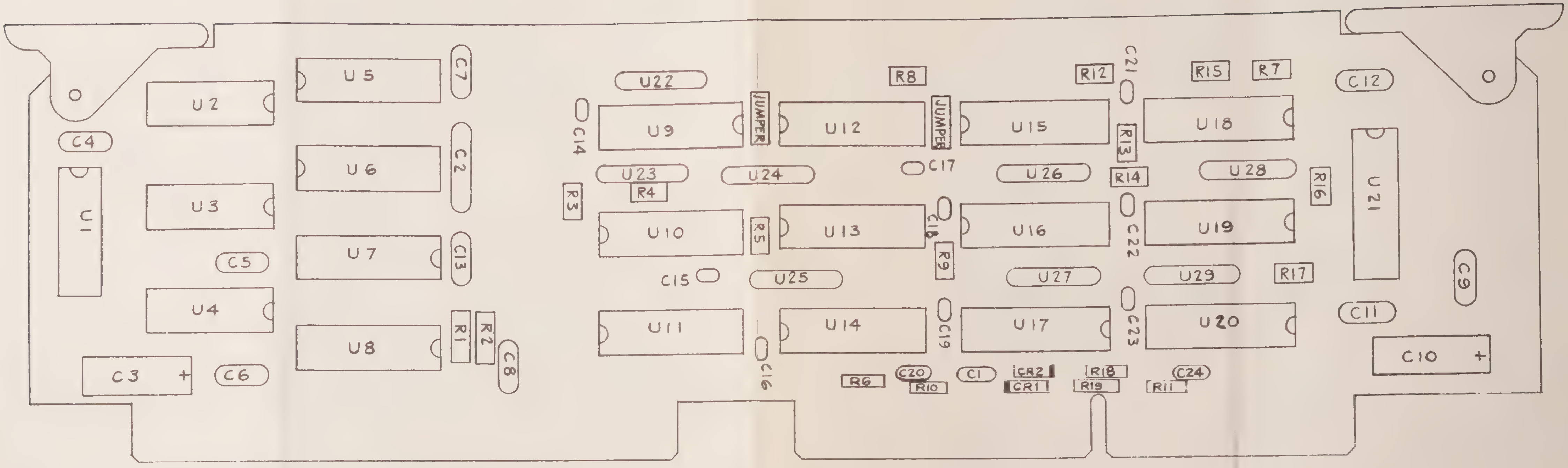
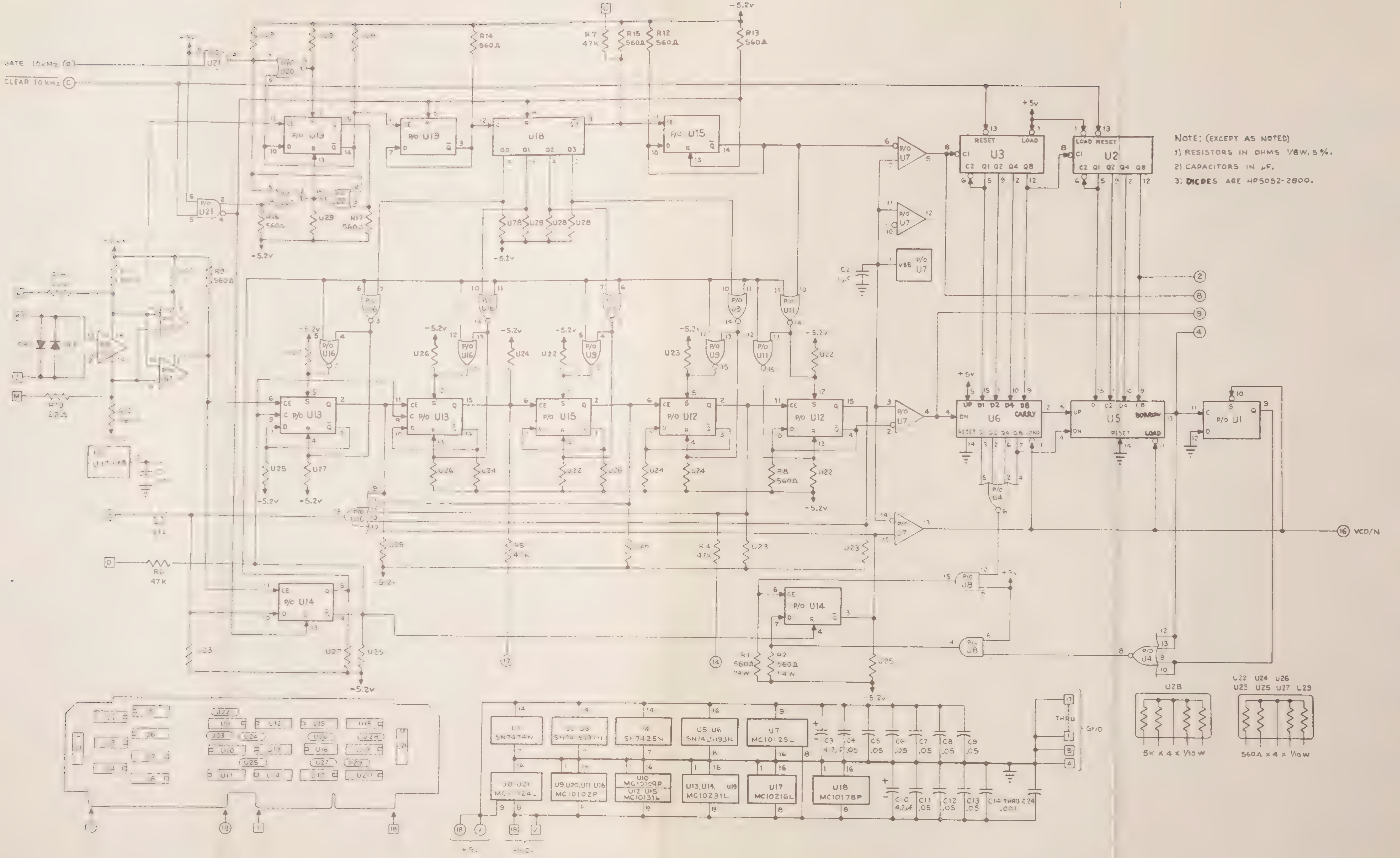

U5
C7
U22
JUMPER
R8
R12
C21
R15
R7
C12
U2
U9
U12
JUMPER
U15
U18
C14
R13
C4
U6
C2
U23
U24
C17
U26
R14
U28
R16
U21
R4
U1
U3
R3
U10
R5
U13
C18
U16
C22
U19
R9
C5
U7
C13
C15
U25
U27
U29
R17
C9
U4
U14
C19
U11
U17
C23
U20
C11
R1
R2
U8
C8
C10
+
C3
+
C6
C16
R6
C20
R10
C1
CR2
CR1
R18
R19
C24
R11

FIGURE 7-12
A9, 10 kHz GENERATOR PC ASSEMBLY
#05334201 Rev $B_2$


GATE 10 kHz (B)
CLEAR 10 kHz (C)
R14 560Ω
R7 47K
R15 560Ω
R12 560Ω
R13 560Ω
-5.2v
+5v
P/O U19
U18
P/O U15
P/O U20
P/O U21
R16 560Ω
U29
R17 560Ω
U28
R9 560Ω
RESET
LOAD
U3
U2
C1 C2 Q1 Q2 Q4 Q8
P/O U7
VBB P/O U7
C2 1µF
P/O U16
P/O U9
P/O U11
P/O U10
P/O U13
P/O U12
P/O U14
UP D1 D2 D4 D8 CARRY
DN
U6
U5
BORROW
P/O U1
P/O U4
P/O U8
VCO/N
R6 47K
R5 47K
R4 47K
R8 560Ω
R1 560Ω 1/4W
R2 560Ω 1/4W
R3 22Ω
U22
U23
U24
U25
U26
U27
U1 SN7474N
U2 U3 SN74S197N
U4 SN7425N
U5 U6 SN74LS193N
U7 MC10125L
U8 U21 MC10124L
U9,U20,U11 U16 MC10102P
U10 MC10109P
U12 U15 MC10131L
U13,U14, U19 MC10231L
U17 MC10216L
U18 MC10178P
C3 4.7µF
C4 .05
C5 .05
C6 .05
C7 .05
C8 .05
C9 .05
C10 4.7µF
C11 .05
C12 .05
C13 .05
C14 THRU C24 .001
THRU
GND
+5v
-5.2v
U28
5K x 4 x 1/10 W
U22 U24 U26
U23 U25 U27 U29
560Ω x 4 x 1/10 W

NOTE: (EXCEPT AS NOTED)
1) RESISTORS IN OHMS 1/8W, 5%.
2) CAPACITORS IN µF.
3) DIODES ARE HP5052-2800.

FIGURE 7-13
A9, 10 kHz GENERATOR SCHEMATIC
#7-05334201 Rev C

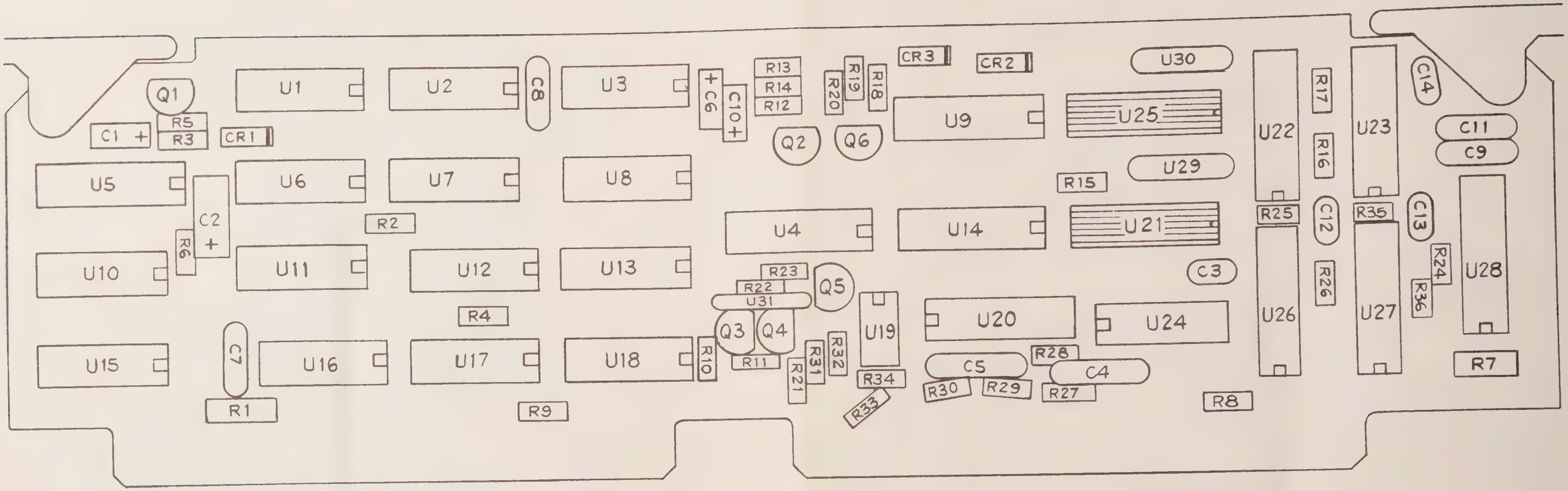
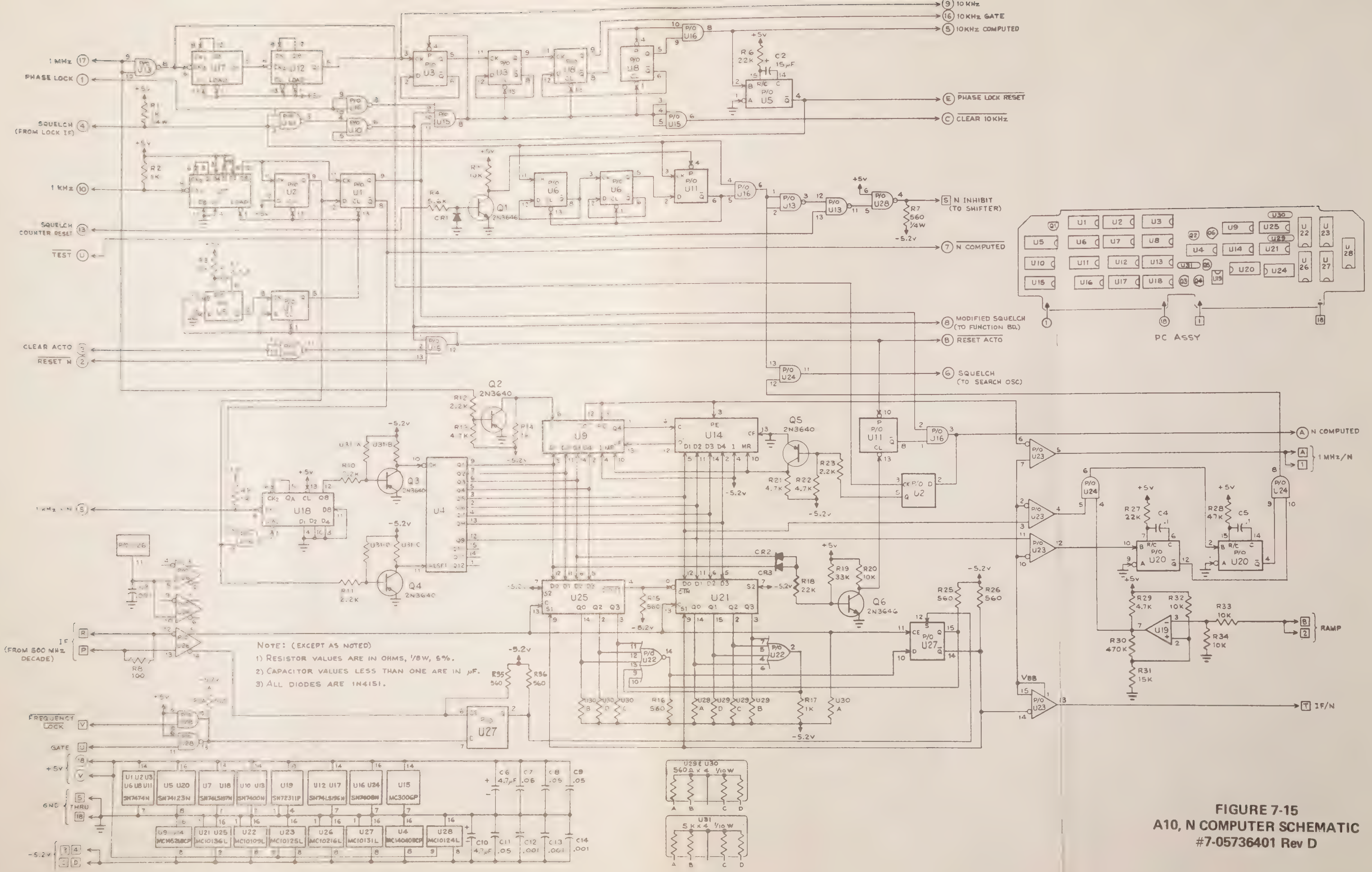

Q1
U1
U2
C8
U3
C6
C10
R13
R14
R12
R20
R19
R18
CR3
CR2
U30
U22
R17
U23
C14
C1
R5
R3
CR1
Q2
Q6
U9
U25
C11
C9
U5
U6
U7
U8
R15
U29
R16
C2
R2
U4
U14
U21
R25
C12
R35
C13
R24
U28
R6
U10
U11
U12
U13
R23
Q5
R22
U31
C3
R26
U26
U27
R36
R4
Q3
Q4
U19
U20
U24
U15
C7
U16
U17
U18
R10
R11
R31
R32
R21
R34
C5
R28
C4
R7
R30
R29
R27
R33
R8
R1
R9

**FIGURE 7-14**
**A10, N COMPUTER PC ASSEMBLY**
**#05736401 Rev $D_1$**



10 KHz
10KHz GATE
10KHz COMPUTED
1 MHz
PHASE LOCK
SQUELCH (FROM LOCK IF)
1 KHz
SQUELCH COUNTER RESET
TEST
CLEAR ACTO
RESET N
PHASE LOCK RESET
CLEAR 10KHz
N INHIBIT (TO SHIFTER)
N COMPUTED
MODIFIED SQUELCH (TO FUNCTION BD)
RESET ACTO
SQUELCH (TO SEARCH OSC)
N COMPUTED
1 MHz/N
RAMP
IF/N
1 MHz ÷ N
IF (FROM 500 MHz DECADE)
FREQUENCY LOCK
GATE
+5V
GND 5 THRU 18
-5.2V
PC ASSY
Q1 2N3646
Q2 2N3640
Q3 2N3640
Q4 2N3640
Q5 2N3640
Q6 2N3646
U1 U2 U3 U6 U8 U11 SN7474N
U5 U20 SN74123N
U7 U18 SN74LS197N
U10 U13 SN7400N
U19 SN72311P
U12 U17 SN74LS196N
U16 U24 SN7408N
U15 MC3006P
U9 U14 MC10136L
U21 U25 MC10136L
U22 MC10109L
U23 MC10125L
U26 MC10216L
U27 MC10131L
U4 MC14040BCP
U28 MC10124L
U29 & U30 560Ω x 4 1/10W
U31 5K x 4 1/10W
NOTE: (EXCEPT AS NOTED)
1) RESISTOR VALUES ARE IN OHMS, 1/8W, 5%.
2) CAPACITOR VALUES LESS THAN ONE ARE IN µF.
3) ALL DIODES ARE 1N4151.

FIGURE 7-15
A10, N COMPUTER SCHEMATIC
#7-05736401 Rev D

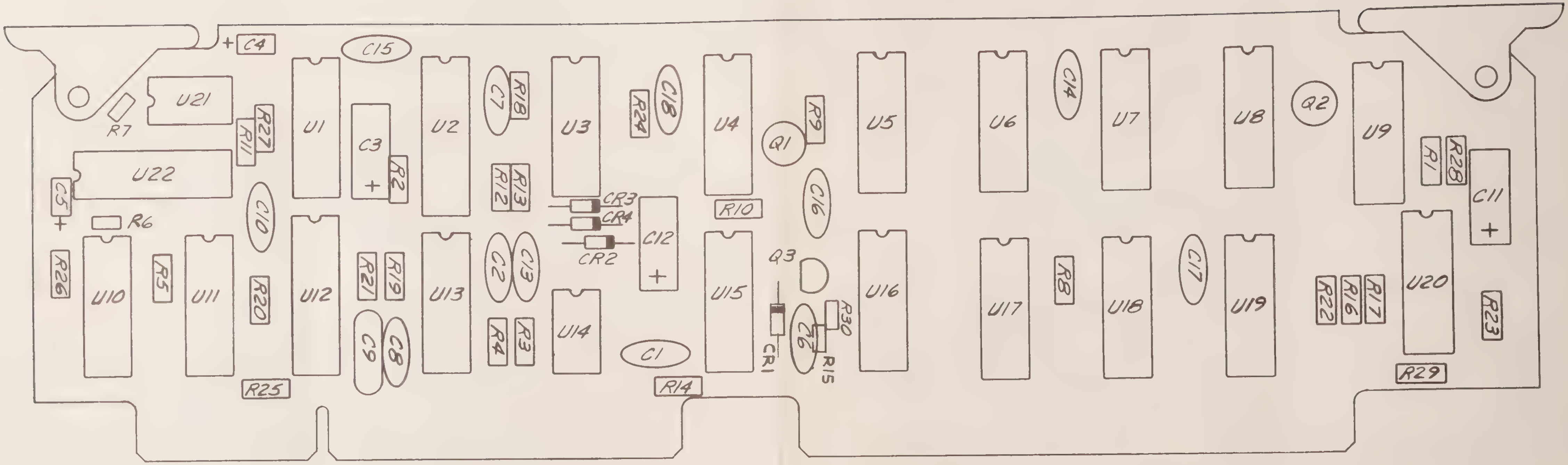
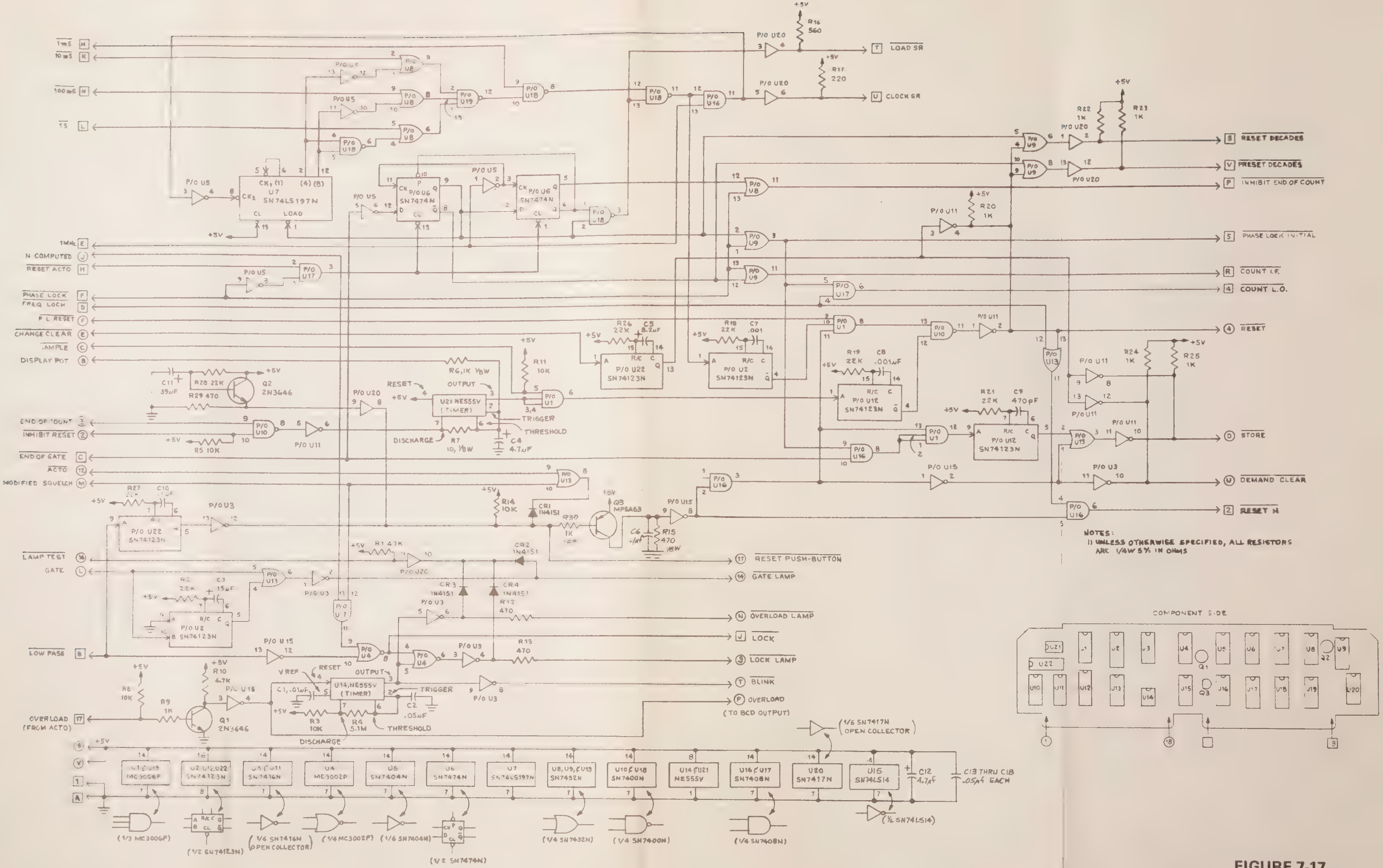
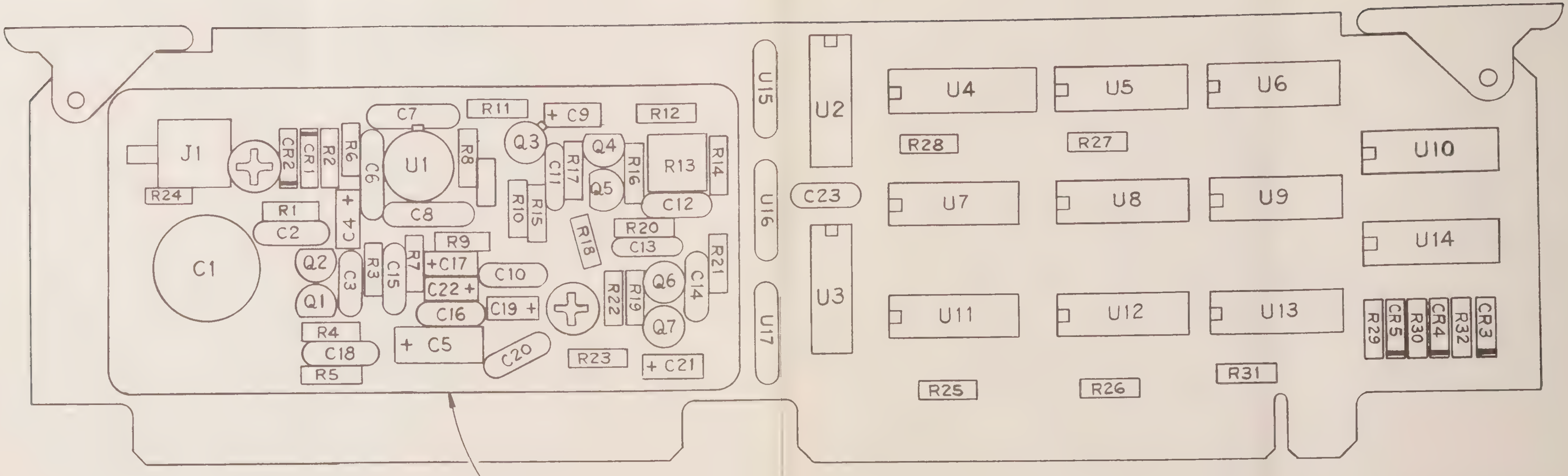

C4
C15
U21
R7
R27
R11
U1
C3
U2
C7
R18
U3
R24
C18
U4
R9
Q1
U5
U6
C14
U7
U8
Q2
U9
R1
R28
C11
U22
R2
R12
R13
CR3
CR4
CR2
C12
R10
C16
C5
R6
C10
R26
U10
R5
U11
R20
U12
R21
R19
U13
C2
C13
R4
R3
U14
C9
C8
C1
U15
Q3
CR1
C6
R30
R15
U16
U17
R8
U18
C17
U19
R22
R16
R17
U20
R23
R25
R14
R29

FIGURE 7-16
A11, FUNCTION PC ASSEMBLY
#05338601 Rev F


1mS M
10mS K
100mS N
1S L
1MHz E
N COMPUTED J
RESET ACTO H
PHASE LOCK F
FREQ LOCK D
P L RESET F
CHANGE CLEAR E
SAMPLE C
DISPLAY POT B
END OF COUNT 3
INHIBIT RESET 2
END OF GATE C
ACTO 12
MODIFIED SQUELCH M
LAMP TEST 16
GATE L
LOW PASS B
OVERLOAD 17
(FROM ACTO)
T LOAD SR
U CLOCK SR
S RESET DECADES
V PRESET DECADES
P INHIBIT END OF COUNT
5 PHASE LOCK INITIAL
R COUNT I.F.
4 COUNT L.O.
4 RESET
D STORE
U DEMAND CLEAR
2 RESET N
17 RESET PUSH-BUTTON
14 GATE LAMP
N OVERLOAD LAMP
J LOCK
S LOCK LAMP
T BLINK
P OVERLOAD
(TO BCD OUTPUT)
U7 SN74LS197N
CK1 (1) (4) (8) CK2 CL LOAD
P/O U6 SN7474N
U21 NE555V (TIMER)
U14, NE555V (TIMER)
P/O U22 SN74123N
P/O U2 SN74123N
P/O U12 SN74123N
RESET OUTPUT TRIGGER THRESHOLD DISCHARGE VREF
R16 560
R17 220
R22 1K
R23 1K
R20 1K
R24 1K
R25 1K
R26 22K
C5 8.2uF
R18 22K
C7 .001
R19 22K
C8 .001uF
R21 22K
C9 470pF
R11 10K
R6, 1K 1/8W
R7 10, 1/8W
C4 4.7uF
C11 39uF
R28 22K
R29 470
Q2 2N3646
R5 10K
R27 22K
C10 .1uF
R14 10K
CR1 1N4151
R30 1K 1/8W
Q3 MPSA63
C6 .1uF
R15 470 1/8W
R1 4.7K
CR2 1N4151
CR3 1N4151
CR4 1N4151
R12 470
R13 470
R2 22K
C3 15uF
R8 10K
R9 1K
R10 4.7K
Q1 2N3646
C1, .01uF
C2 .05uF
R3 10K
R4 5.1M
+5V
U1 & U19 MC3006P
U2 U12, U22 SN74123N
U3 & U11 SN7416N
U4 MC3002P
U5 SN7404N
U6 SN7474N
U7 SN74LS197N
U8, U9, & U13 SN7432N
U10 & U18 SN7400N
U14 & U21 NE555V
U16 & U17 SN7408N
U20 SN7417N
U15 SN74LS14
C12 4.7uF
C13 THRU C18 .05uF EACH
(1/3 MC3006P)
(1/2 SN74123N)
(1/6 SN7416N OPEN COLLECTOR)
(1/4 MC3002P)
(1/6 SN7404N)
(1/2 SN7474N)
(1/4 SN7432N)
(1/4 SN7400N)
(1/4 SN7408N)
(1/6 SN7417N OPEN COLLECTOR)
(1/6 SN74LS14)
COMPONENT SIDE
U21 U22 U1 U2 U3 U4 U5 U6 U7 U8 U9 Q1 Q2
U10 U11 U12 U13 U14 U15 Q3 U16 U17 U18 U19 U20
1 18 B

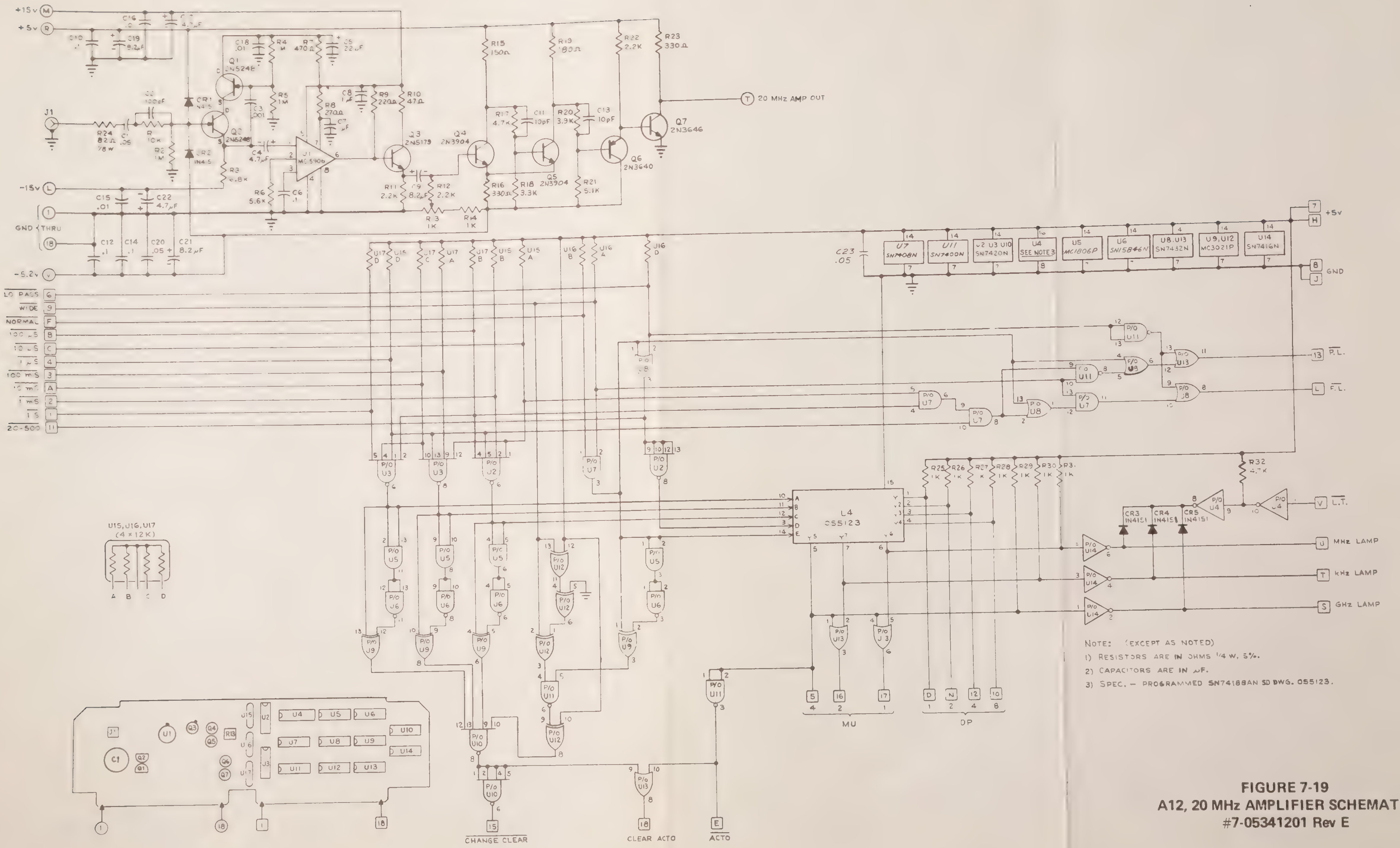
NOTES:
1) UNLESS OTHERWISE SPECIFIED, ALL RESISTORS ARE 1/4W 5% IN OHMS

FIGURE 7-17
A11, FUNCTION SCHEMATIC
#7-05338601 Rev G


J1
R24
CR2
CR1
R2
R6
C6
C7
U1
C8
R11
R8
+ C9
Q3
C11
R17
Q4
Q5
R16
R12
R13
R14
C12
R1
C2
C1
+
C4
Q2
Q1
C3
R3
C15
R7
R9
+C17
C22 +
C16
C19 +
C10
R10
R15
R18
R20
C13
R21
R22
R19
Q6
Q7
C14
R4
C18
R5
+ C5
C20
R23
+ C21
U15
U16
U17
U2
C23
U3
U4
U5
U6
R28
R27
U10
U7
U8
U9
U14
U11
U12
U13
R29
CR5
R30
CR4
R32
CR3
R31
R25
R26

COMPONENTS UNDER SHIELD CAN.

FIGURE 7-18
A12, 20 MHz AMPLIFIER PC ASSEMBLY
#05341201 Rev D


+15v M
+5v R
-15v L
GND THRU 1 18
-5.2v V
LO PASS 6
WIDE 9
NORMAL F
100 µS B
10 µS C
1 µS 4
100 mS 3
10 mS A
1 mS 2
1 S 1
20-500 11
J1
R24 82Ω 1/8W
C1 .05
R2 1M
R3 6.8K
R4 1M
R5 1M
R6 5.6K
R7 470Ω
R8 270Ω
R9 220Ω
R10 47Ω
R11 2.2K
R12 2.2K
R13 1K
R14 1K
R15 150Ω
R16 330Ω
R17 4.7K
R18 3.3K
R19 180Ω
R20 3.9K
R21 5.1K
R22 2.2K
R23 330Ω
CR1 1N415
CR2 1N415
Q1 2N5248
Q2 2N5248
U1 MC5906
Q3 2N5179
Q4 2N3904
Q5 2N3904
Q6 2N3640
Q7 2N3646
20 MHz AMP OUT T
C23 .05
U7 SN7408N
U11 SN7400N
U2 U3 U10 SN7420N
U4 SEE NOTE 3
U5 MC1806P
U6 SN15846N
U8, U13 SN7432N
U9, U12 MC3021P
U14 SN7416N
+5v 7 H
GND 8 J
P.L. 13
F.L. L
L.T. V
U4 055123
R32 4.7K
CR3 1N4151
CR4 1N4151
CR5 1N4151
MHz LAMP U
kHz LAMP T
GHz LAMP S
MU 5 16 17 4 2 1
DP D N 12 10 1 2 4 8
CHANGE CLEAR 15
CLEAR ACTO 18
ACTO E
U15, U16, U17 (4 × 12K) A B C D

NOTE: (EXCEPT AS NOTED)

1) RESISTORS ARE IN OHMS 1/4 W, 5%.

2) CAPACITORS ARE IN µF.

3) SPEC. – PROGRAMMED SN74188AN SD DWG. 055123.

**FIGURE 7-19**
**A12, 20 MHz AMPLIFIER SCHEMATIC**
**#7-05341201 Rev E**

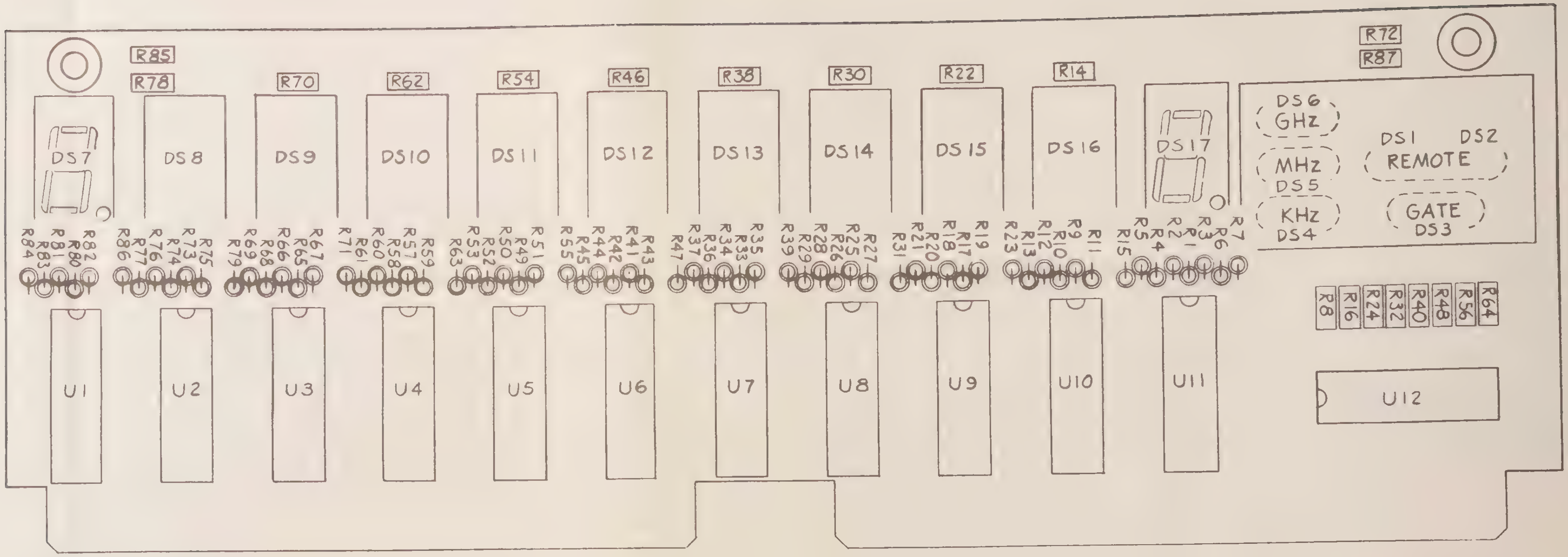
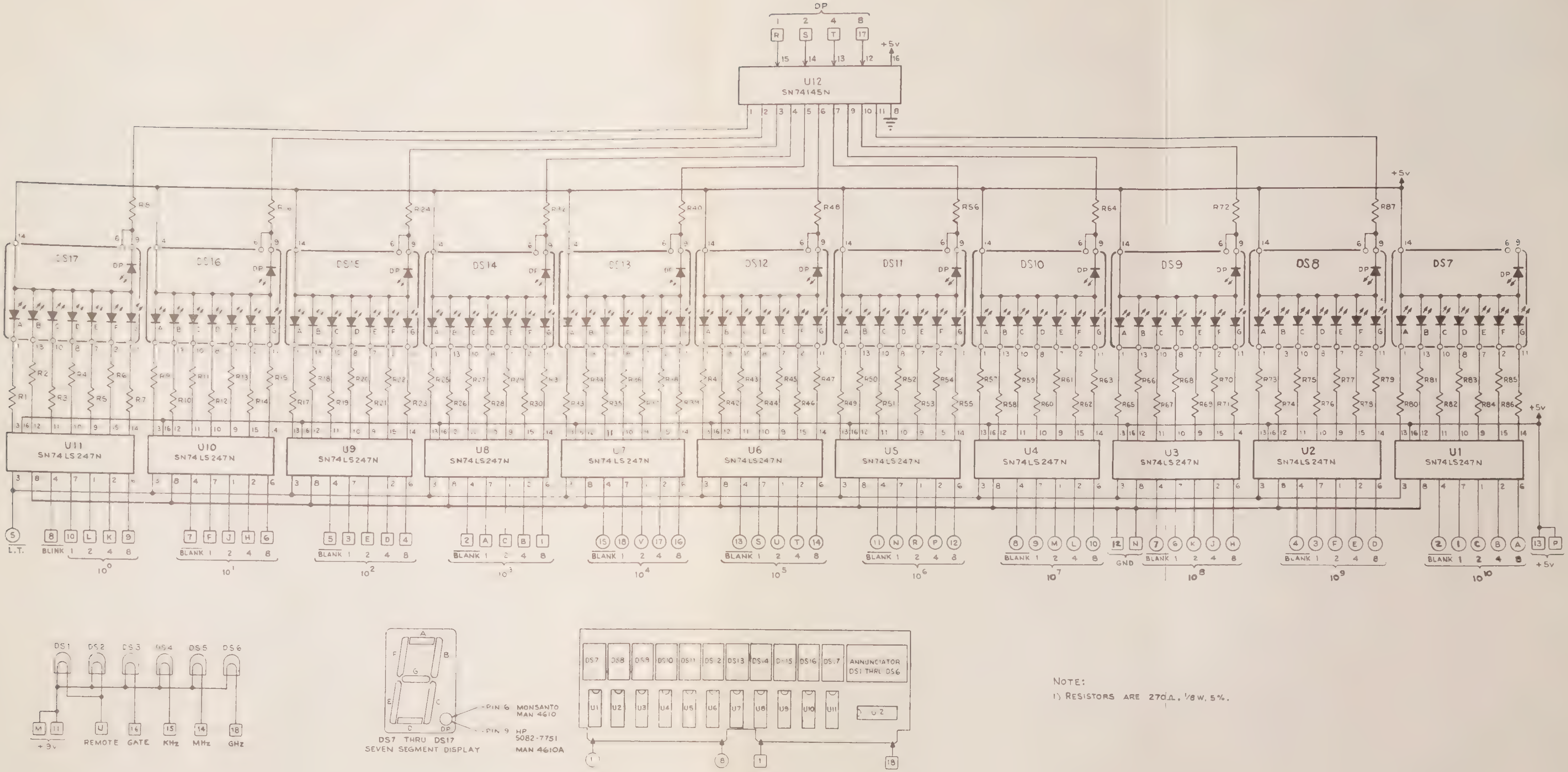
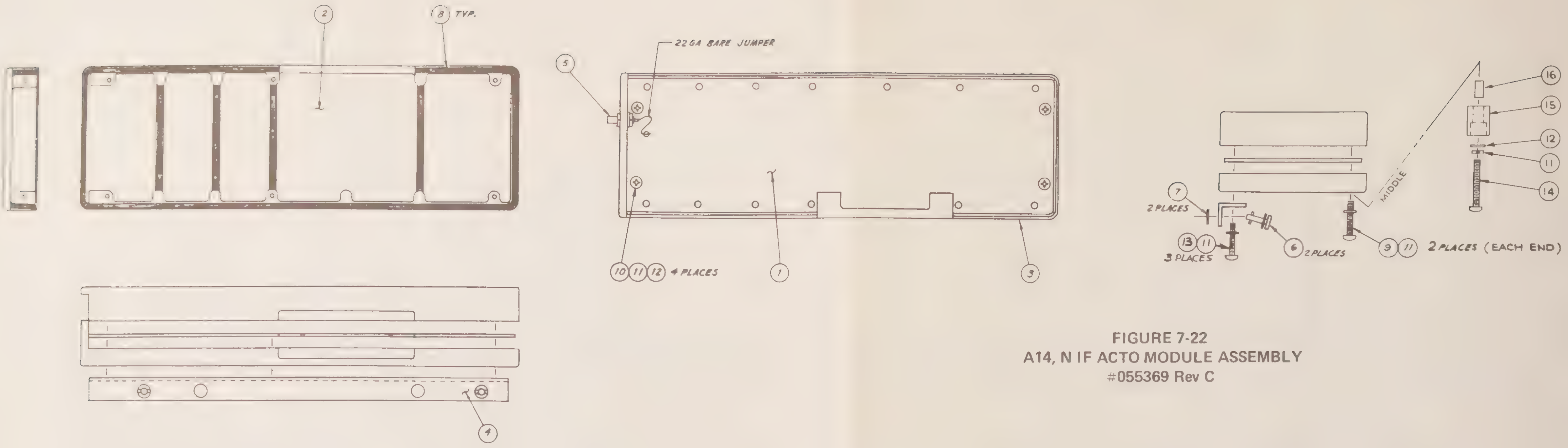

R85
R78
R70
R62
R54
R46
R38
R30
R22
R14
R72
R87
DS7
DS8
DS9
DS10
DS11
DS12
DS13
DS14
DS15
DS16
DS17
DS6
GHz
MHz
DS5
KHz
DS4
DS1
DS2
REMOTE
GATE
DS3
R84 R83 R81 R80 R82
R86 R77 R76 R74 R73 R75
R79 R69 R68 R66 R65 R67
R71 R61 R60 R58 R57 R59
R63 R53 R52 R50 R49 R51
R55 R45 R44 R42 R41 R43
R47 R37 R36 R34 R33 R35
R39 R29 R28 R26 R25 R27
R31 R21 R20 R18 R17 R19
R23 R13 R12 R10 R9 R11
R15 R5 R4 R2 R1 R3 R6 R7
R8
R16
R24
R32
R40
R48
R56
R64
U1
U2
U3
U4
U5
U6
U7
U8
U9
U10
U11
U12

FIGURE 7-20
A13, DISPLAY PC ASSEMBLY
#05326301 Rev $B_2$


DP
1 2 4 8
R S T 17
+5v
U12
SN74145N
+5v
DS17
DS16
DS15
DS14
DS13
DS12
DS11
DS10
DS9
DS8
DS7
U11 SN74LS247N
U10 SN74LS247N
U9 SN74LS247N
U8 SN74LS247N
U7 SN74LS247N
U6 SN74LS247N
U5 SN74LS247N
U4 SN74LS247N
U3 SN74LS247N
U2 SN74LS247N
U1 SN74LS247N
L.T.
BLINK 1 2 4 8
$10^0$
BLANK 1 2 4 8
$10^1$
$10^2$
$10^3$
$10^4$
$10^5$
$10^6$
$10^7$
GND
$10^8$
$10^9$
$10^{10}$
+5v
DS1 DS2 DS3 DS4 DS5 DS6
+5v REMOTE GATE KHz MHz GHz
DS7 THRU DS17
SEVEN SEGMENT DISPLAY
PIN 6 MONSANTO MAN 4610
PIN 9 HP 5082-7751 MAN 4610A
ANNUNCIATOR DS1 THRU DS6

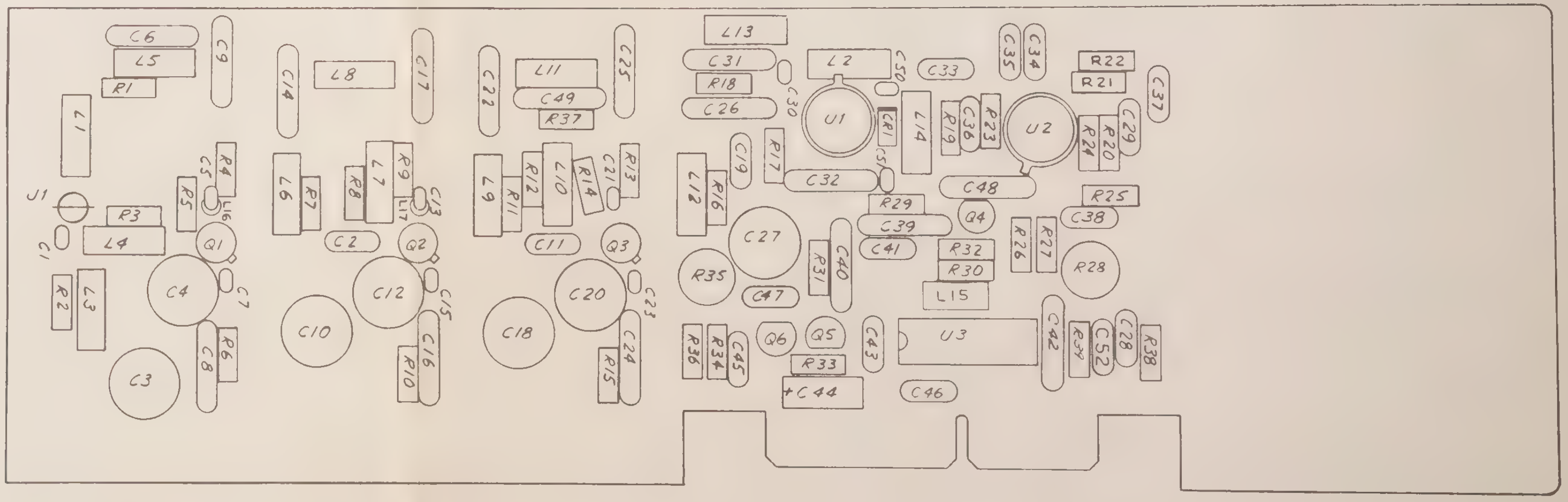
NOTE:
1) RESISTORS ARE 270Ω, 1/8W, 5%.

FIGURE 7-21
A13, DISPLAY SCHEMATIC
#7-05326301 Rev A



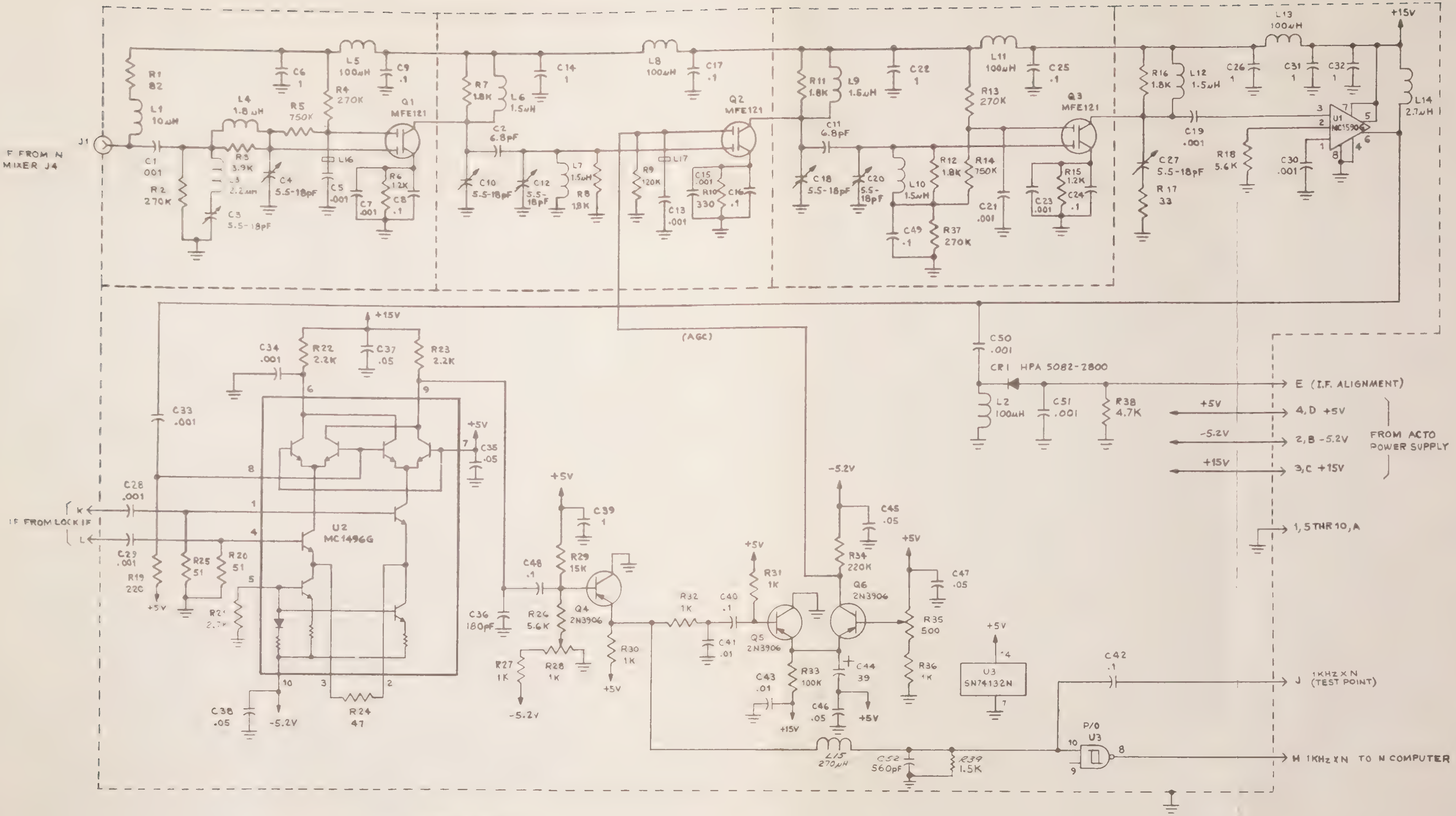
2
8 TYP.
5
22GA BARE JUMPER
10 11 12 4 PLACES
1
3
4
16
15
12
11
14
MIDDLE
7
2 PLACES
13 11
3 PLACES
6 2 PLACES
9 11 2 PLACES (EACH END)

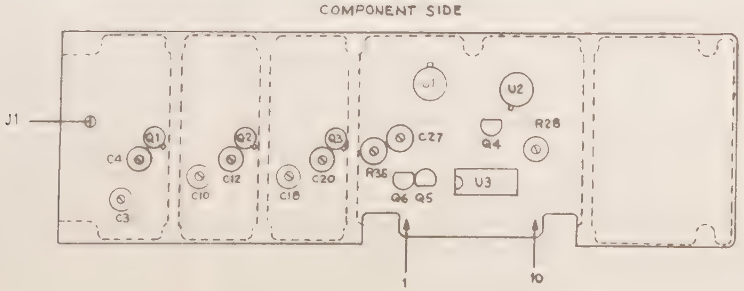
FIGURE 7-22
A14, N IF ACTO MODULE ASSEMBLY
#055369 Rev C



C6
L5
R1
C9
L1
U1
C1
R3
L4
R2
L3
C3
C4
R4
C5
R5
L16
Q1
C7
R6
C8
C14
L8
C17
L6
R7
R8
L7
R9
L17
C13
C2
Q2
C10
C12
C15
C16
R10
C22
L11
C49
R37
C25
L9
R11
R12
L10
R14
C21
R13
C11
Q3
C18
C20
C23
C24
R15
L13
C31
R18
C26
C30
L2
C50
U1
CR1
L14
C33
C35
C34
R19
C36
R23
U2
R22
R21
C37
R24
R20
C29
C19
R17
C51
C32
L12
R16
C27
R35
C48
R29
Q4
C39
C41
R25
C38
R26
R27
R32
R30
L15
R28
R31
C40
C47
R36
R34
C45
Q6
Q5
R33
+C44
C43
U3
C46
C42
R39
C52
C28
R38

FIGURE 7-23
A14, N IF PC ASSEMBLY
#05324601 Rev $G_1$


F FROM N MIXER J4
J1
R1 82
L1 10µH
C1 .001
R2 270K
L4 1.8µH
R3 3.9K
L3 2.2µH
C3 5.5-18pF
C4 5.5-18pF
R5 750K
C6 1
L5 100µH
C9 .1
R4 270K
L16
C5 .001
Q1 MFE121
R6 1.2K
C7 .001
C8 .1
R7 1.8K
L6 1.5µH
C14 1
C2 6.8pF
C10 5.5-18pF
C12 5.5-18pF
L7 1.5µH
R8 1.8K
L8 100µH
C17 .1
Q2 MFE121
R9 120K
L17
C13 .001
C15 .001
R10 330
C16 .1
R11 1.8K
L9 1.5µH
C22 1
C11 6.8pF
C18 5.5-18pF
C20 5.5-18pF
L10 1.5µH
R12 1.8K
R14 750K
C49 .1
R37 270K
L11 100µH
C25 .1
R13 270K
Q3 MFE121
C21 .001
C23 .001
R15 1.2K
C24 .1
R16 1.8K
L12 1.5µH
C26 1
L13 100µH
C31 1
C32 1
+15V
L14 2.7µH
C19 .001
C27 5.5-18pF
R17 33
R18 5.6K
C30 .001
U1 MC1590G
(AGC)
C50 .001
CR1 HPA 5082-2800
L2 100µH
C51 .001
R38 4.7K
E (I.F. ALIGNMENT)
+5V
4, D +5V
-5.2V
2, B -5.2V
+15V
3, C +15V
FROM ACTO POWER SUPPLY
1, 5 THR 10, A
+15V
C34 .001
R22 2.2K
C37 .05
R23 2.2K
C33 .001
C35 .05
+5V
U2 MC1496G
C28 .001
IF FROM LOCK IF
K
L
C29 .001
R19 220
R25 51
R20 51
R21 2.7K
+5V
C38 .05
-5.2V
R24 47
+5V
C39 1
C48 .1
R29 15K
Q4 2N3906
C36 180pF
R26 5.6K
R27 1K
R28 1K
-5.2V
R30 1K
+5V
R32 1K
C40 .1
C41 .01
+5V
R31 1K
Q5 2N3906
-5.2V
C45 .05
R34 220K
Q6 2N3906
+5V
C47 .05
R35 500
R36 1K
R33 100K
C43 .01
+15V
C44 39
C46 .05
+5V
L15 270µH
C52 560pF
R39 1.5K
+5V
U3 SN74132N
C42 .1
J 1KHz x N (TEST POINT)
P/O U3
H 1KHz x N TO N COMPUTER


COMPONENT SIDE
J1
Q1
C4
C3
Q2
C10
C12
C18
Q3
C20
C27
R36
Q6 Q5
U3
Q1
U2
Q4
R28
1
10

NOTES:

1) Unless otherwise specified
All Resistors are 1/4W 5% in ohms
all Capacitors are in µF.

2) R6 & R15 1.2k nominal, 560Ω minimum.
(Decrease nominal value to increase gain)

FIGURE 7-24
A14, N IF SCHEMATIC
#7-05324601 Rev $G_1$

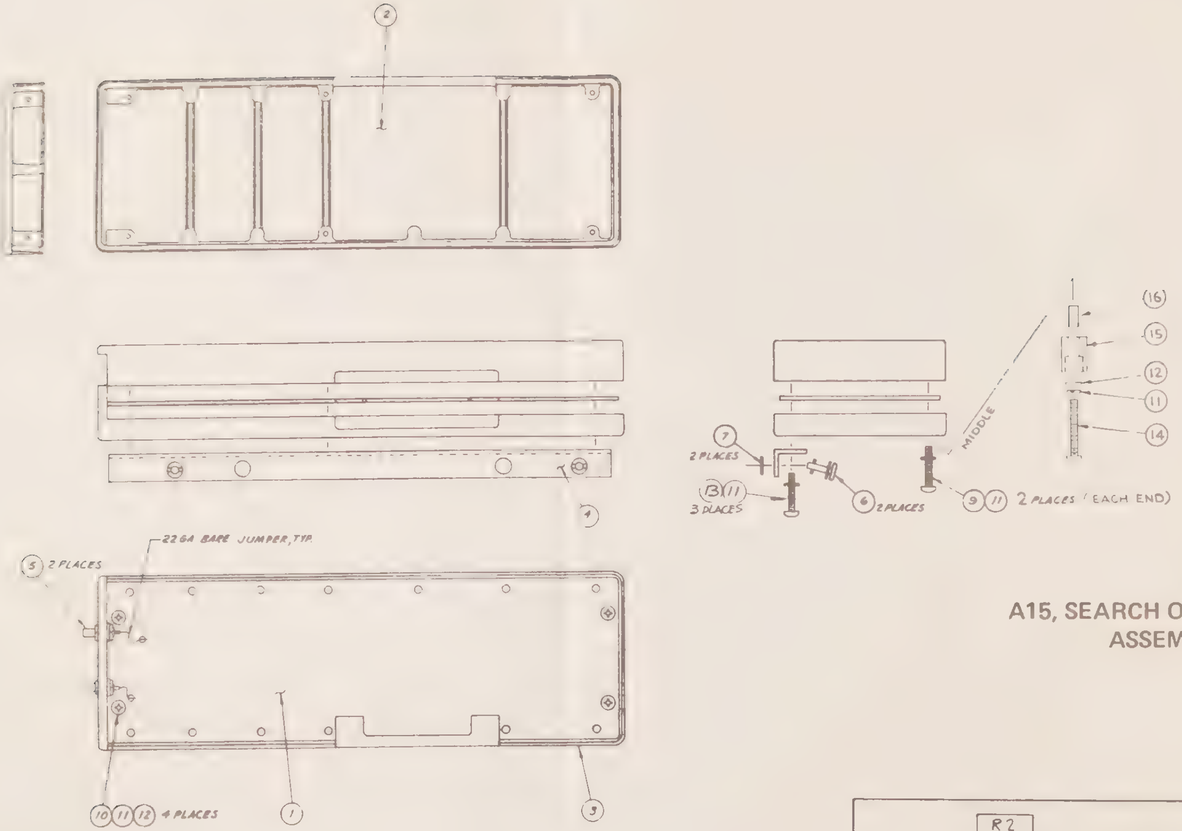

2
16
15
12
11
14
MIDDLE
7 2 PLACES
13 11 3 PLACES
6 2 PLACES
9 11 2 PLACES (EACH END)
4
22 GA BARE JUMPER, TYP
5 2 PLACES
10 11 12 4 PLACES
1
3

FIGURE 7-25
A15, SEARCH OSCILLATOR ACTO MODULE
ASSEMBLY #055370 Rev C

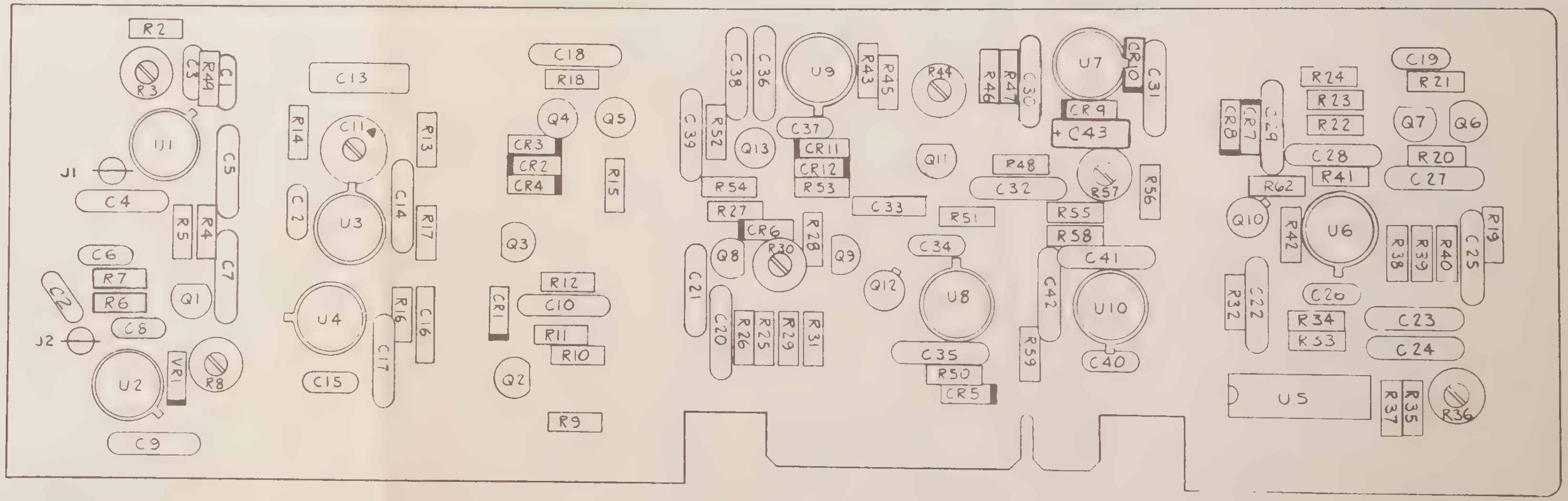
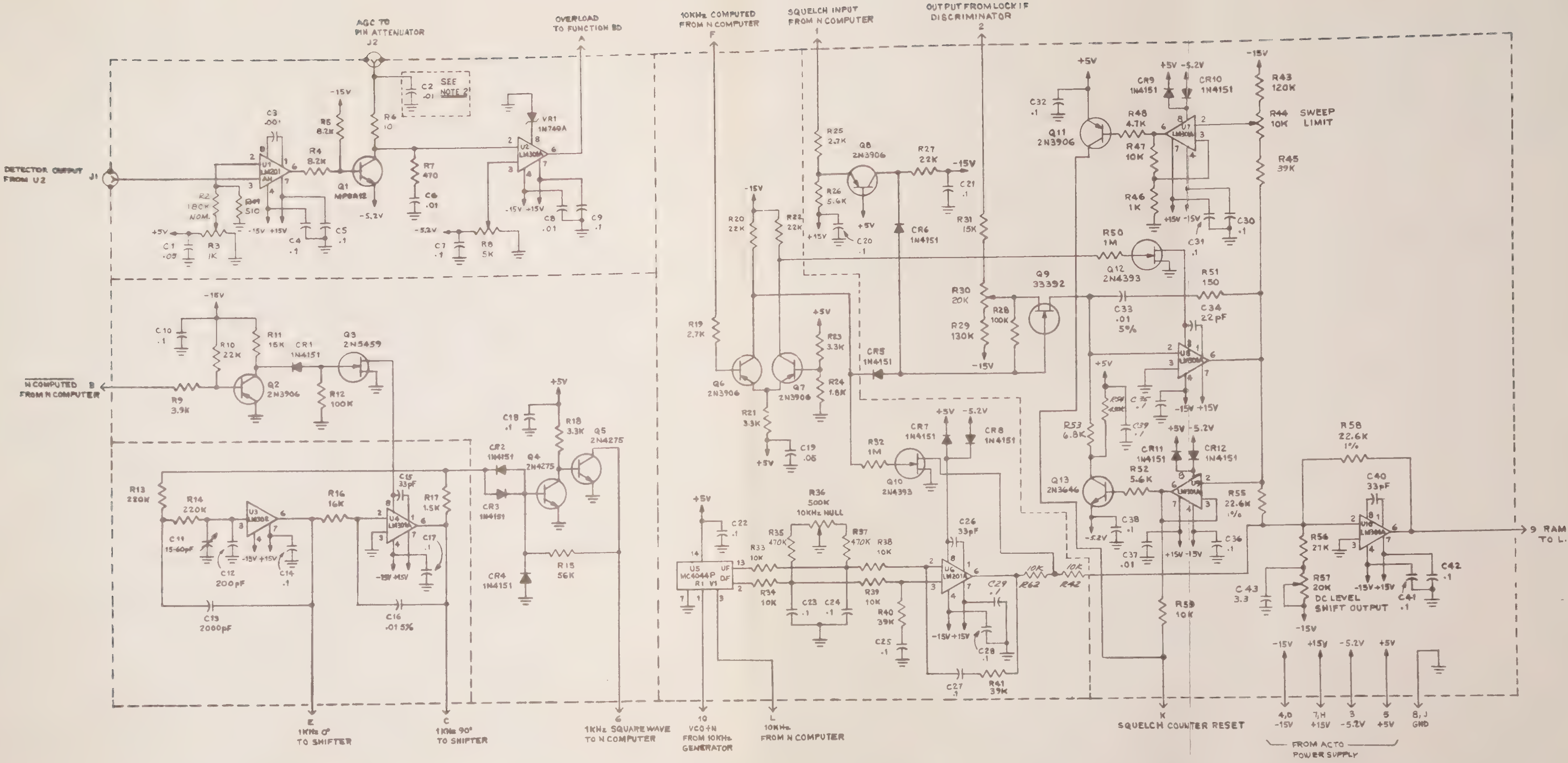
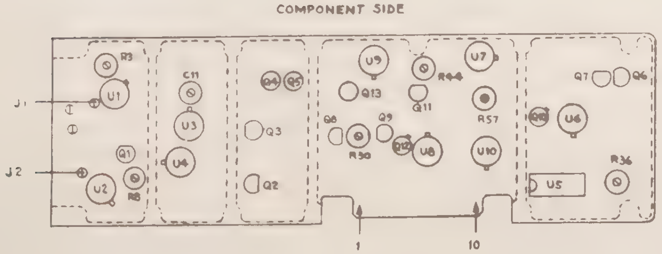

R2
R3
C3
R49
C1
U1
J1
C5
C4
R5
R4
C6
C7
R7
C2
R6
Q1
C8
J2
U2
VR1
R8
C9
C13
R14
C11
R13
C 2
U3
C14
R17
U4
R16
C16
C17
C15
C18
R18
Q4
Q5
CR3
CR2
CR4
R15
Q3
R12
C10
CR1
R11
R10
Q2
R9
C38
C36
U9
R43
R45
R44
C39
R52
Q13
C37
CR11
CR12
R53
R54
R27
CR6
R28
Q8
R30
Q9
C21
C20
R26
R25
R29
R31
R46
R47
C30
U7
CR10
C31
CR9
C43
Q11
R48
C32
R57
R56
C33
R51
R55
R58
C34
Q12
U8
C35
R50
CR5
C41
C42
U10
R59
C40
CR8
CR7
C29
R24
R23
R22
C19
R21
Q7
Q6
C28
R20
R41
C27
R62
Q10
R42
U6
R38
R39
R40
R19
C25
R32
C22
C26
R34
R33
C23
C24
U5
R37
R35
R36

FIGURE 7-26
A15, SEARCH OSCILLATOR PC ASSEMBLY
#05322801 Rev $K_1$



AGC TO PIN ATTENUATOR J2
OVERLOAD TO FUNCTION BD A
10KHz COMPUTED FROM N COMPUTER F
SQUELCH INPUT FROM N COMPUTER 1
OUTPUT FROM LOCK IF DISCRIMINATOR 2
DETECTOR OUTPUT FROM U2 J1
C2 .01 SEE NOTE 2
U1 LM201AH
U2 LM308A
Q1 MPS812
VR1 1N749A
R44 10K SWEEP LIMIT
R43 120K
R45 39K
Q11 2N3906
Q8 2N3906
Q9 33392
Q12 2N4393
CR9 1N4151
CR10 1N4151
N COMPUTED B FROM N COMPUTER
Q2 2N3906
Q3 2N5459
CR1 1N4151
Q6 2N3906
Q7 2N3906
CR5 1N4151
CR6 1N4151
Q10 2N4393
CR7 1N4151
CR8 1N4151
Q13 2N3646
CR11 1N4151
CR12 1N4151
R58 22.6K 1%
C40 33pF
R36 500K 10KHz NULL
U5 MC4044P
U6 LM201A
Q4 2N4275
Q5 2N4275
CR2 1N4151
CR3 1N4151
CR4 1N4151
U3 LM308
U4 LM301A
R57 20K DC LEVEL SHIFT OUTPUT
9 RAMP TO L.O.
E 1KHz 0° TO SHIFTER
C 1KHz 90° TO SHIFTER
6 1KHz SQUARE WAVE TO N COMPUTER
10 VCO+N FROM 10KHz GENERATOR
L 10KHz FROM N COMPUTER
K SQUELCH COUNTER RESET
4,D -15V
7,H +15V
3 -5.2V
5 +5V
8,J GND
FROM AC TO POWER SUPPLY



COMPONENT SIDE
J1
J2
U1
U2
U3
U4
U5
U6
U7
U8
U9
U10
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
Q11
Q12
Q13
R3
R8
R30
R36
R44
R57
C11
1
10

NOTES:
1) UNLESS OTHERWISE SPECIFIED:
ALL RESISTORS ARE 1/4 W 5% IN OHMS
ALL CAPACITORS ARE IN µF
2) DELETE C2 IF PIN ATTENUATOR IS CROWN #CS10090.

FIGURE 7-27
A15, SEARCH OSCILLATOR SCHEMATIC
#7-05322801 Rev H

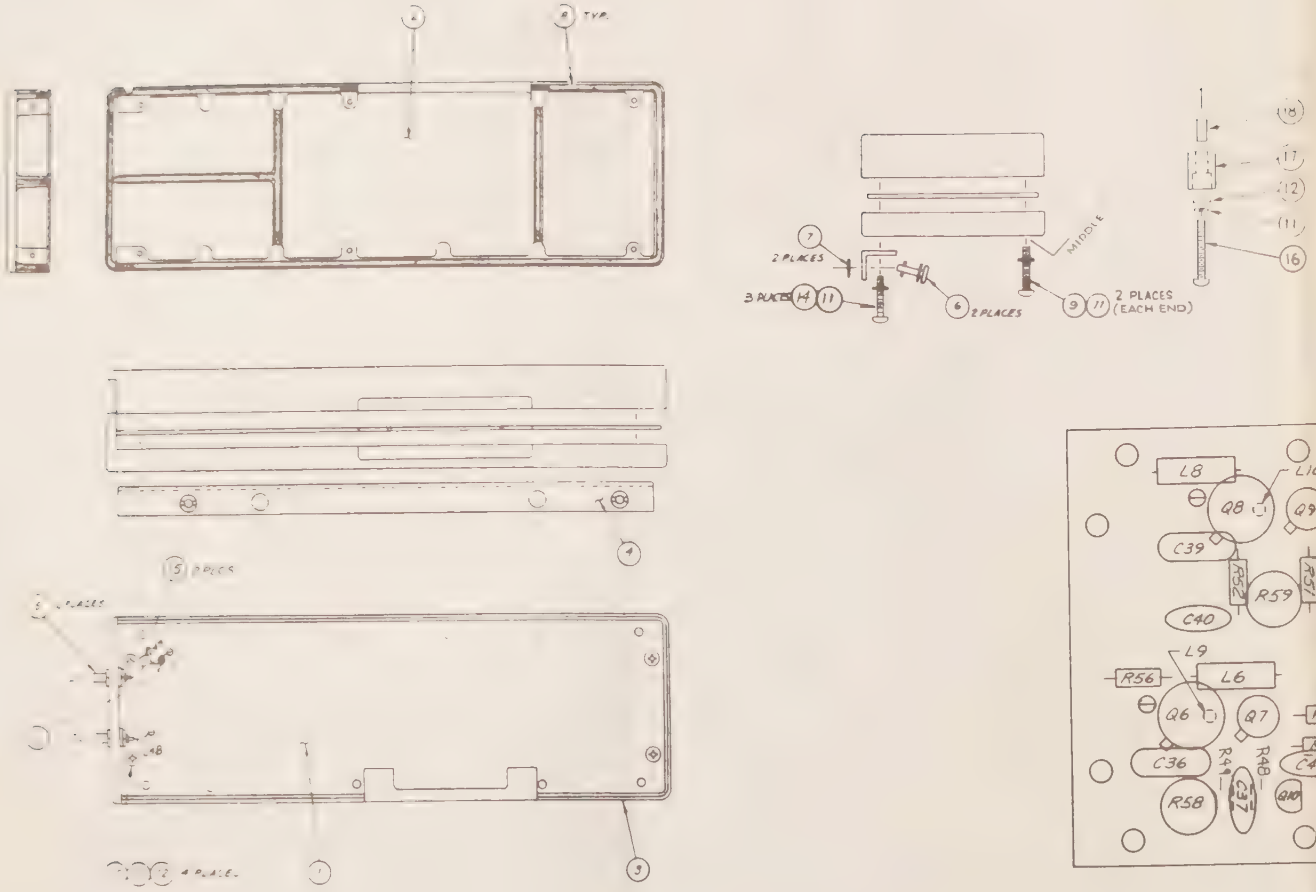
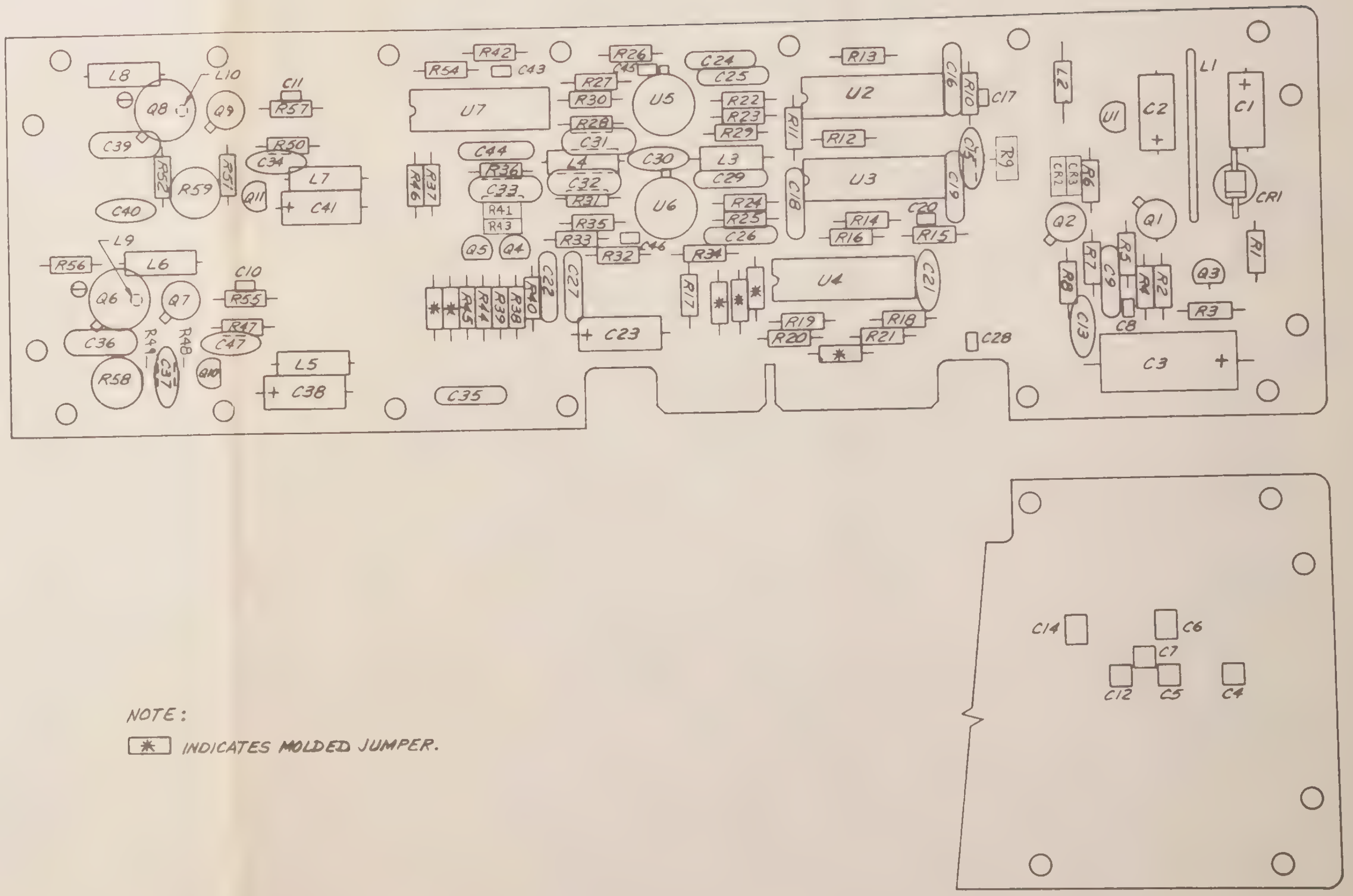

TYP.
MIDDLE
2 PLACES
3 PLACES
2 PLACES
2 PLACES (EACH END)
4 PLACES
2 PLACES

FIGURE 7-28
A16, LO/SHIFTER ACTO MODULE
ASSEMBLY #057167 Rev E


L8
L10
C11
R57
Q8
Q9
C39
R50
C34
R52
R59
R51
Q11
L7
C41
C40
L9
R56
L6
C10
R55
Q6
Q7
R47
C47
C36
R49
R48
C37
Q10
R58
L5
C38
C35
R42
R54
C43
U7
R26
C45
R27
R30
R28
C31
C44
R36
C33
R41
R43
R37
R46
L4
C32
R31
R35
R33
Q5
Q4
C22
C27
R32
C46
R45
R44
R39
R38
R40
C23
U5
C30
U6
C24
C25
R22
R23
R29
L3
C29
R24
R25
C26
R34
R17
R13
U2
R11
R12
C16
R10
C17
C15
C18
U3
C19
R9
R14
C20
R16
R15
U4
C21
R19
R20
R18
R21
C28
L2
U1
C2
L1
C1
CR3
CR2
R6
CR1
Q2
Q1
R7
R5
R4
R2
C9
R8
R1
Q3
C13
C8
R3
C3
C14
C6
C7
C12
C5
C4

NOTE:

[✱] INDICATES MOLDED JUMPER.

FIGURE 7-29
A16, LO/SHIFTER PC ASSEMBLY
#05710401 Rev $F_2$

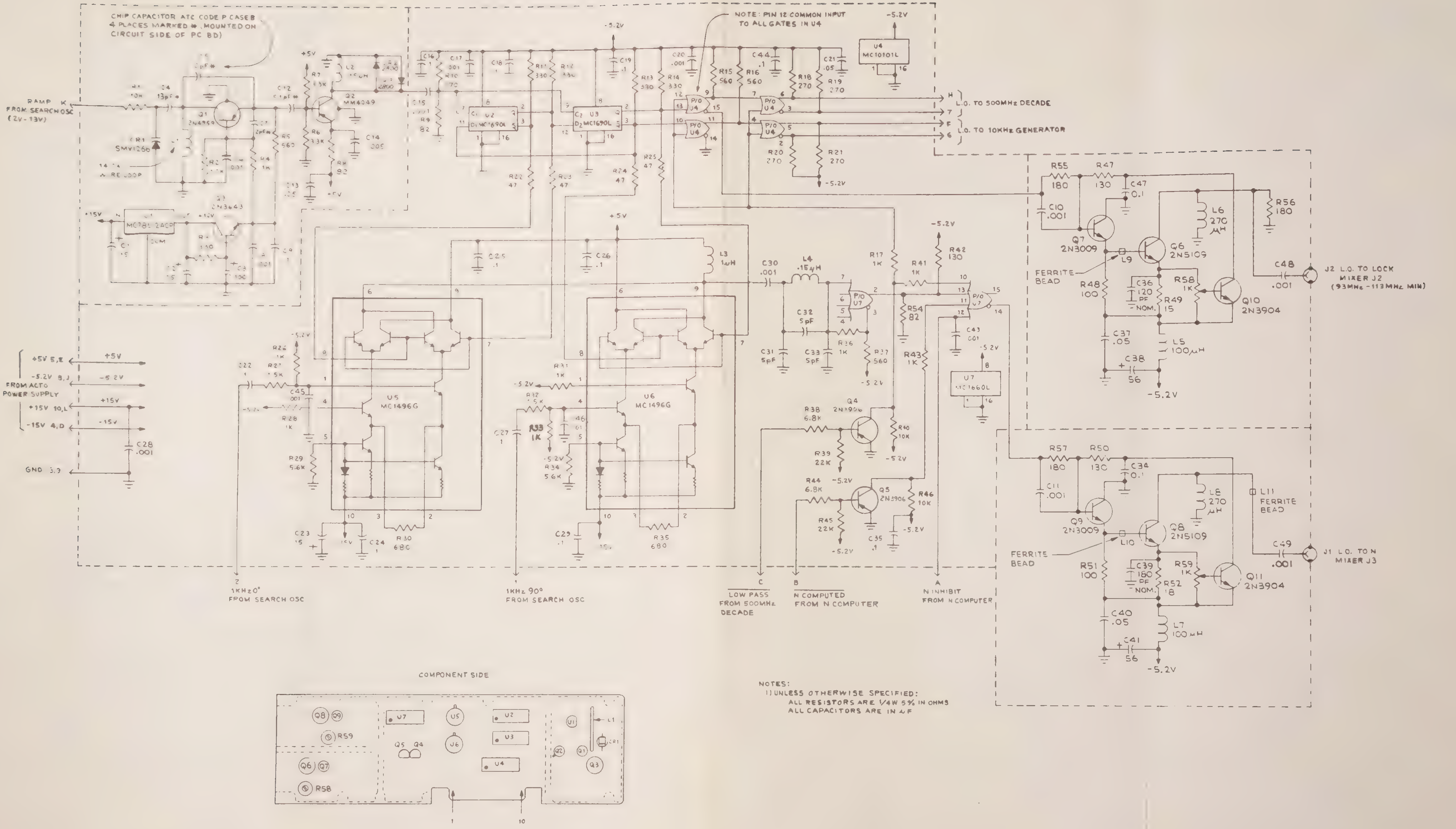

CHIP CAPACITOR ATC CODE P CASE B 4 PLACES MARKED ✱, MOUNTED ON CIRCUIT SIDE OF PC BD)
NOTE: PIN 12 COMMON INPUT TO ALL GATES IN U4
RAMP K FROM SEARCH OSC (2V-13V)
U4 MC10101L
L.O. TO 500MHz DECADE
L.O. TO 10KHz GENERATOR
Q1 2N4959
Q2 MM4049
Q3 2N3643
U1 MC78L12ACP
CR1 SMV1266
U2 MC1690L
U3 MC1690L
U5 MC1496G
U6 MC1496G
U7 MC1660L
Q4 2N3906
Q5 2N3906
Q6 2N5109
Q7 2N3009
Q8 2N5109
Q9 2N3009
Q10 2N3904
Q11 2N3904
FERRITE BEAD
J2 L.O. TO LOCK MIXER J2 (93MHz-113MHz MIN)
J1 L.O. TO N MIXER J3
+5V 5,E
-5.2V 9,J
FROM ACTO POWER SUPPLY
+15V 10,L
-15V 4,D
GND 3,7
1KHz 0° FROM SEARCH OSC
1KHz 90° FROM SEARCH OSC
LOW PASS FROM 500MHz DECADE
N COMPUTED FROM N COMPUTER
N INHIBIT FROM N COMPUTER
NOTES:
1) UNLESS OTHERWISE SPECIFIED:
ALL RESISTORS ARE 1/4W 5% IN OHMS
ALL CAPACITORS ARE IN µF
COMPONENT SIDE

FIGURE 7-30
A16, LO/SHIFTER SCHEMATIC
#7-05710401 Rev F₁

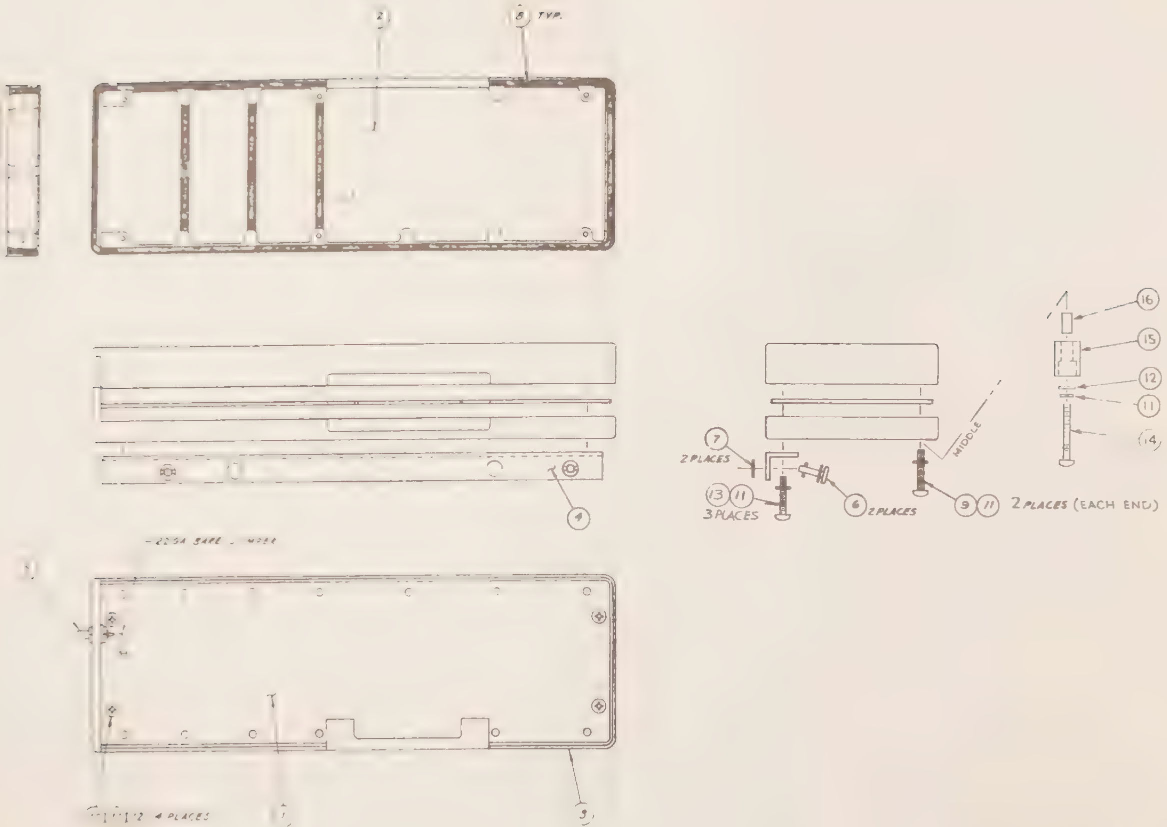

2
8 TYP.
1
4
7
2 PLACES
13
11
3 PLACES
6
2 PLACES
9
11
2 PLACES (EACH END)
MIDDLE
16
15
12
11
14
4 PLACES
3

FIGURE 7-31
A17, LOCK IF ACTO MODULE
ASSEMBLY #055367 Rev C

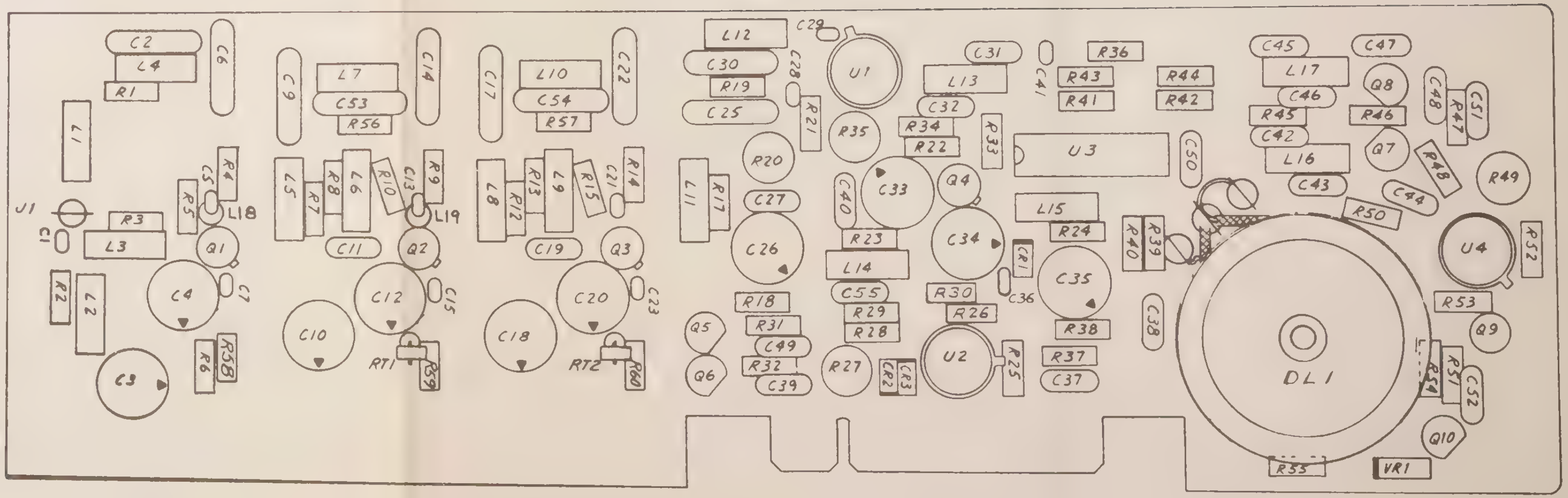
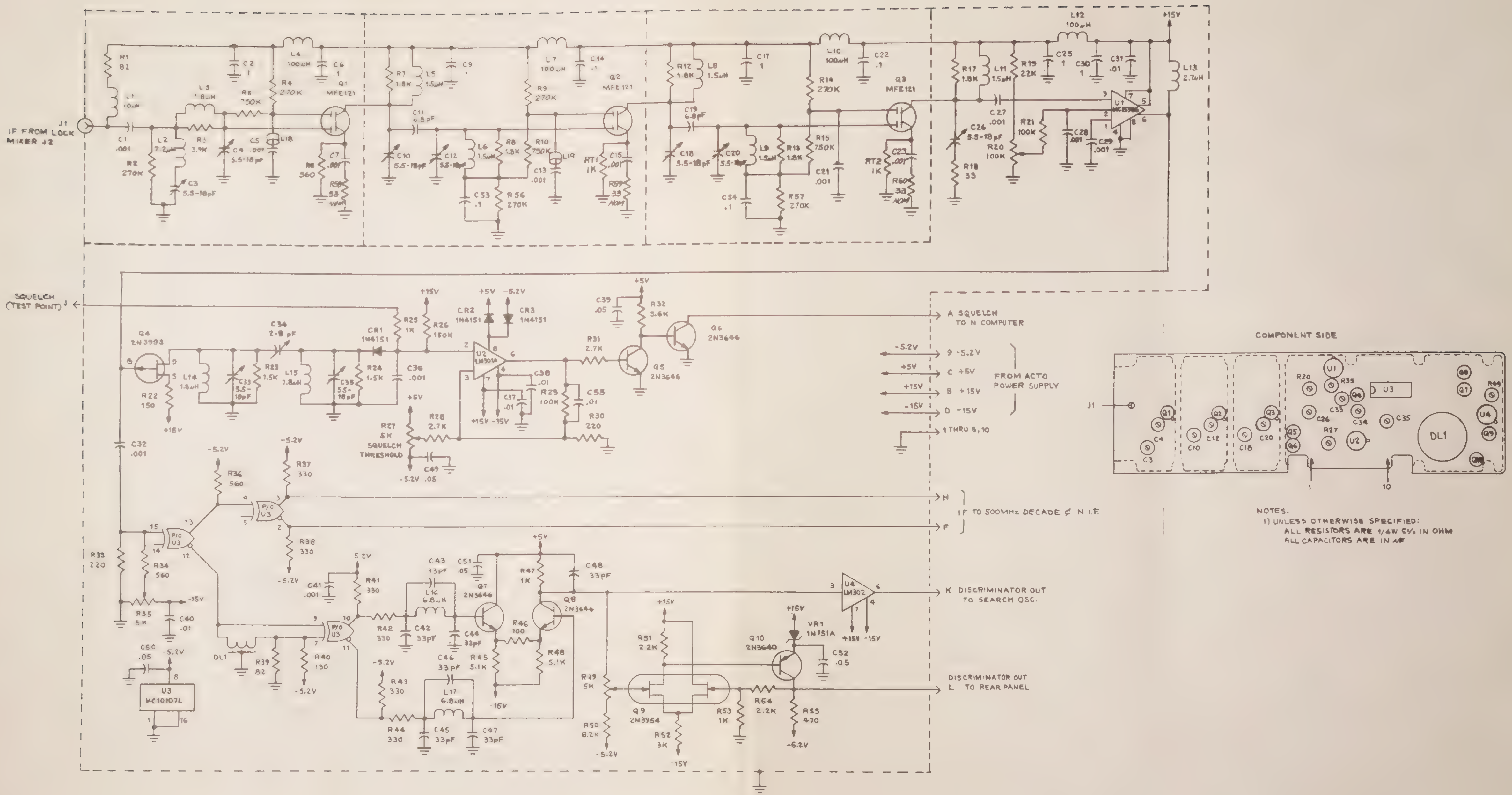

C2
L4
R1
C6
L1
J1
C1
R3
L3
R2
L2
C3
C4
C7
R4
C5
R5
L18
Q1
R58
R6
C9
L7
C53
R56
L5
R7
R8
L6
R10
C13
R9
L19
C11
Q2
C14
C10
C12
C15
RT1
R59
C17
L10
C54
R57
C22
L8
R12
R13
L9
R15
C21
R14
C19
Q3
C18
C20
C23
RT2
R60
L12
C29
C30
C28
R19
C25
R21
U1
L11
R17
R20
C27
C26
Q5
Q6
R18
R31
C49
R32
C39
R27
CR2
CR3
R35
C40
C33
Q4
C31
L13
C32
R34
R22
R33
C41
R36
R43
R41
R44
R42
U3
C50
L15
R24
R40
R39
C34
CR1
R23
L14
C55
R29
R28
R30
R26
C36
U2
R25
C35
R38
R37
C37
C38
C45
C47
L17
C46
R45
C42
L16
C43
Q8
C48
R47
C51
R46
Q7
R48
C44
R49
R50
U4
R52
R53
Q9
DL1
R54
R51
C52
Q10
R55
VR1

FIGURE 7-32
A17, LOCK IF PC ASSEMBLY
#05321801 Rev $D_1$


J1
IF FROM LOCK MIXER J2
SQUELCH (TEST POINT)
A SQUELCH TO N COMPUTER
9 -5.2V
C +5V
B +15V
D -15V
FROM ACTO POWER SUPPLY
1 THRU 8, 10
IF TO 500MHz DECADE ⊄ N I.F.
H
F
K DISCRIMINATOR OUT TO SEARCH OSC.
DISCRIMINATOR OUT L TO REAR PANEL
Q1 MFE121
Q2 MFE121
Q3 MFE121
U1 MC1590G
Q4 2N3993
U2 LM301A
Q5 2N3646
Q6 2N3646
Q7 2N3646
Q8 2N3646
Q9 2N3954
Q10 2N3640
U3 MC10107L
U4 LM302
VR1 1N751A
CR1 1N4151
CR2 1N4151
CR3 1N4151
DL1
R27 5K SQUELCH THRESHOLD
+15V
+5V
-5.2V
-15V
-6.2V
COMPONENT SIDE

NOTES:
1) UNLESS OTHERWISE SPECIFIED:
ALL RESISTORS ARE 1/4W 5% IN OHM
ALL CAPACITORS ARE IN µF

FIGURE 7-33
A17, LOCK IF SCHEMATIC
#7-05321801 Rev C

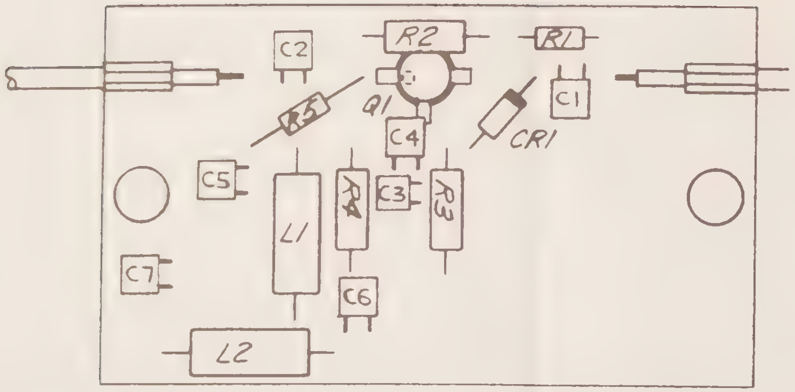
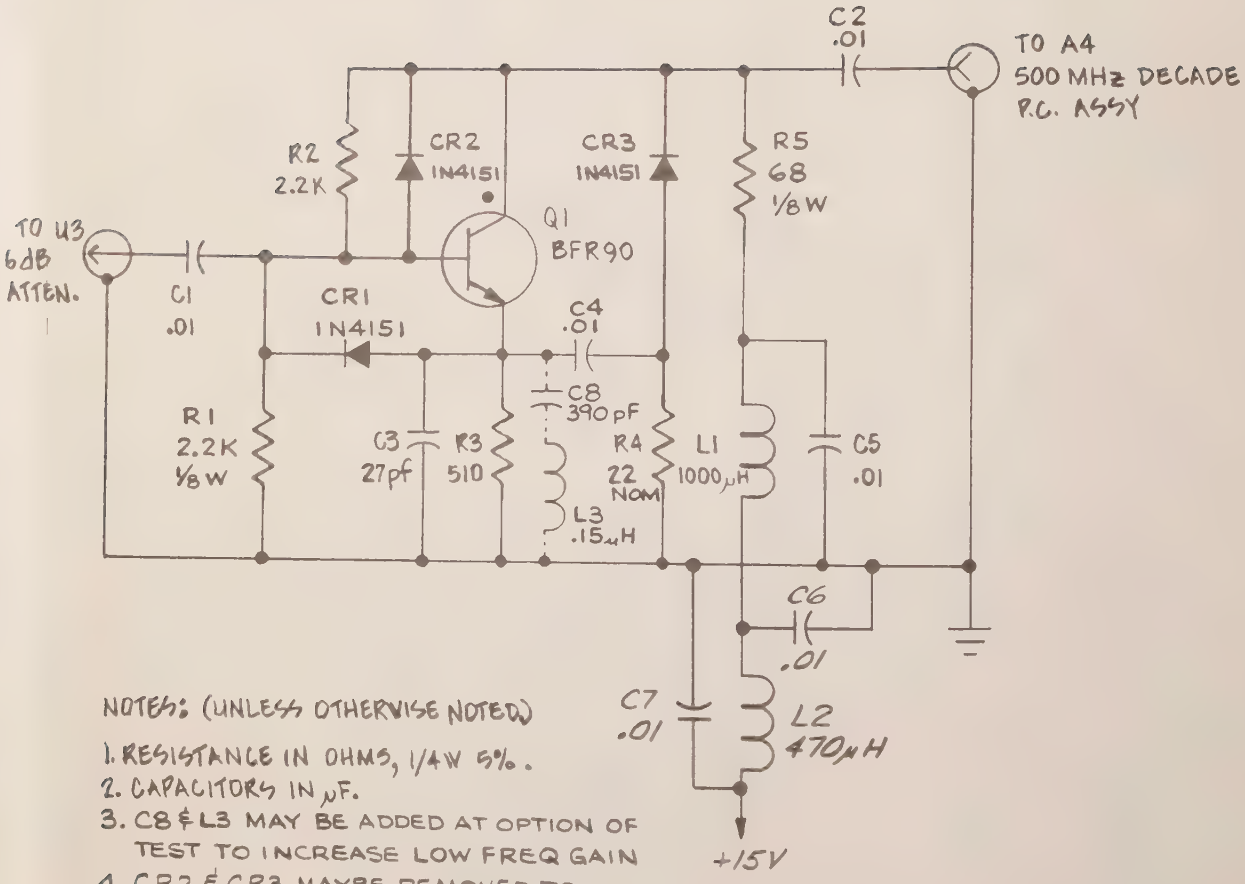

C2
R2
R1
Q1
R5
C1
C4
CR1
C5
L1
R4
C3
R3
C7
C6
L2

FIGURE 7-34
A22, 500 MHz PRE AMP PC ASSEMBLY
#06748401 Rev E


C2
.01
TO A4
500 MHz DECADE
P.C. ASSY
R2
2.2K
CR2
1N4151
CR3
1N4151
R5
68
1/8 W
Q1
BFR90
TO U3
6dB
ATTEN.
C1
.01
CR1
1N4151
C4
.01
C8
390 pF
R1
2.2K
1/8 W
C3
27pf
R3
510
R4
22
NOM
L1
1000 μH
C5
.01
L3
.15 μH
C6
.01
C7
.01
L2
470 μH
+15V

NOTES: (UNLESS OTHERWISE NOTED)

1. RESISTANCE IN OHMS, 1/4 W 5%.
2. CAPACITORS IN μF.
3. C8 & L3 MAY BE ADDED AT OPTION OF TEST TO INCREASE LOW FREQ GAIN
4. CR2 & CR3 MAYBE REMOVED TO INCREASE HF GAIN AT OPTION OF TEST (TEST CHECK FOR HF OSCILLATION IF DIODE REMOVED)

FIGURE 7-35
A22, 500 MHz PRE AMP SCHEMATIC
#7-06748401 Rev E

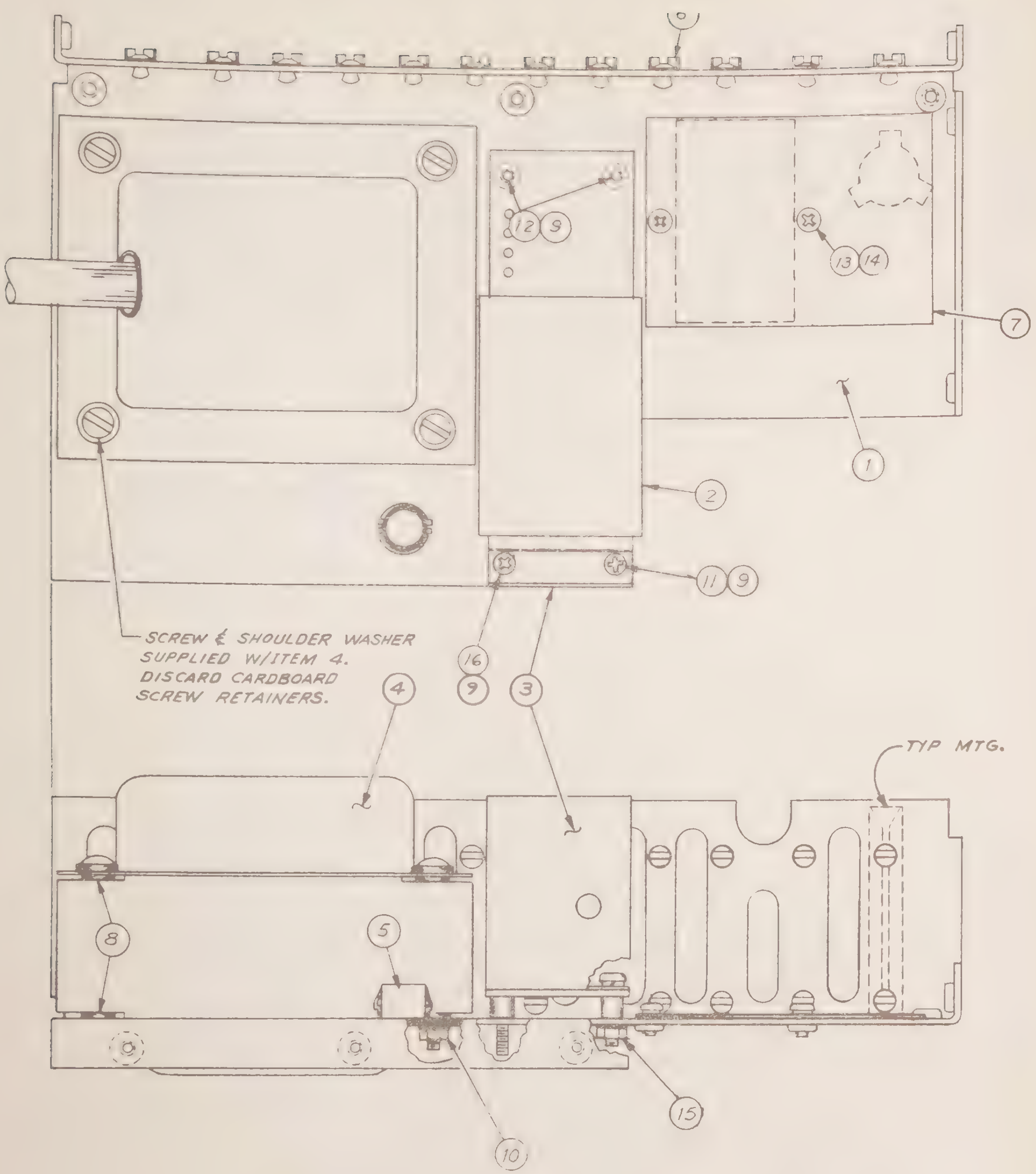

12
9
13
14
7
1
2
11
9
SCREW & SHOULDER WASHER
SUPPLIED W/ITEM 4.
DISCARD CARDBOARD
SCREW RETAINERS.
16
9
3
4
TYP MTG.
8
5
15
10

FIGURE 7-36
TRANSFORMER CHASSIS ASSEMBLY
#055116 Rev B₂

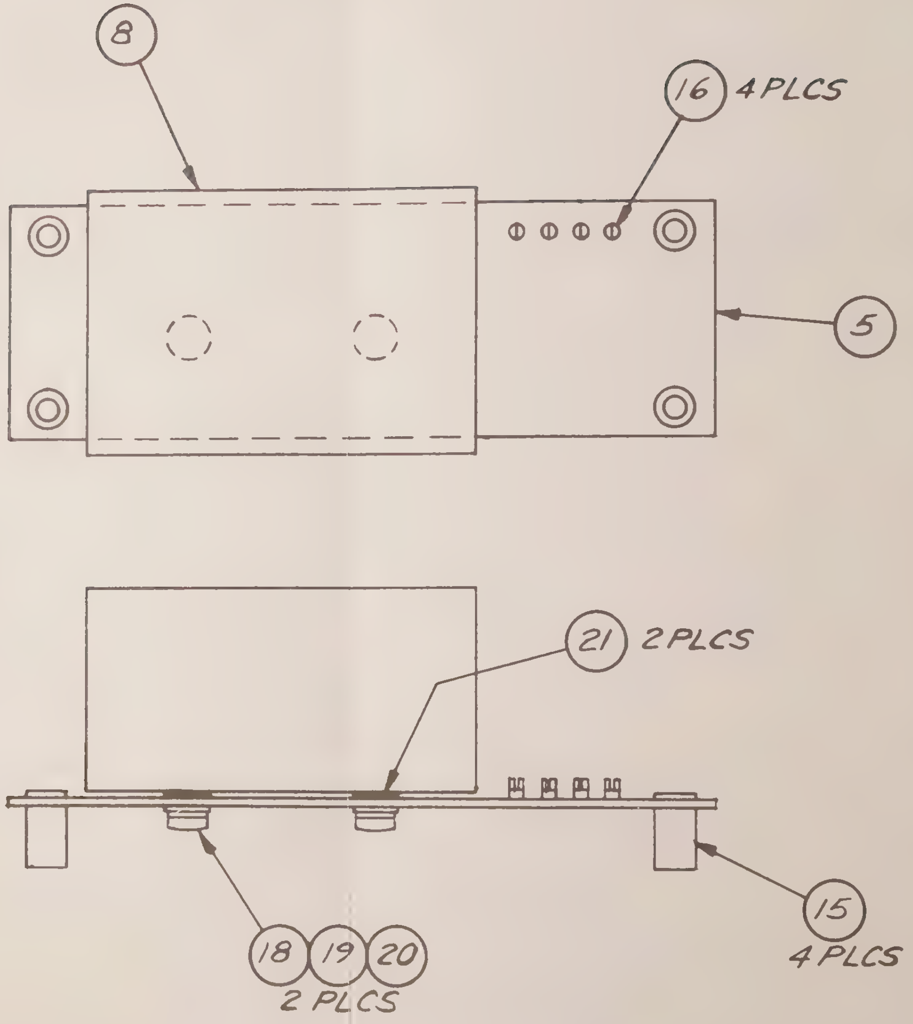

8
16 4 PLCS
5
21 2 PLCS
18
19
20
2 PLCS
15
4 PLCS

FIGURE 7-37
TIMEBASE OSCILLATOR ASSEMBLY
#06738201 Rev A

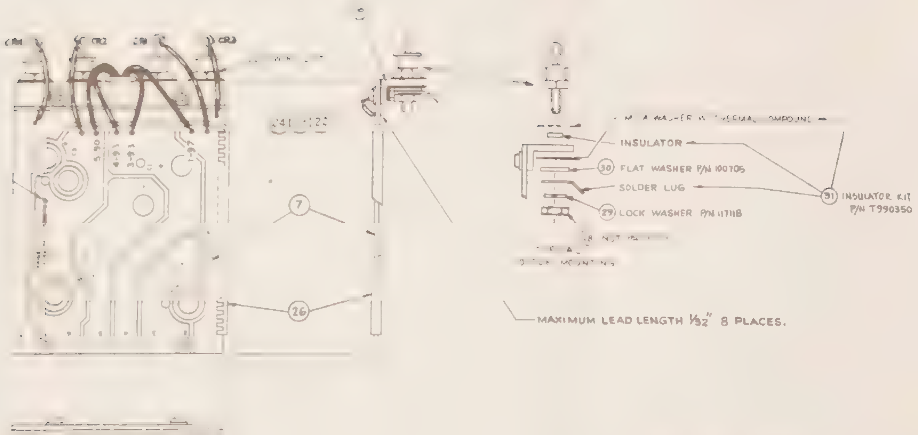

CR4
CR2
CR1
CR3
5-90
4-91
3-93
1-97
7
26
INSULATOR
30 FLAT WASHER P/N 100705
SOLDER LUG
29 LOCK WASHER P/N 11711B
31 INSULATOR KIT P/N T990350
MAXIMUM LEAD LENGTH 1/32" 8 PLACES.

FIGURE 7-38

DIODE ASSEMBLY #05389001 Rev A

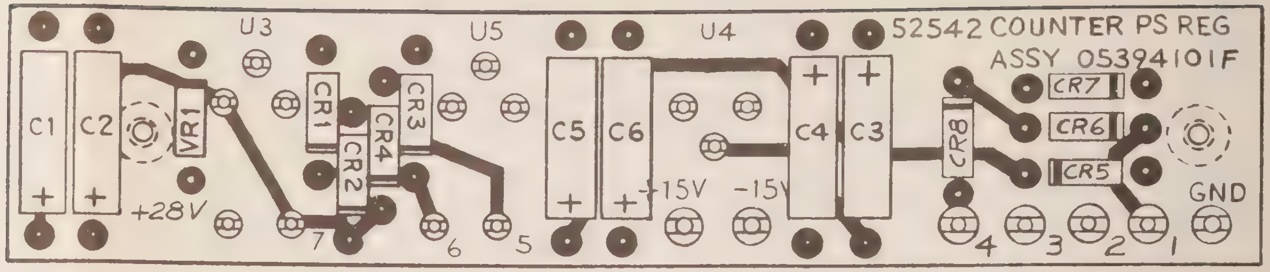

52542 COUNTER PS REG
ASSY 05394101F
U3
U5
U4
C1
C2
VR1
CR1
CR2
CR3
CR4
C5
C6
C4
C3
CR8
CR7
CR6
CR5
+28V
+15V
-15V
GND
7
6
5
4
3
2
1

FIGURE 7-39
A23, COUNTER PS REGULATOR
PC ASSEMBLY #05394101 Rev C

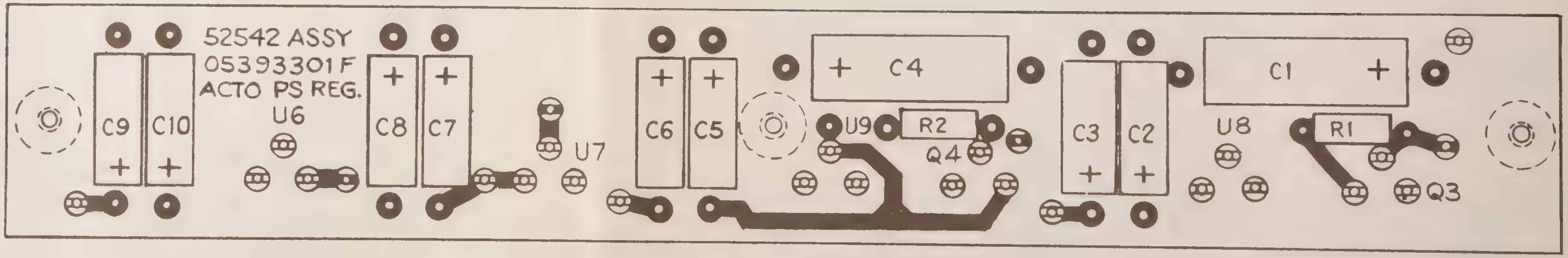

52542 ASSY
05393301F
ACTO PS REG.
U6
C9
C10
C8
C7
U7
C6
C5
C4
U9
R2
Q4
C3
C2
U8
C1
R1
Q3

FIGURE 7-40
A13, ACTO PS REGULATOR
PC ASSEMBLY #05393301 Rev C

NOTE:
1) RESISTORS 1/4 W, 5%.
2) CAPACITOR VALUES IN μF.
3) C5, T2 & U3 ARE P/O HIGH STABILITY OSCILLATOR OPTIONS 11, 12 OR 13.

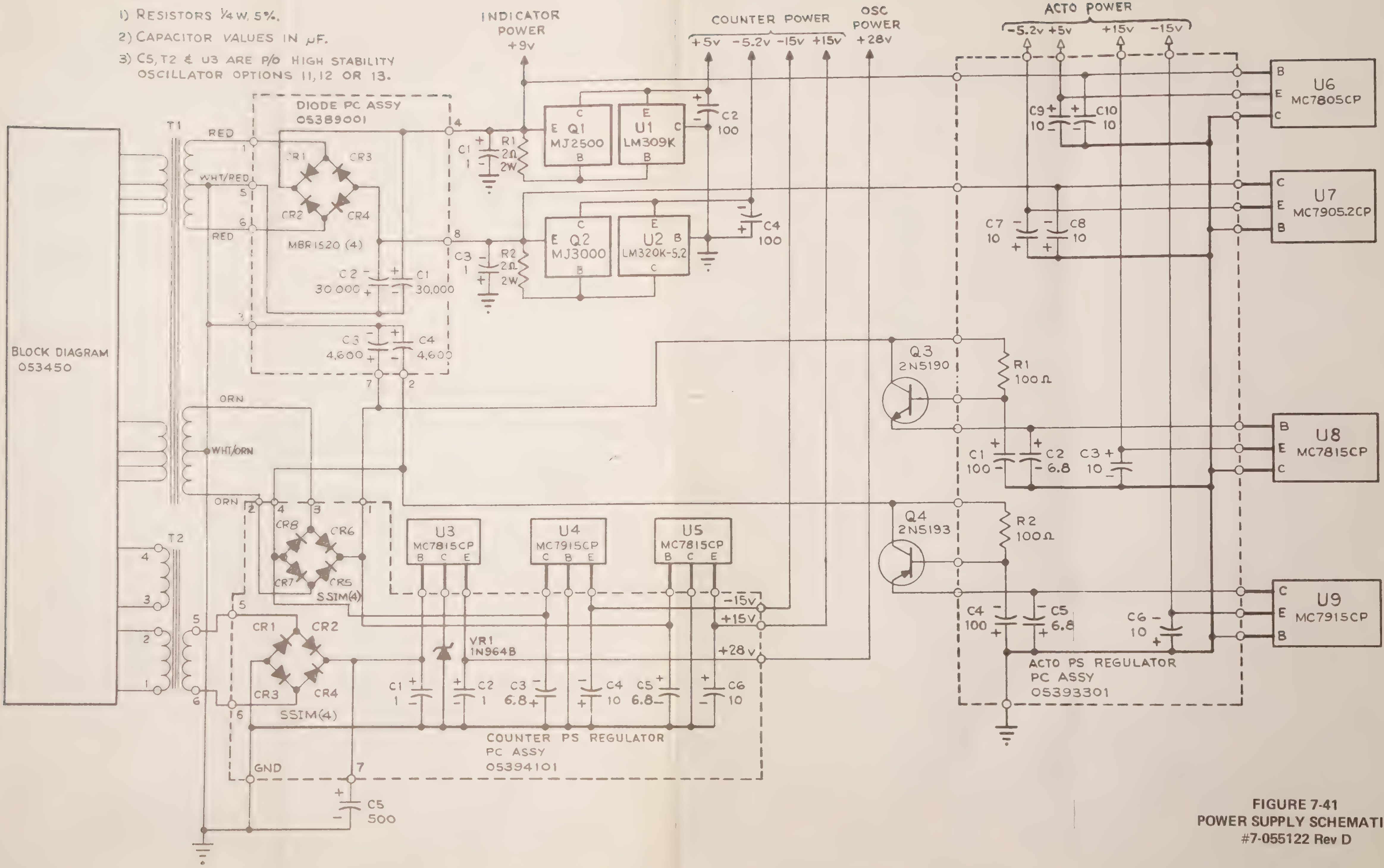

INDICATOR POWER +9v
COUNTER POWER
+5v -5.2v -15v +15v
OSC POWER +28v
ACTO POWER
-5.2v +5v +15v -15v
BLOCK DIAGRAM 053450
T1
RED
WHT/RED
RED
ORN
WHT/ORN
ORN
T2
DIODE PC ASSY 05389001
CR1 CR3 CR2 CR4
MBR1520 (4)
C2 30,000
C1 30,000
C3 4,600
C4 4,600
C1 1
R1 2Ω 2W
C3 1
R2 2Ω 2W
Q1 MJ2500
U1 LM309K
C2 100
Q2 MJ3000
U2 LM320K-5.2
C4 100
CR8 CR6 CR7 CR5
SSIM(4)
CR1 CR2 CR3 CR4
SSIM(4)
U3 MC7815CP
U4 MC7915CP
U5 MC7815CP
VR1 1N964B
C1 1
C2 1
C3 6.8
C4 10
C5 6.8
C6 10
-15v
+15v
+28v
COUNTER PS REGULATOR PC ASSY 05394101
GND
C5 500
Q3 2N5190
R1 100Ω
C1 100
C2 6.8
C3 10
Q4 2N5193
R2 100Ω
C4 100
C5 6.8
C6 10
U6 MC7805CP
C9 10
C10 10
U7 MC7905.2CP
C7 10
C8 10
U8 MC7815CP
U9 MC7915CP
ACTO PS REGULATOR PC ASSY 05393301

FIGURE 7-41
POWER SUPPLY SCHEMATIC
#7-055122 Rev D

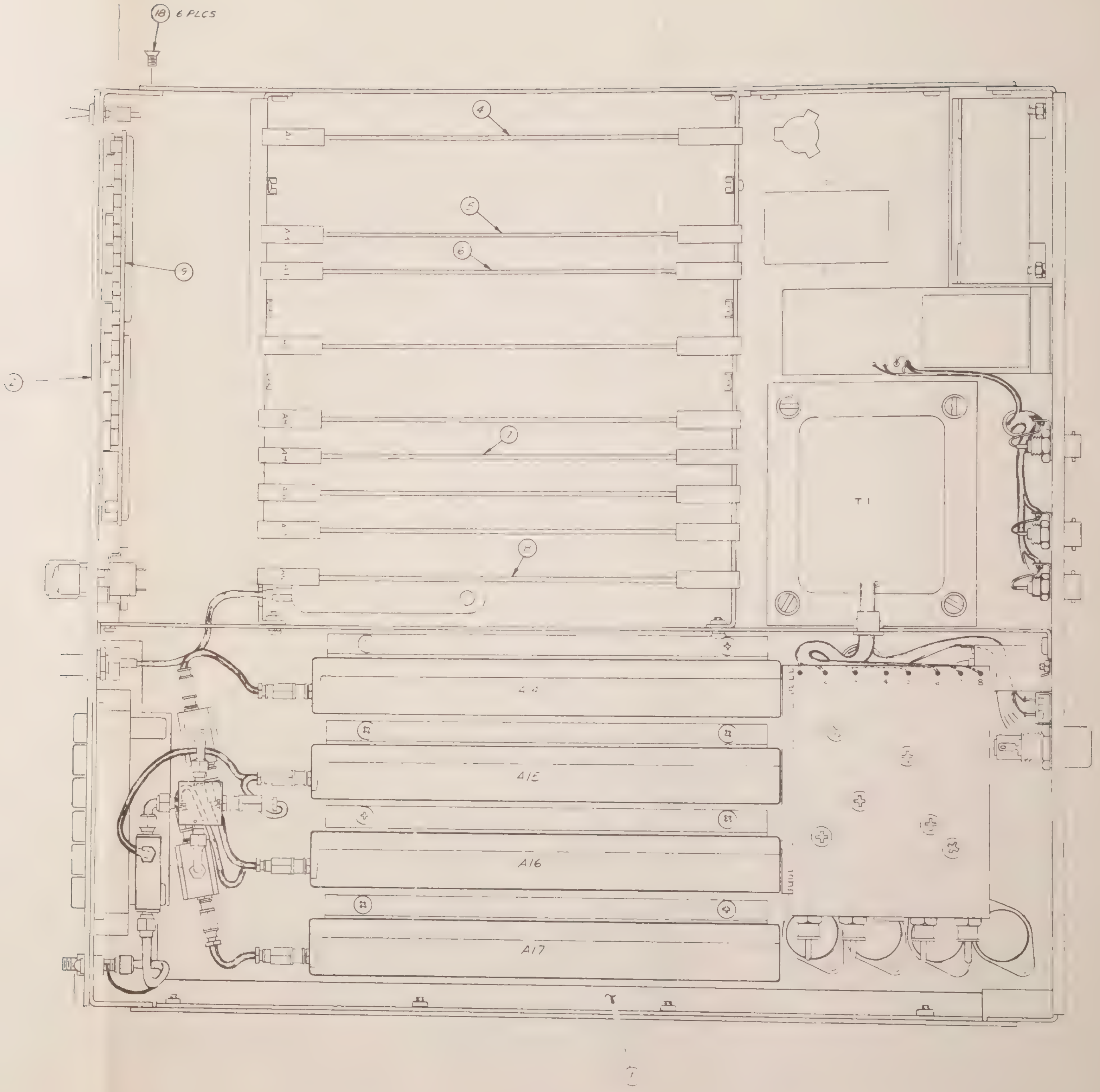
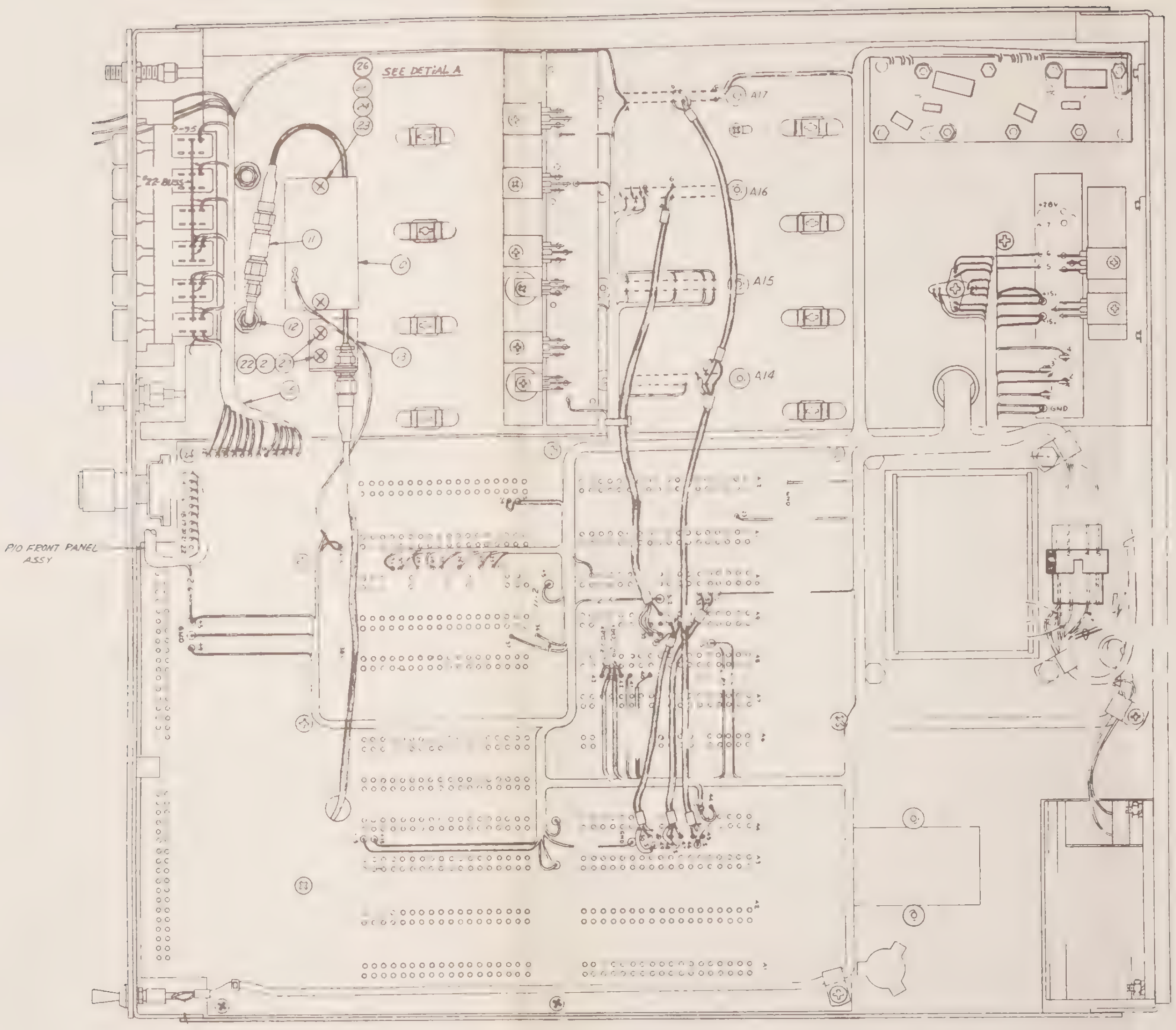

18
6 PLCS
4
5
6
9
7
T1
A15
A16
A17

FIGURE 7-42
TEST ASSEMBLY
#057164 Rev $M_2$ (Sheet 1 of 2)


SEE DETIAL A
26
24
23
9-75
22 BUSS
11
C
12
13
22
2
21
A17
A16
A15
A14
+28V
GND
P10 FRONT PANEL ASSY

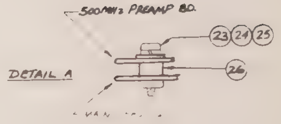
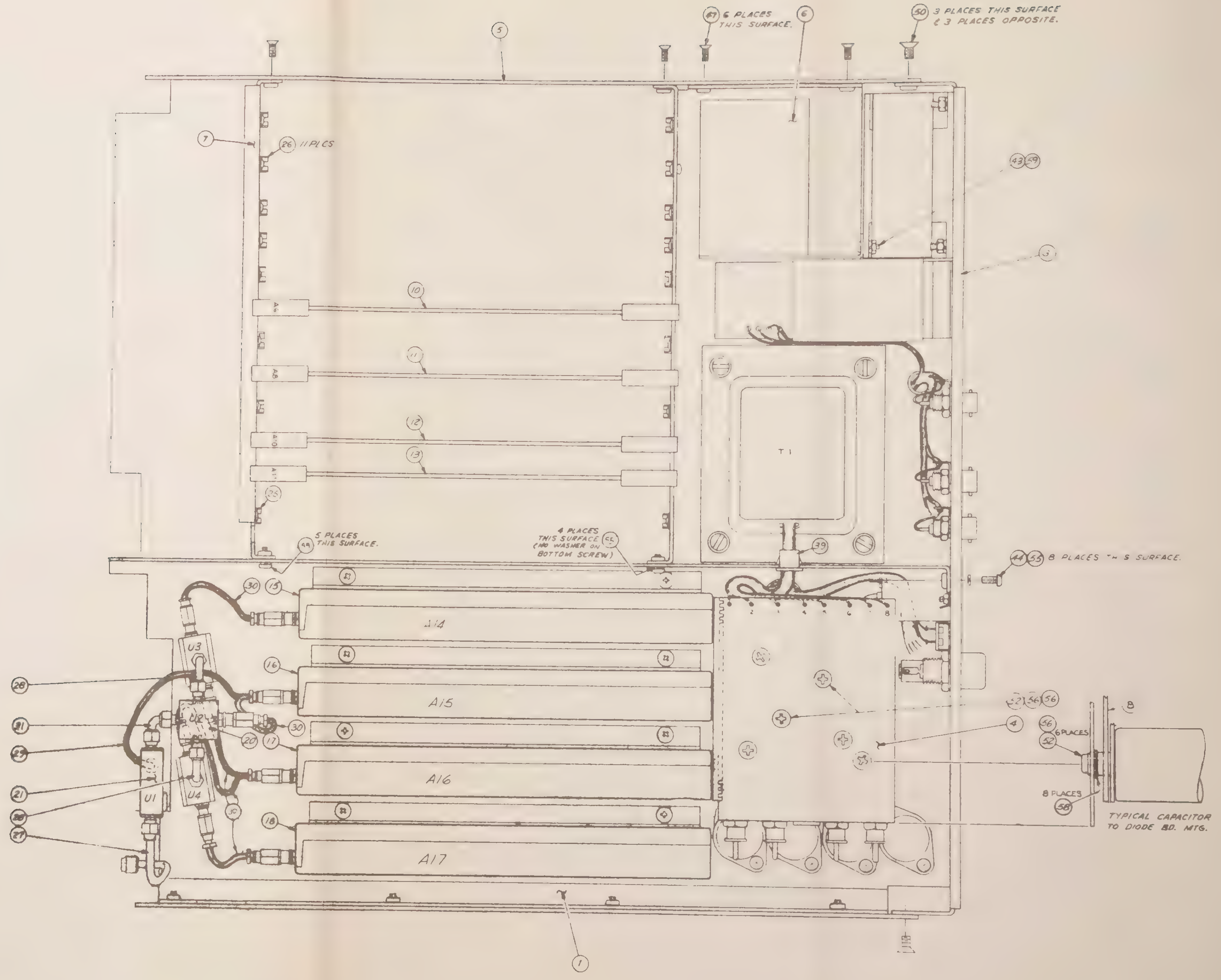

500MHz PREAMP BD.
23
24
25
26
DETAIL A

FIGURE 7-42
TEST ASSEMBLY
#057164 Rev $M_2$ (Sheet 2 of 2)



5
47 6 PLACES THIS SURFACE.
6
50 3 PLACES THIS SURFACE & 3 PLACES OPPOSITE.
7
26 11 PLCS
43 59
3
10
A6
11
A8
12
A10
13
A11
25
T1
5 PLACES THIS SURFACE.
49
4 PLACES THIS SURFACE (NO WASHER ON BOTTOM SCREW)
55
39
44 55 8 PLACES THIS SURFACE.
30
15
A14
U3
16
A15
28
31
U2
30
20
17
29
A16
21
U1
U4
26
27
30
18
A17
52 56 56
8
4
56
6 PLACES
52
8 PLACES
58
TYPICAL CAPACITOR TO DIODE BD. MTG.
1

FIGURE 7-43
UNIVERSAL CHASSIS ASSEMBLY
#057496 Rev H (Sheet 1 of 2)

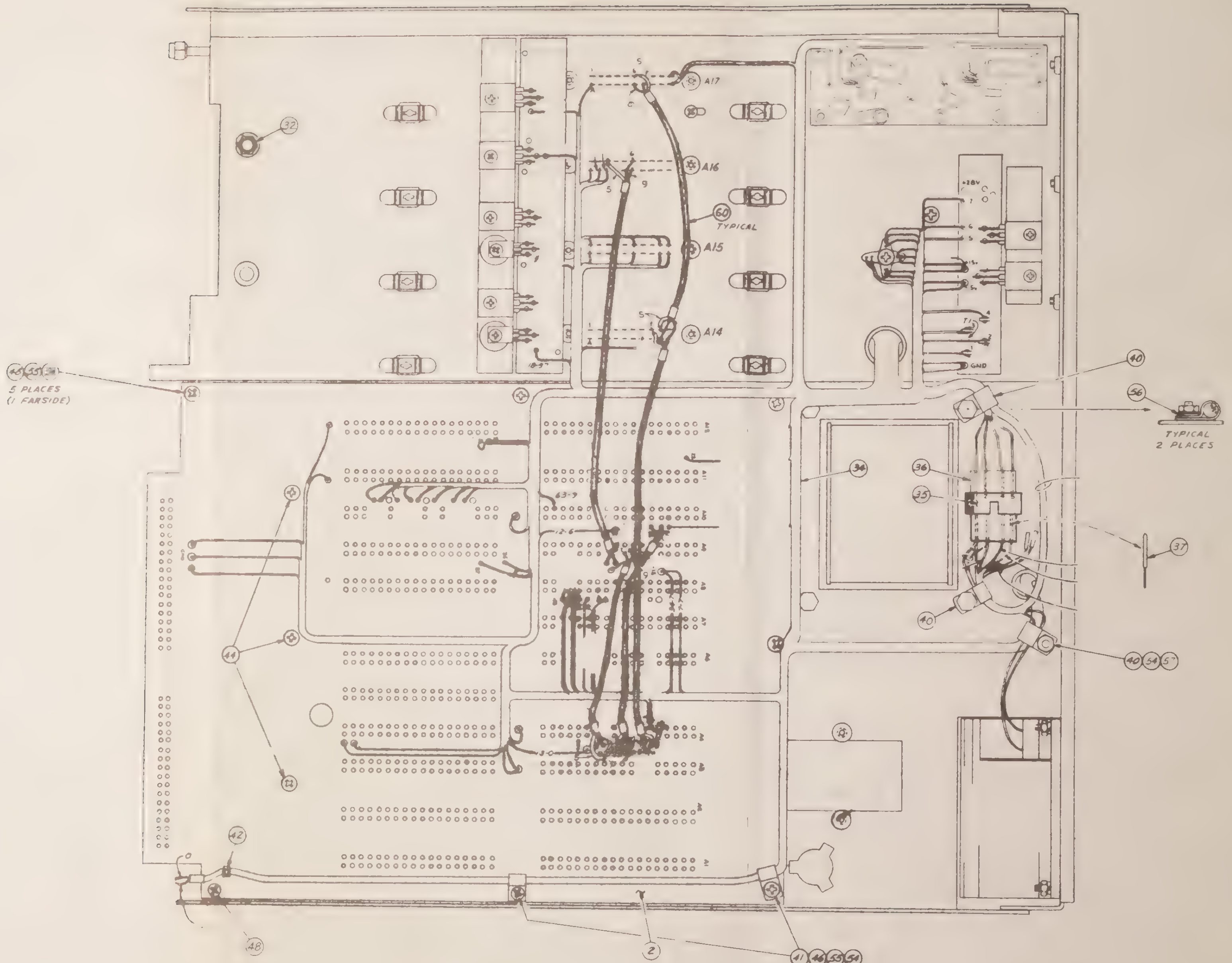

32
A17
A16
60
TYPICAL
A15
A14
45
55
5 PLACES
(1 FARSIDE)
40
56
TYPICAL
2 PLACES
34
36
35
37
40
40
54
57
44
42
48
2
41
46
55
54
+28V
GND

FIGURE 7-43
UNIVERSAL CHASSIS ASSEMBLY
#057496 Rev H (Sheet 2 of 2)

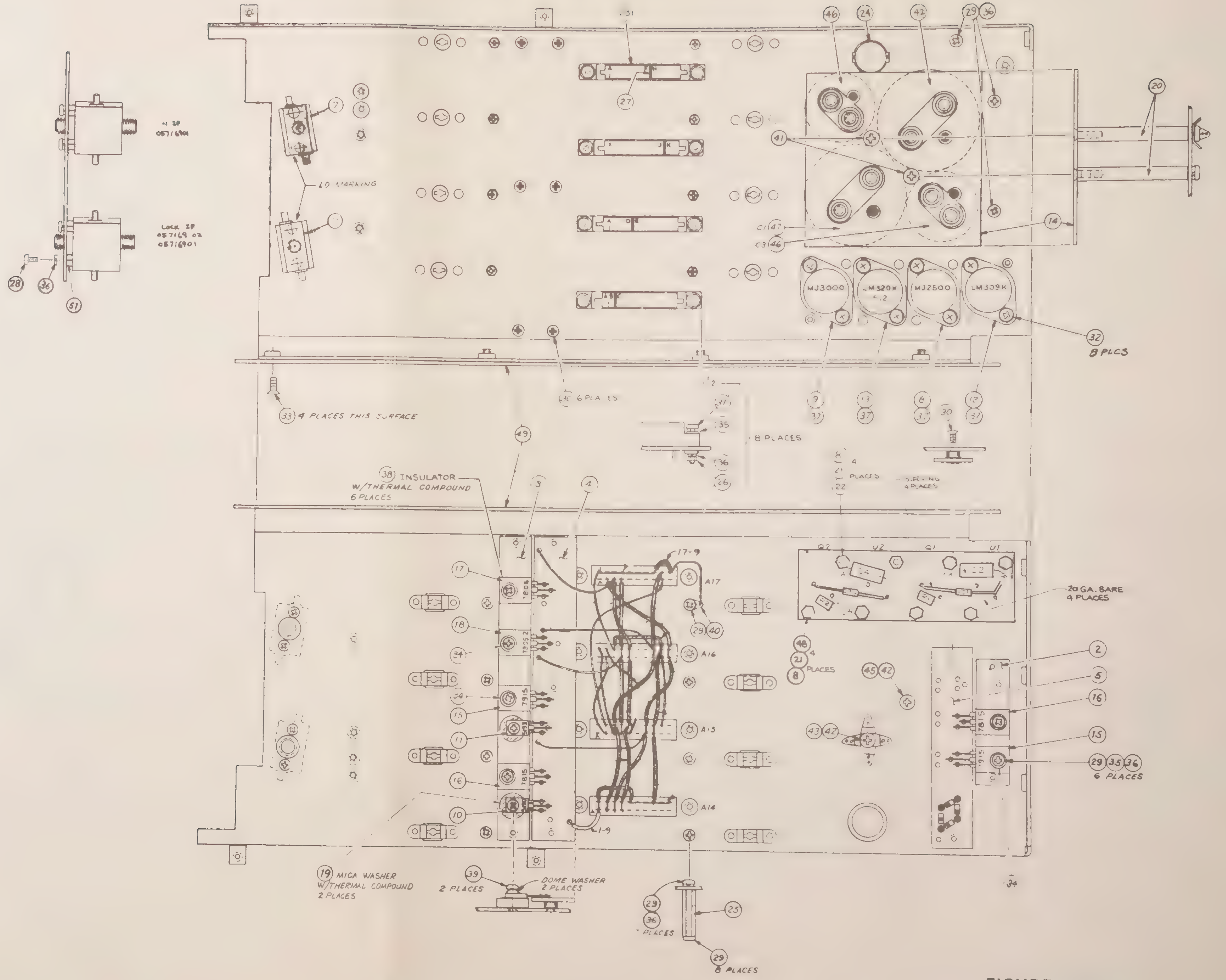
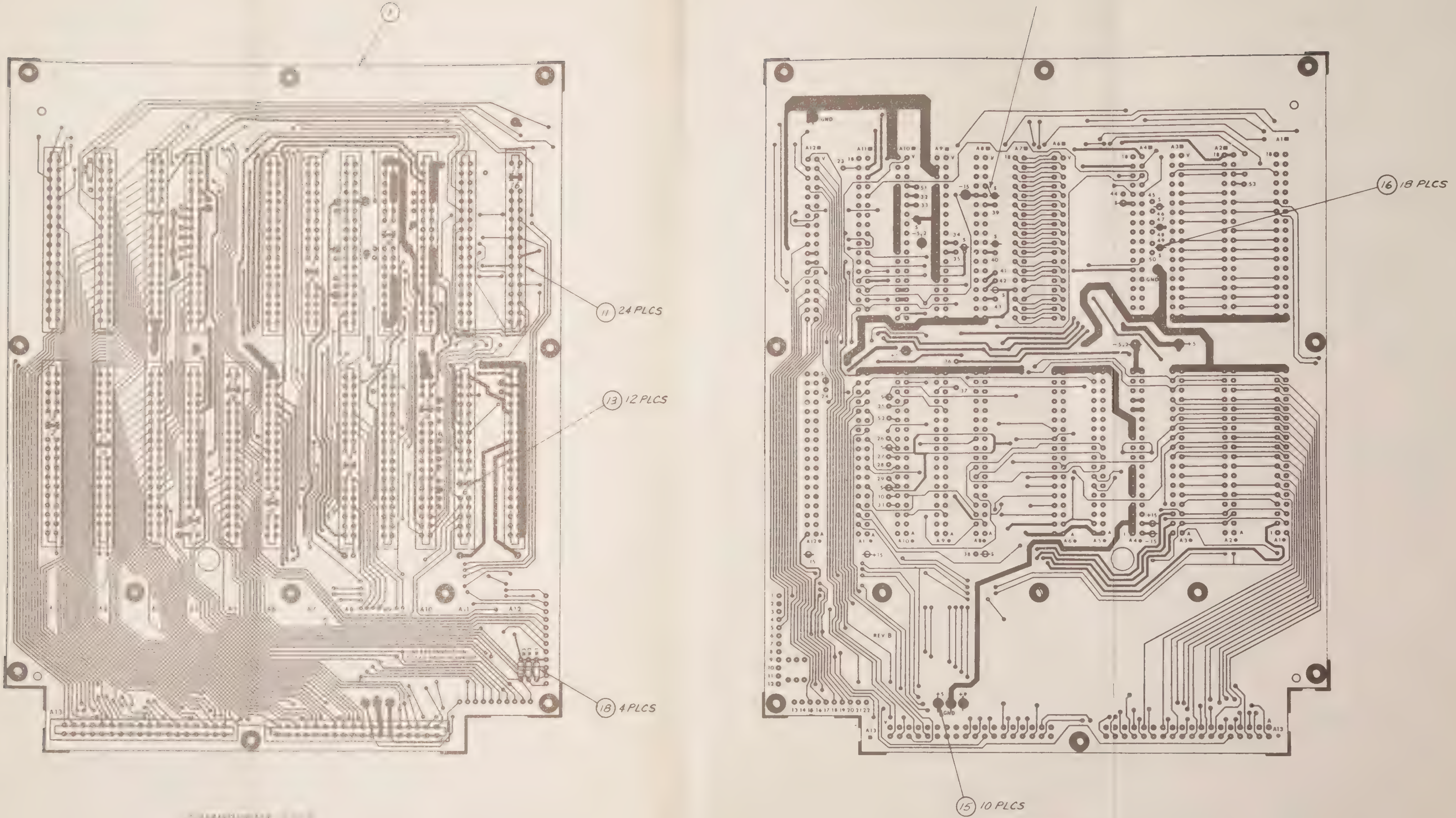

N IF
0571 6901
LOCK IF
057169 02
05716901
28
36
51
7
LO MARKING
31
27
46
24
42
29
36
20
41
C1 47
C3 46
14
MJ3000
LM320K
MJ2500
LM309K
32
8 PLCS
33 4 PLACES THIS SURFACE
30 6 PLACES
12
37
35
8 PLACES
36
26
9
37
13
37
8
37
30
12
37
8
21
22
4 PLACES
SLEEVING 4 PLACES
49
38 INSULATOR W/THERMAL COMPOUND 6 PLACES
3
4
17-9
A17
Q2
U2
Q1
U1
20 GA. BARE 4 PLACES
17
7806
18
7905
34
7915
34
15
11
7815
16
10
29
40
A16
48
21 4 PLACES
8
45
42
2
5
16
15
A15
43
42
7815
7915
29 35 36 6 PLACES
A14
1-9
19 MICA WASHER W/THERMAL COMPOUND 2 PLACES
39 2 PLACES
DOME WASHER 2 PLACES
29
36
PLACES
25
29
8 PLACES
34

FIGURE 7-44
MAIN CHASSIS ASSEMBLY
#057163 Rev J


①
⑪ 24 PLCS
⑬ 12 PLCS
⑱ 4 PLCS
⑯ 18 PLCS
⑮ 10 PLCS
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
A12
A13
GND
REV B

COMPONENT SIDE

CIRCUIT SIDE

FIGURE 7-45
INTERCONNECT PC BOARD
ASSEMBLY #05344001 Rev C

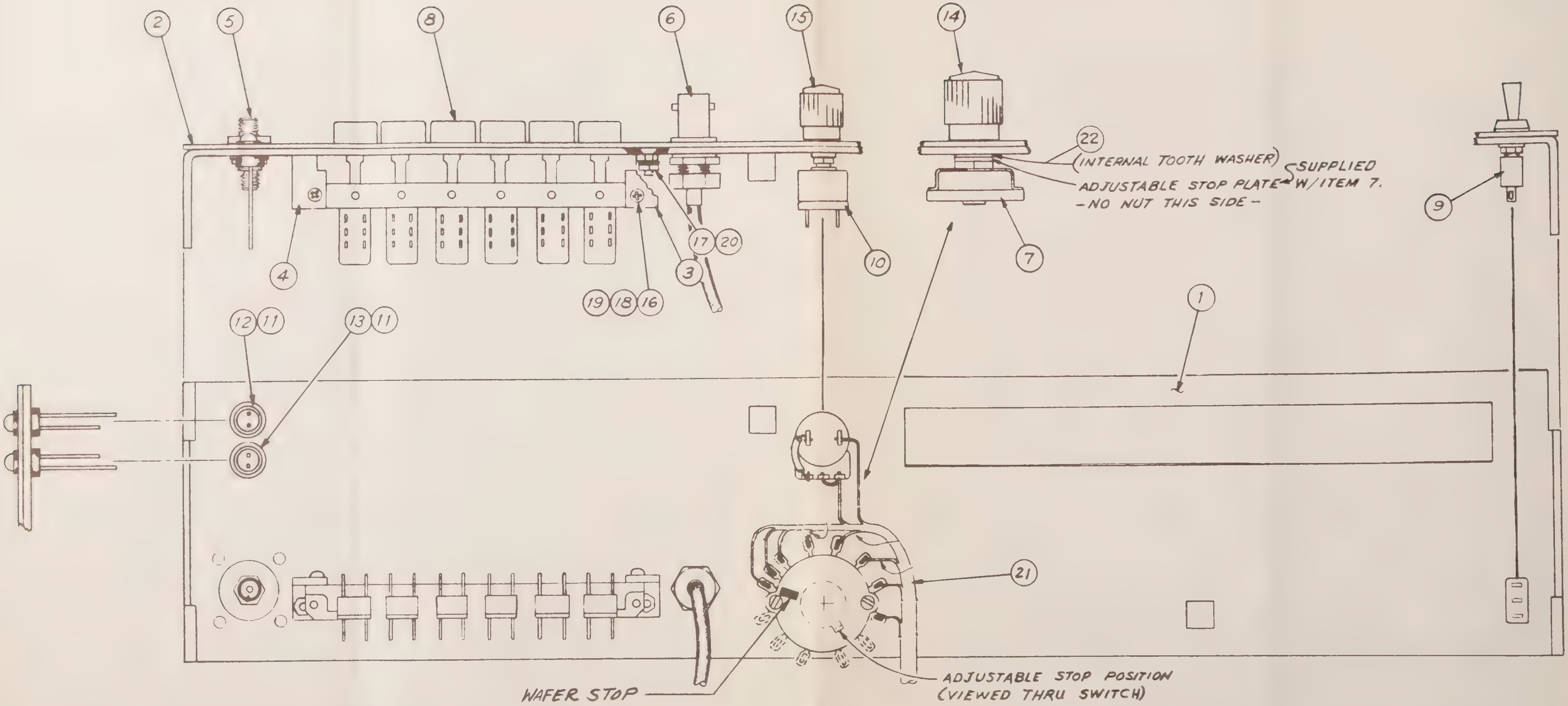

2
5
8
6
15
14
22
(INTERNAL TOOTH WASHER)
SUPPLIED W/ITEM 7.
ADJUSTABLE STOP PLATE
-NO NUT THIS SIDE-
9
4
3
17
20
10
7
19
18
16
1
12
11
13
11
21
WAFER STOP
ADJUSTABLE STOP POSITION
(VIEWED THRU SWITCH)

FIGURE 7-46
FRONT PANEL ASSEMBLY
#057162 Rev C

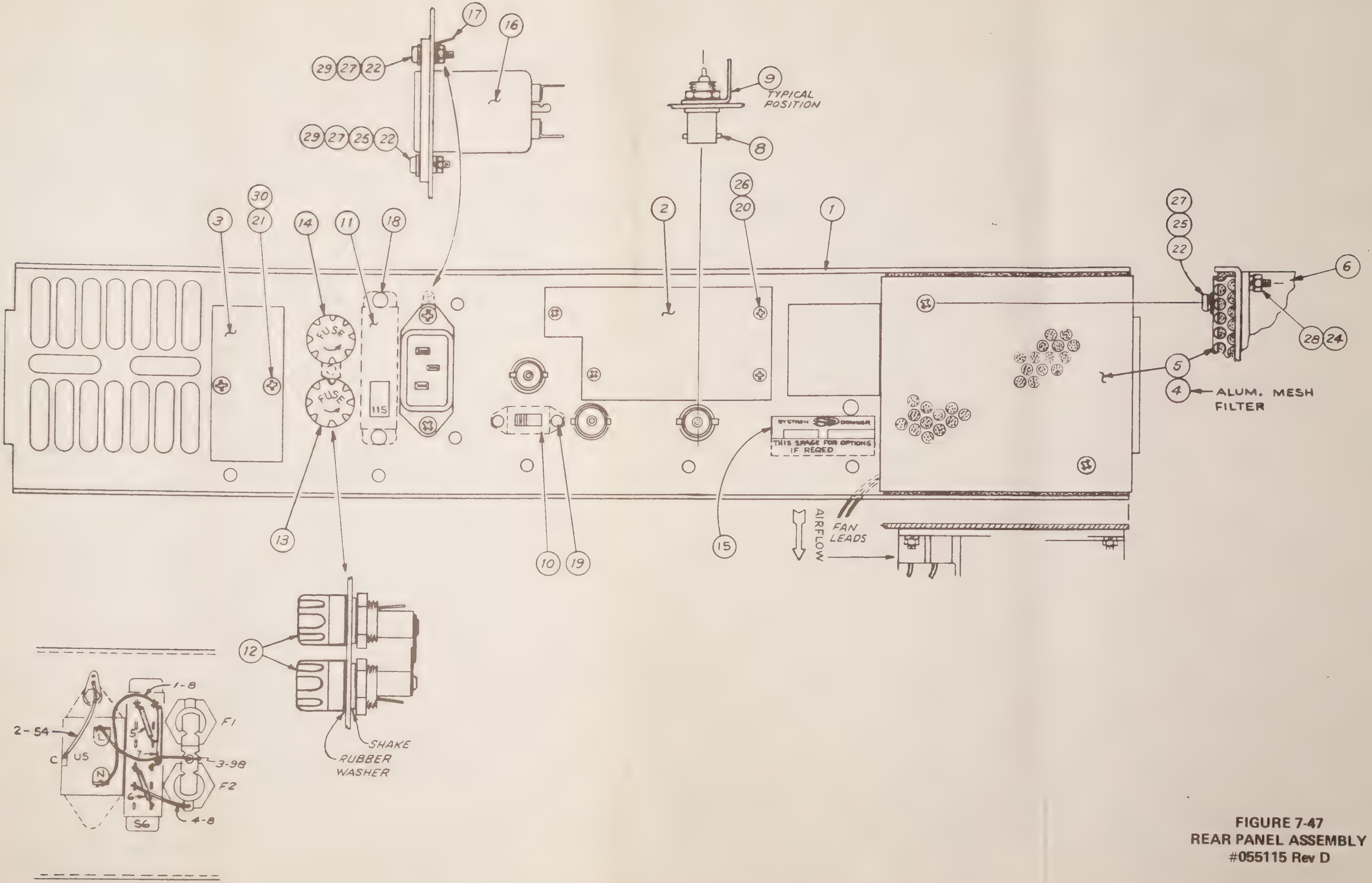

17
16
29 27 22
29 27 25 22
9
TYPICAL POSITION
8
30
21
3
14
11
18
2
26
20
1
27
25
22
6
28 24
5
4
ALUM. MESH FILTER
FUSE
FUSE
115
SYSTRON DONNER
THIS SPACE FOR OPTIONS IF REQED
13
10
19
15
AIRFLOW
FAN LEADS
12
SHAKE
RUBBER WASHER
1-8
2-54
L
5
C
US
7
3-98
N
6
4-8
F1
F2
S6

FIGURE 7-47
REAR PANEL ASSEMBLY
#055115 Rev D

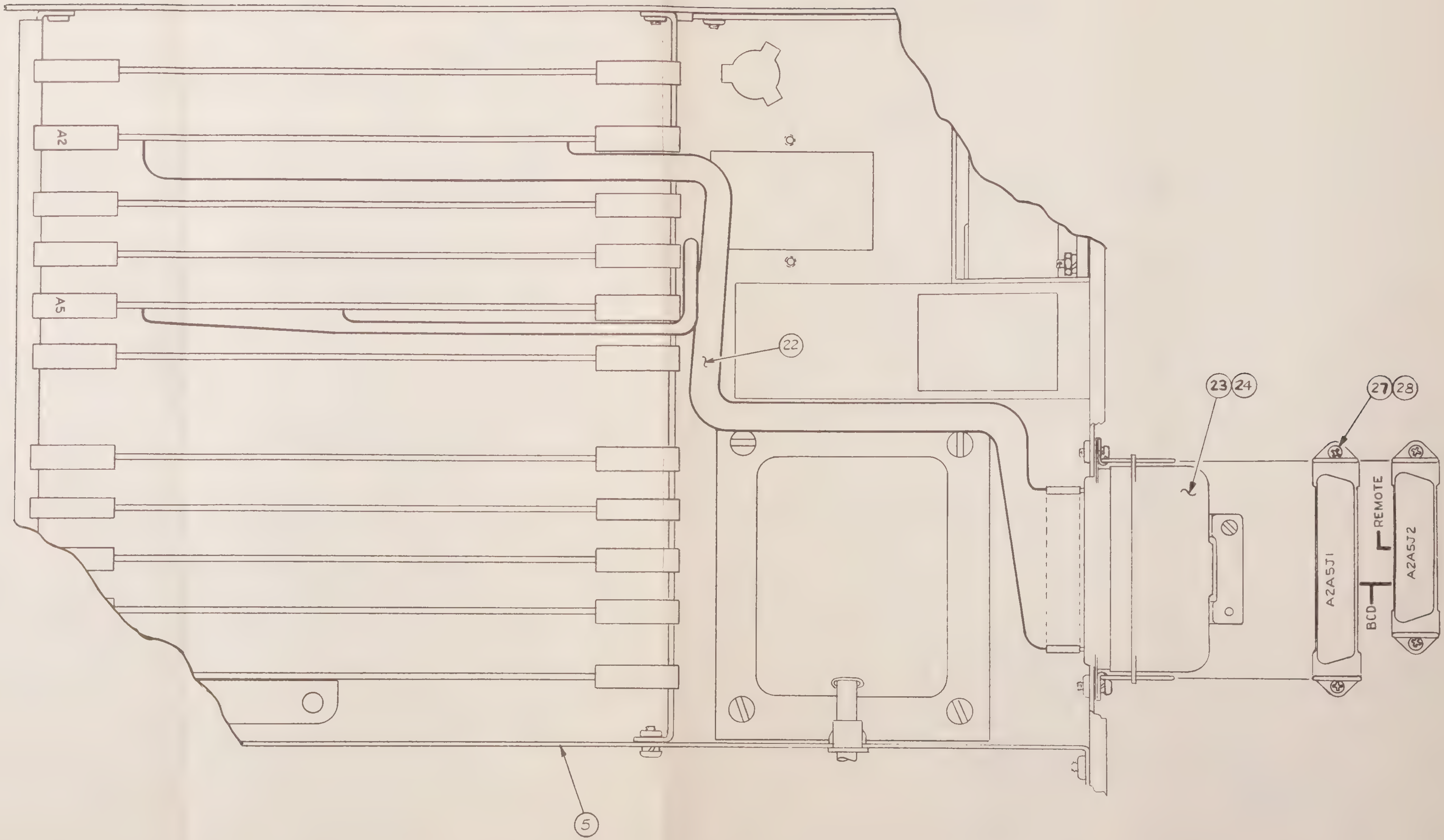

A2
A5
22
23
24
27
28
REMOTE
A2A5J1
A2A5J2
BCD
5

FIGURE 7-48
OPTION 04 FINAL ASSEMBLY
#055500 Rev A

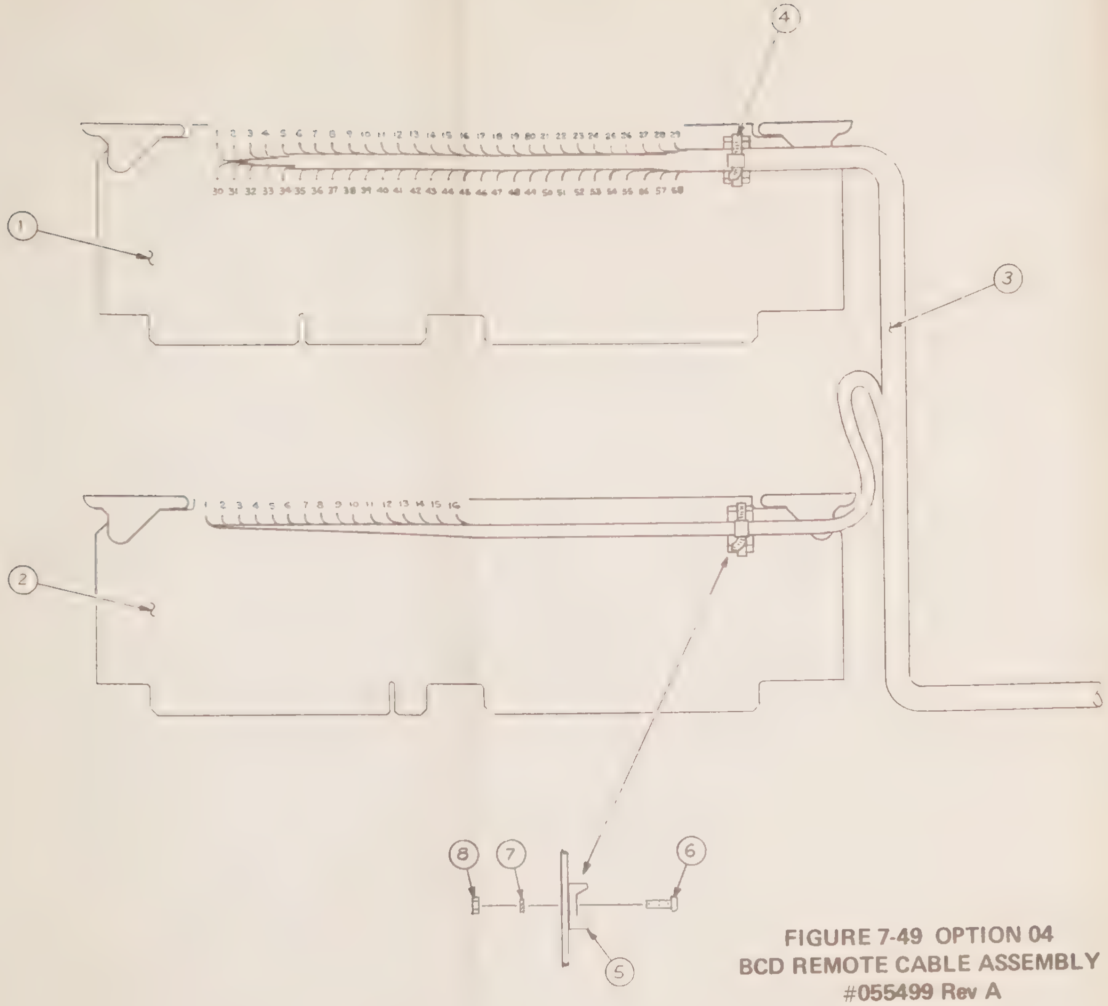

4
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29
30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58
1
3
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16
2
8
7
6
5

FIGURE 7-49 OPTION 04
BCD REMOTE CABLE ASSEMBLY
#055499 Rev A

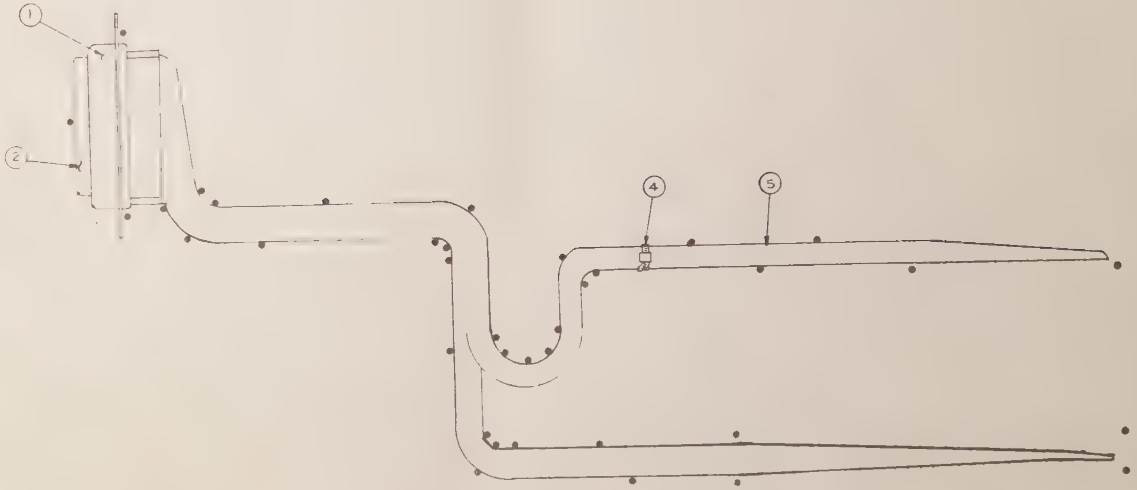


FIGURE 7-50 OPTION 04
BCD REMOTE CABLE
#055498 Rev A

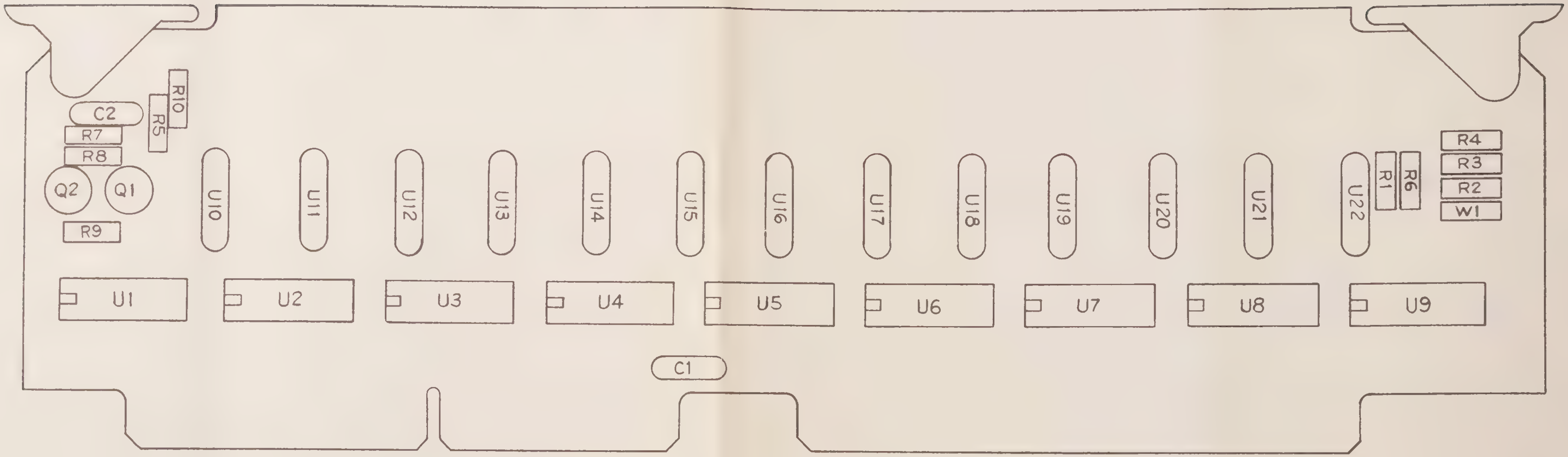
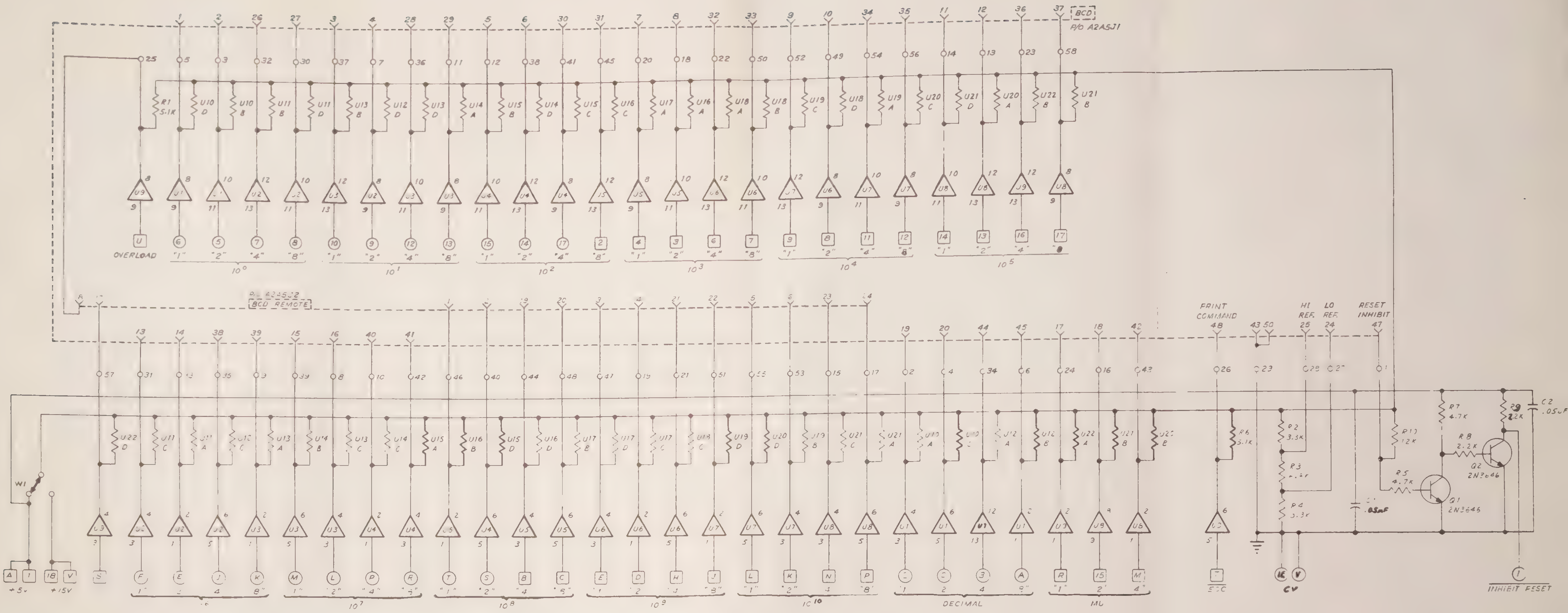
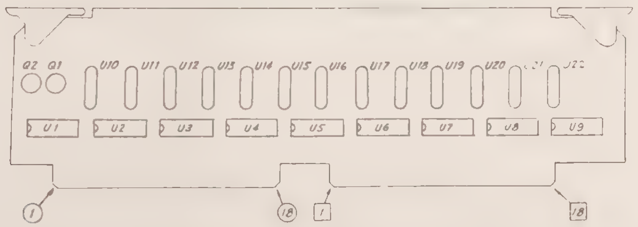
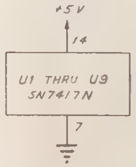

C2
R10
R5
R7
R8
Q2
Q1
R9
U10
U11
U12
U13
U14
U15
U16
U17
U18
U19
U20
U21
U22
R1
R6
R4
R3
R2
W1
U1
U2
U3
U4
U5
U6
U7
U8
U9
C1

FIGURE 7-51 OPTION 04
A2, BCD OUTPUT PC ASSEMBLY
#05344604 Rev A


BCD
P/O A2A5J1
P/O A2A5J2
BCD REMOTE
R1 5.1K
OVERLOAD
"1"
"2"
"4"
"8"
$10^0$
$10^1$
$10^2$
$10^3$
$10^4$
$10^5$
$10^7$
$10^8$
$10^9$
$10^{10}$
DECIMAL
MU
PRINT COMMAND
HI REF.
LO REF.
RESET INHIBIT
R2 3.3K
R3
R4 3.3K
R5 4.7K
R6 5.1K
R7 4.7K
R8 2.2K
R9 2.2K
R10 12K
C1 .05uF
C2 .05uF
Q1 2N3646
Q2 2N3646
W1
+5V
+15V
CV
INHIBIT RESET


Q2
Q1
U10
U11
U12
U13
U14
U15
U16
U17
U18
U19
U20
U21
U22
U1
U2
U3
U4
U5
U6
U7
U8
U9
1
18
1
18


+5V
14
U1 THRU U9
SN7417N
7

NOTE:

1) ALL RESISTORS ¼W 5%.

2) U10 THRU U22 ARE 4×5K RESISTOR NETWORKS.

3) A2A5J1 = 50 PIN AMPHENOL #57-40500.
A2A5P1 = 50 PIN AMPHENOL #57-30500.

4) A2A5J2 = 36 PIN AMPHENOL #57-40360.
A2A5P2 = 36 PIN AMPHENOL #57-30360.

FIGURE 7-52 OPTION 04
A2, BCD OUTPUT SCHEMATIC
#7-05344604 Rev A

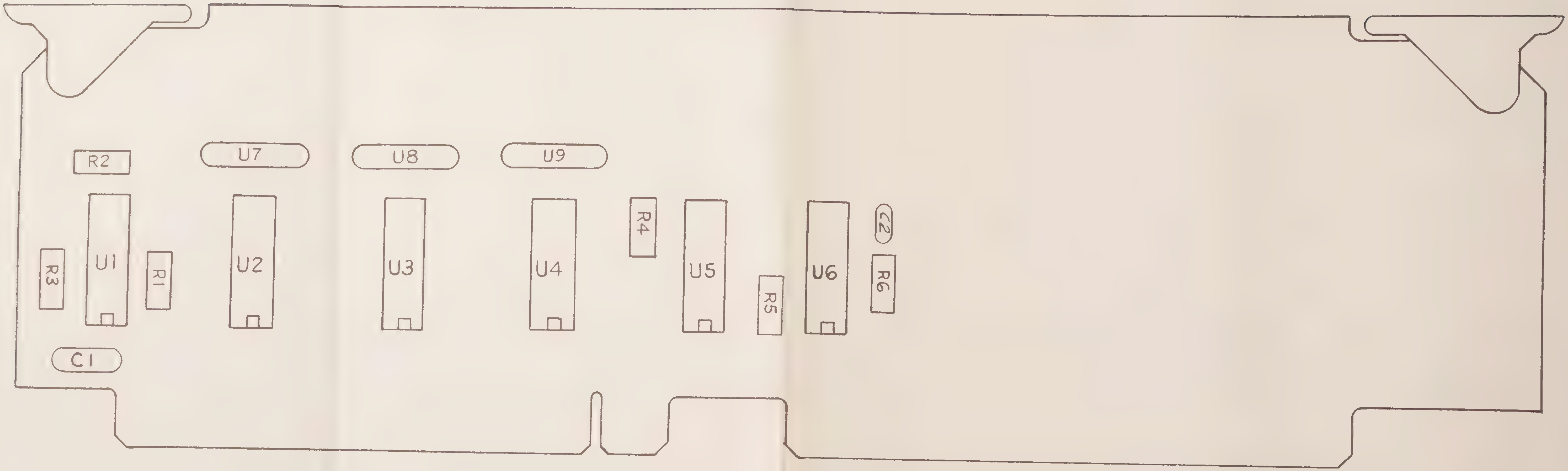
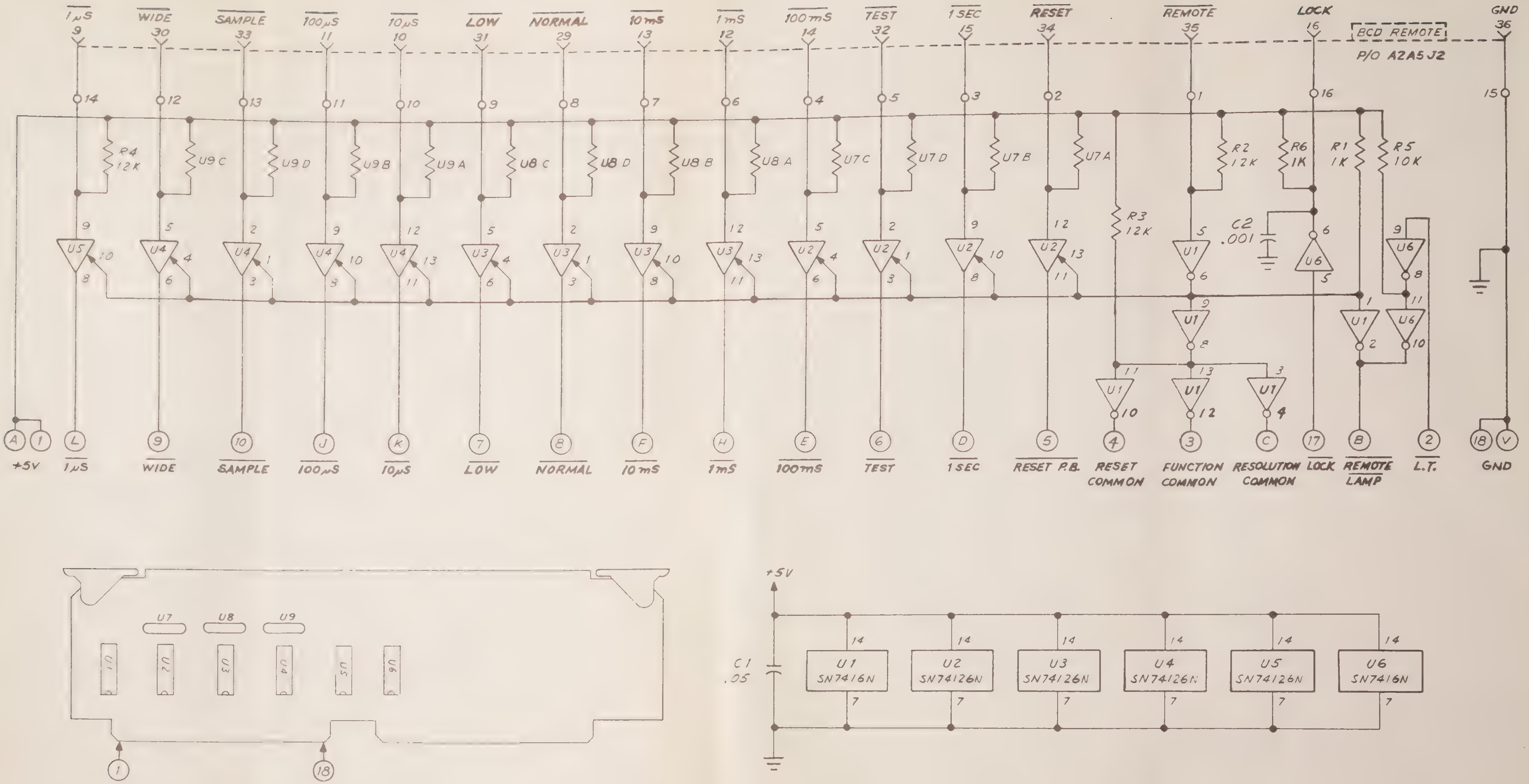

R2
U7
U8
U9
R3
U1
R1
U2
U3
U4
R4
U5
R5
U6
C2
R6
C1

FIGURE 7-53 OPTION 04
A5, REMOTE PC ASSEMBLY
#05339001 Rev B


1µS 9
WIDE 30
SAMPLE 33
100µS 11
10µS 10
LOW 31
NORMAL 29
10mS 13
1mS 12
100mS 14
TEST 32
1 SEC 15
RESET 34
REMOTE 35
LOCK 16
GND 36
BCD REMOTE
P/O A2A5J2
R4 12K
U9C
U9D
U9B
U9A
U8C
U8D
U8B
U8A
U7C
U7D
U7B
U7A
R2 12K
R6 1K
R1 1K
R5 10K
R3 12K
C2 .001
U1
U2
U3
U4
U5
U6
+5V
1µS
WIDE
SAMPLE
100µS
10µS
LOW
NORMAL
10mS
1mS
100mS
TEST
1 SEC
RESET P.B.
RESET COMMON
FUNCTION COMMON
RESOLUTION COMMON
LOCK
REMOTE LAMP
L.T.
GND
U7
U8
U9
+5V
C1 .05
U1 SN7416N
U2 SN74126N
U3 SN74126N
U4 SN74126N
U5 SN74126N
U6 SN7416N
14
7

NOTES: UNLESS OTHERWISE NOTED

1. CAPACITORS ARE IN µF.
2. RESISTORS ARE 1/4W 5%
3. U7 THRU U9 ARE 4 × 12K NETWORKS.
4. A2A5J2 = 36 PIN AMPHENOL #57-40360.
   P2 = 36 PIN AMPHENOL #57-30360.

FIGURE 7-54 OPTION 04
A5, REMOTE SCHEMATIC
#7-05339001 Rev B

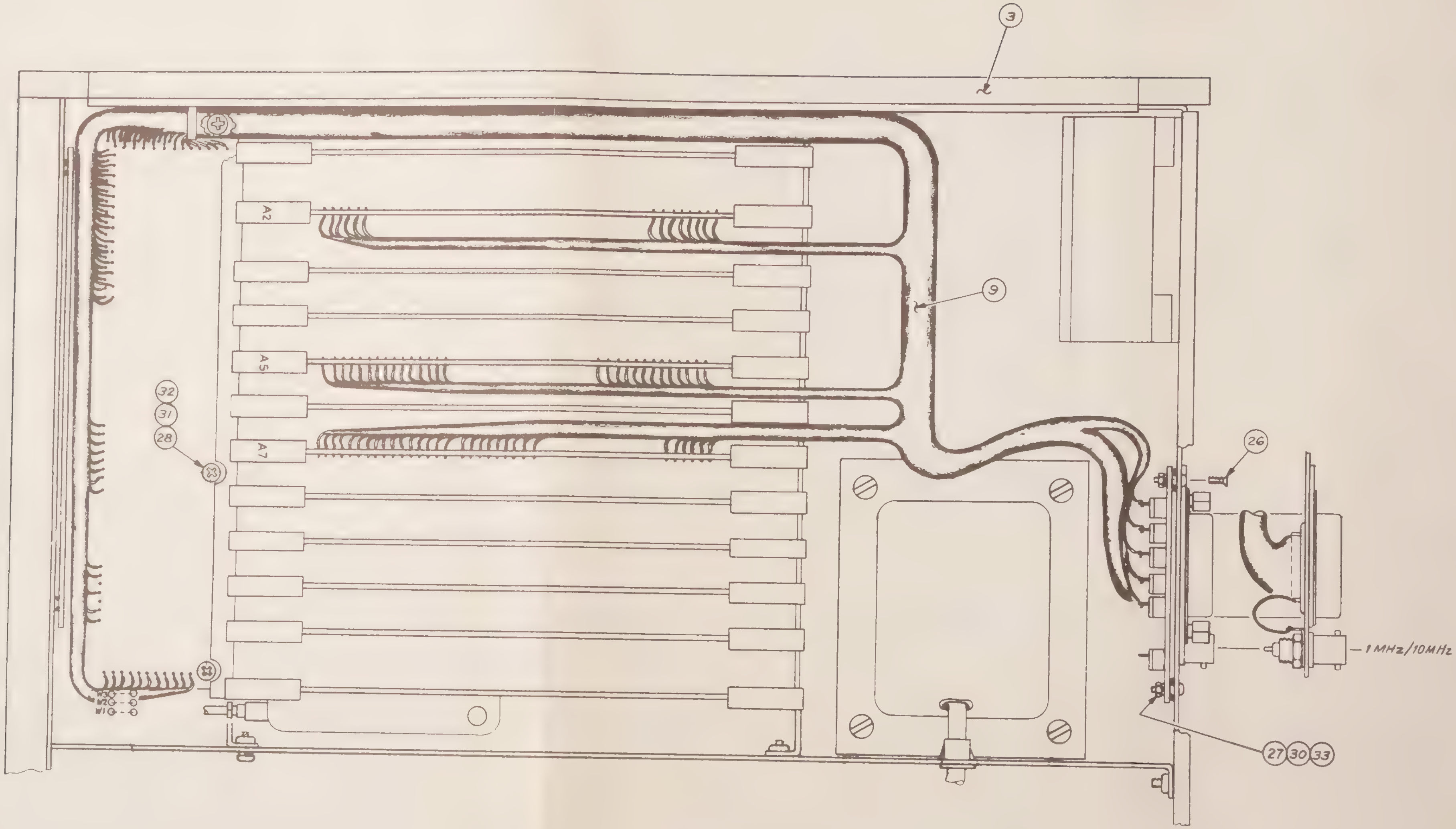

3
9
A2
A5
A7
32
31
28
26
27 30 33
W3
W2
W1
1MHz/10MHz

FIGURE 7-55 OPTION 05
IEEE 488 FINAL ASSEMBLY
#057359 Rev C (Sheet 1 of 2)

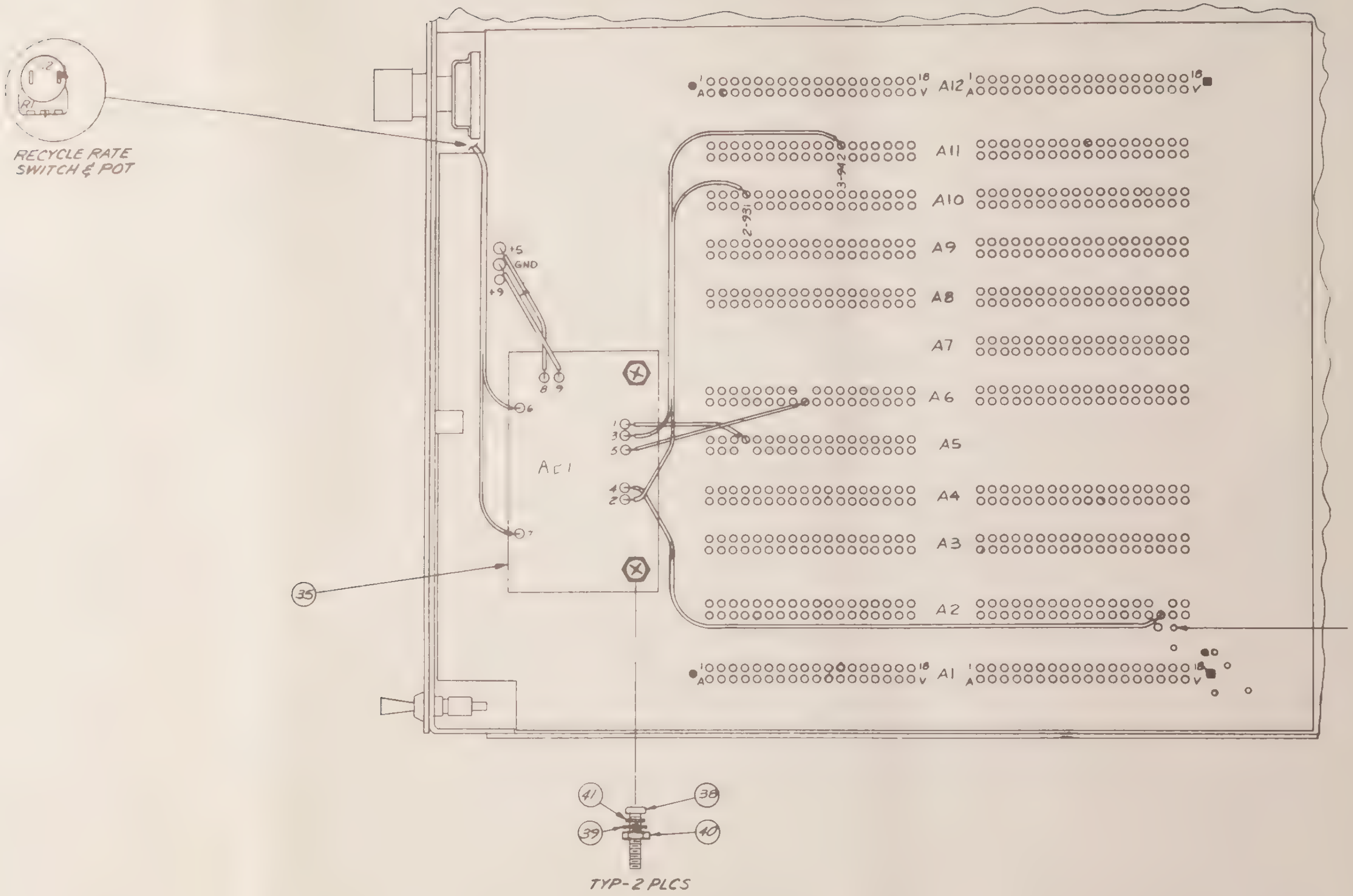
 
R1
2
RECYCLE RATE SWITCH & POT
+5
GND
+9
8
9
6
7
1
3
5
4
2
AC1
35
3-94
2-93
A12
A11
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
1
18
A
V
41
38
39
40
TYP-2 PLCS

FIGURE 7-55 OPTION 05
IEEE 488 FINAL ASSEMBLY
#057359 Rev C (Sheet 2 of 2)

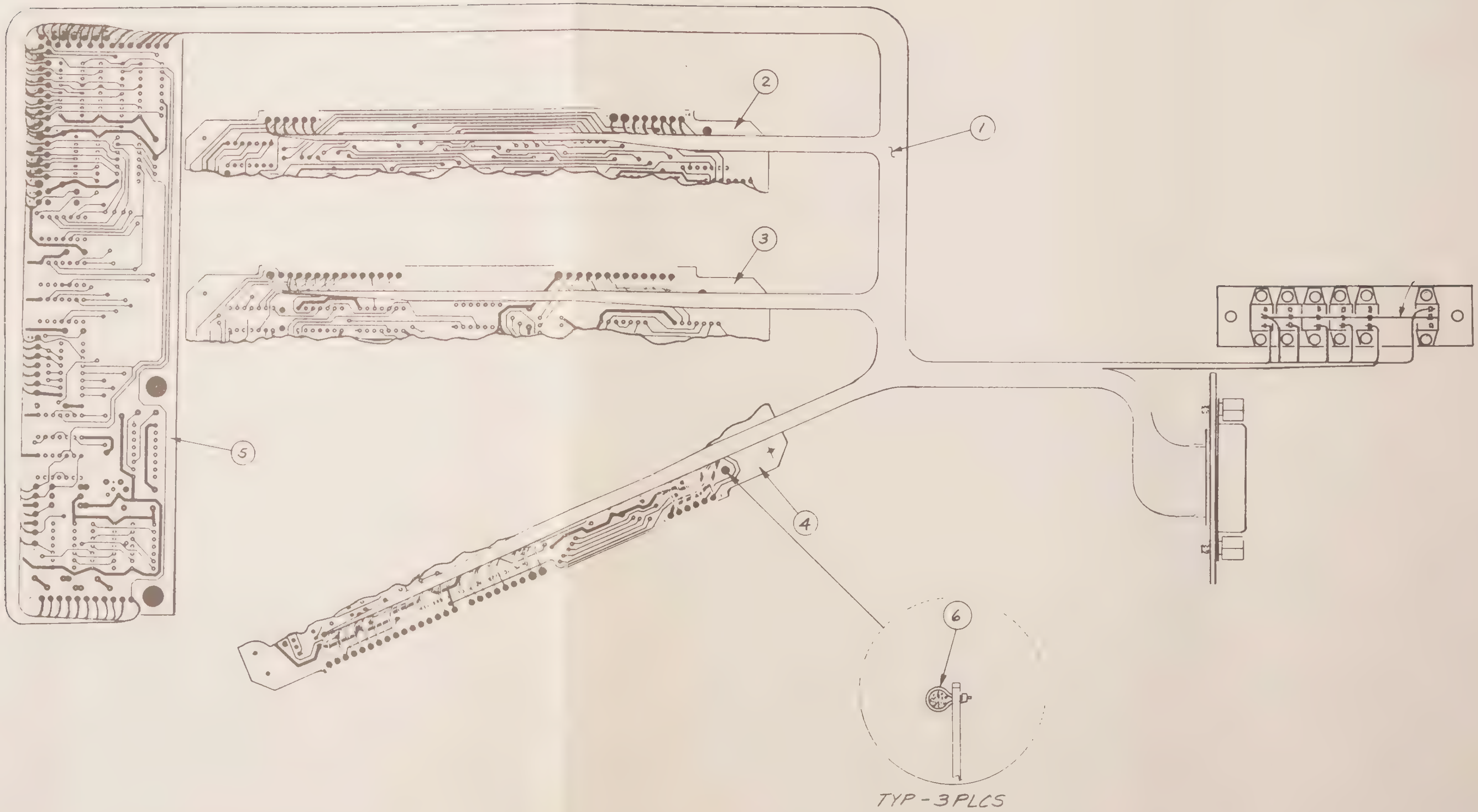

2
1
3
5
4
6
TYP - 3 PLCS

FIGURE 7-56 OPTION 05
IEEE 488 CABLE ASSEMBLY
#057362 Rev B

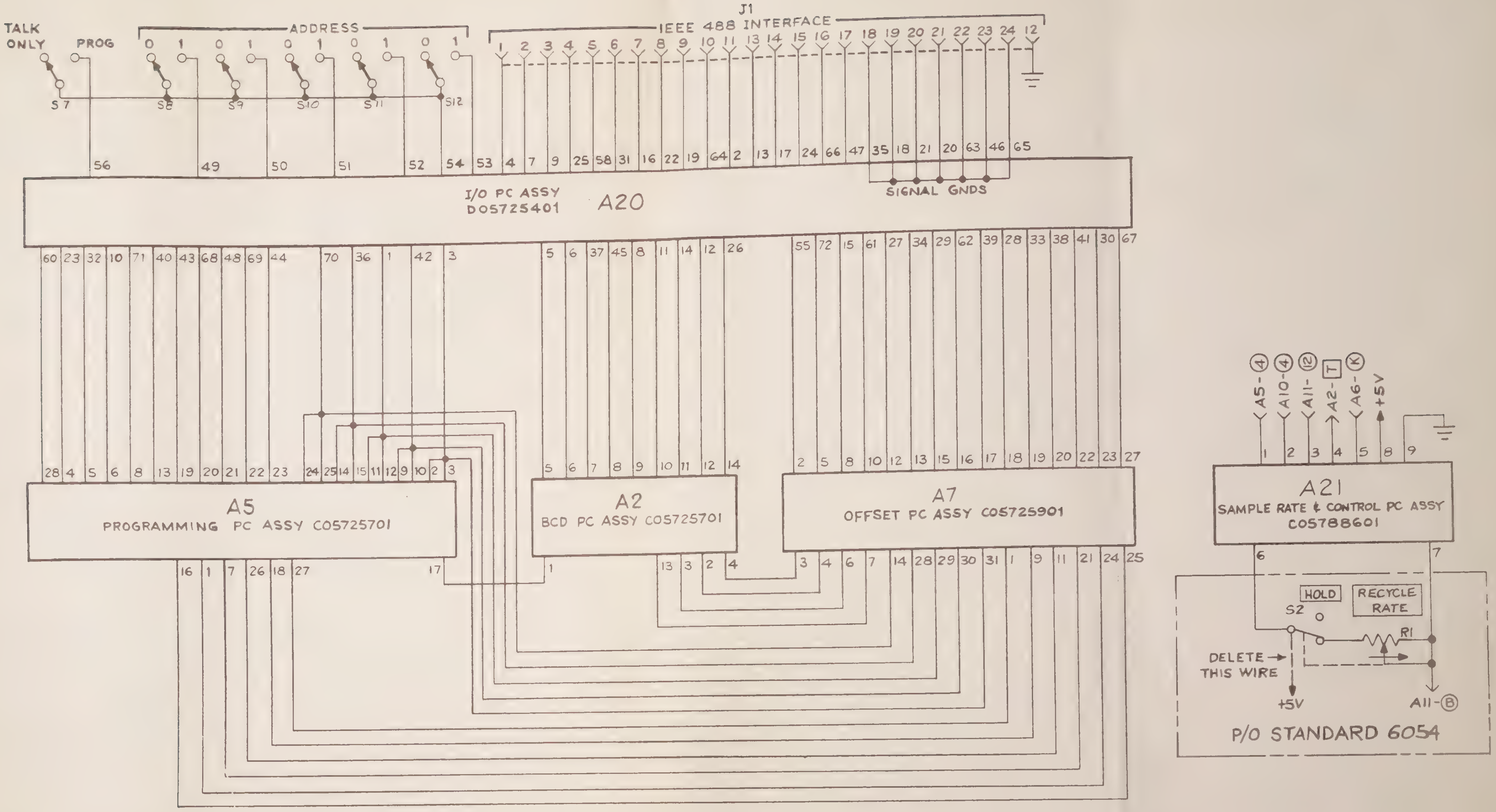

TALK ONLY
PROG
ADDRESS
0 1 0 1 0 1 0 1 0 1
S7 S8 S9 S10 S11 S12
J1
IEEE 488 INTERFACE
1 2 3 4 5 6 7 8 9 10 11 13 14 15 16 17 18 19 20 21 22 23 24 12
56 49 50 51 52 54 53 4 7 9 25 58 31 16 22 19 64 2 13 17 24 66 47 35 18 21 20 63 46 65
I/O PC ASSY
D05725401
A20
SIGNAL GNDS
60 23 32 10 71 40 43 68 48 69 44 70 36 1 42 3
5 6 37 45 8 11 14 12 26
55 72 15 61 27 34 29 62 39 28 33 38 41 30 67
28 4 5 6 8 13 19 20 21 22 23 24 25 14 15 11 12 9 10 2 3
A5
PROGRAMMING PC ASSY C05725701
16 1 7 26 18 27 17
5 6 7 8 9 10 11 12 14
A2
BCD PC ASSY C05725701
1 13 3 2 4
2 5 8 10 12 13 15 16 17 18 19 20 22 23 27
A7
OFFSET PC ASSY C05725901
3 4 6 7 14 28 29 30 31 1 9 11 21 24 25
A5-④
A10-④
A11-⑫
A2-T
A6-Ⓚ
+5V
1 2 3 4 5 8 9
A21
SAMPLE RATE & CONTROL PC ASSY
C05788601
6 7
HOLD
RECYCLE RATE
S2
R1
DELETE THIS WIRE
+5V
A11-Ⓑ
P/O STANDARD 6054

FIGURE 7-57 OPTION 05
IEEE 488 BLOCK DIAGRAM
#7-057359 Rev C

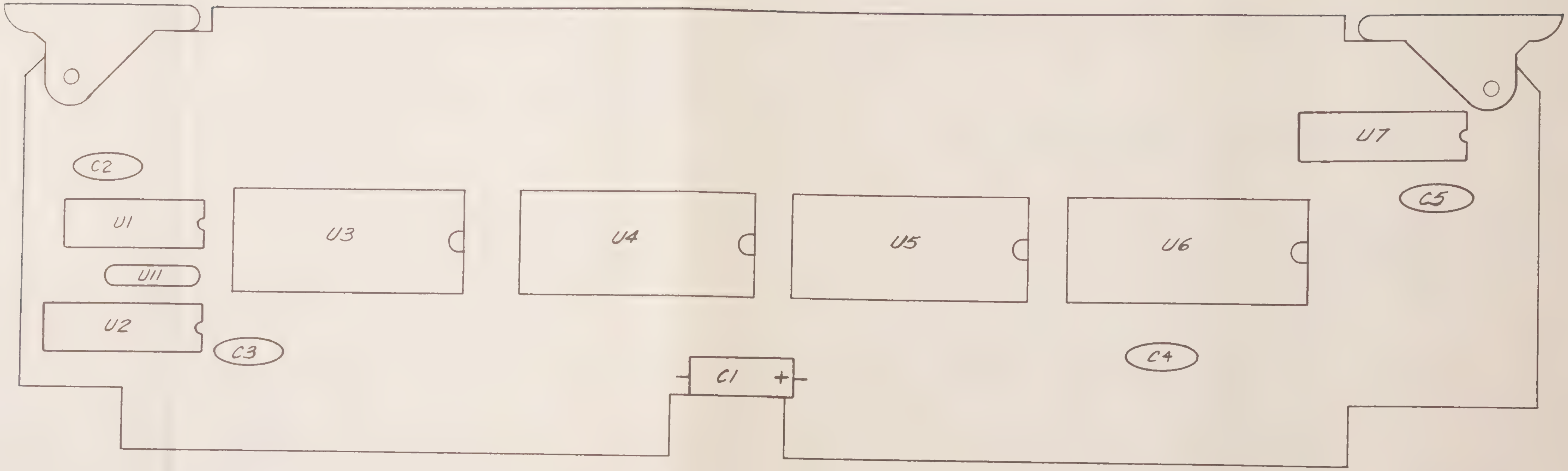
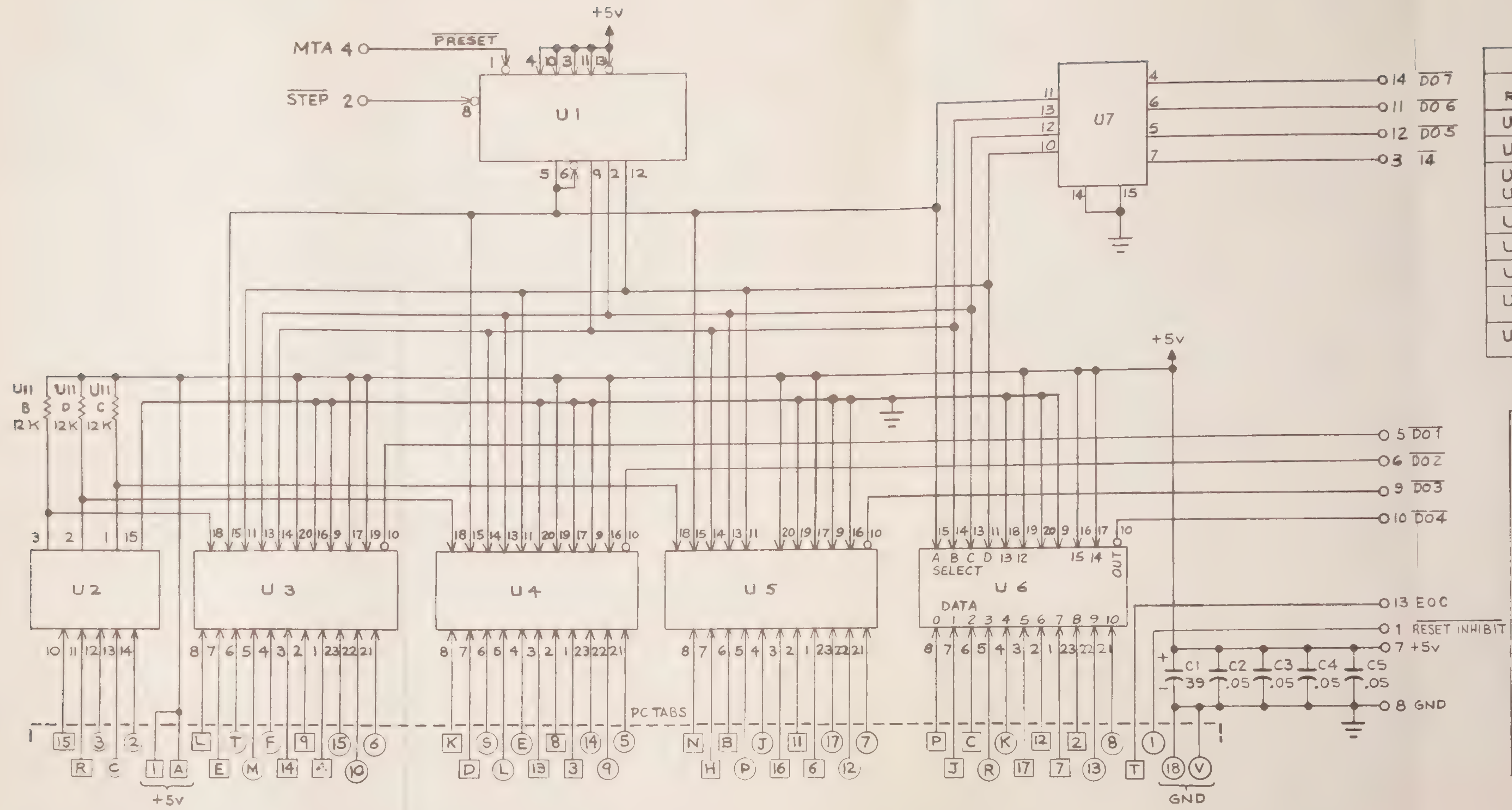

C2
U1
U11
U2
C3
U3
U4
C1
+
U5
U6
C4
U7
C5

FIGURE 7-58 OPTION 05
IEEE 488 BCD OUT PC ASSEMBLY
#05725701 Rev D

NOTE:
1) CAPACITOR VALUES ARE IN µF.


MTA 4
PRESET
STEP 2
+5V
U1
U2
U3
U4
U5
U6
U7
SELECT
DATA
OUT
U11 B 12K
U11 D 12K
U11 C 12K
14 DO7
11 DO6
12 DO5
3 14
5 DO1
6 DO2
9 DO3
10 DO4
13 EOC
1 RESET INHIBIT
7 +5V
8 GND
C1 39
C2 .05
C3 .05
C4 .05
C5 .05
PC TABS
+5V
GND

| I.C. POWER HOOK UP | | | |
|---|---|---|---|
| REF | TYPE | GND | +5V |
| U1 | SN74LS197N | 7 | 14 |
| U2 | 057082 | 8 | 16 |
| U3,U4<br>U5,U6 | SN74150N | 12 | 24 |
| U7 | 067271 | 8 | 16 |
| U8 | ——— | — | — |
| U9 | ——— | — | — |
| U10 | ——— | — | — |
| U11 | RESISTOR NETWORK 4×12 K | — | — |

| | BYTE | COCE | DIO1 | DIO2 | DIO3 | DIO4 | DIO5 | DIO6 | DIO7 |
|---|---|---|---|---|---|---|---|---|---|
| MSD | 1 | 0 | X | X | X | X | 1 | 1 | 0 |
| | 2 | 1 | X | X | X | X | 1 | 1 | 0 |
| | 3 | 2 | X | X | X | X | 1 | 1 | 0 |
| | 4 | 3 | X | X | X | X | 1 | 1 | 0 |
| | 5 | 4 | X | X | X | X | 1 | 1 | 0 |
| | 6 | 5 | X | X | X | X | 1 | 1 | 0 |
| | 7 | 6 | X | X | X | X | 1 | 1 | 0 |
| | 8 | 7 | X | X | X | X | 1 | 1 | 0 |
| | 9 | 8 | X | X | X | X | 1 | 1 | 0 |
| | 10 | 9 | X | X | X | X | 1 | 1 | 0 |
| LSD | 11 | 10 | X | X | X | X | 1 | 1 | 0 |
| E | 12 | 11 | 1 | 0 | 1 | 0 | 0 | 0 | 1 |
| + | 13 | 12 | 1 | 1 | 0 | 1 | 0 | 1 | 0 |
| 0→6 | 14 | 13 | X | X | X | 0 | 1 | 1 | 0 |
| CR | 15 | 14 | 1 | 0 | 1 | 1 | 0 | 0 | 0 |
| LF | 16 | 15 | 0 | 1 | 0 | 1 | 0 | 0 | 0 |

FIGURE 7-59 OPTION 05
IEEE 488 BCD OUT SCHEMATIC
#7-05725701 Rev D

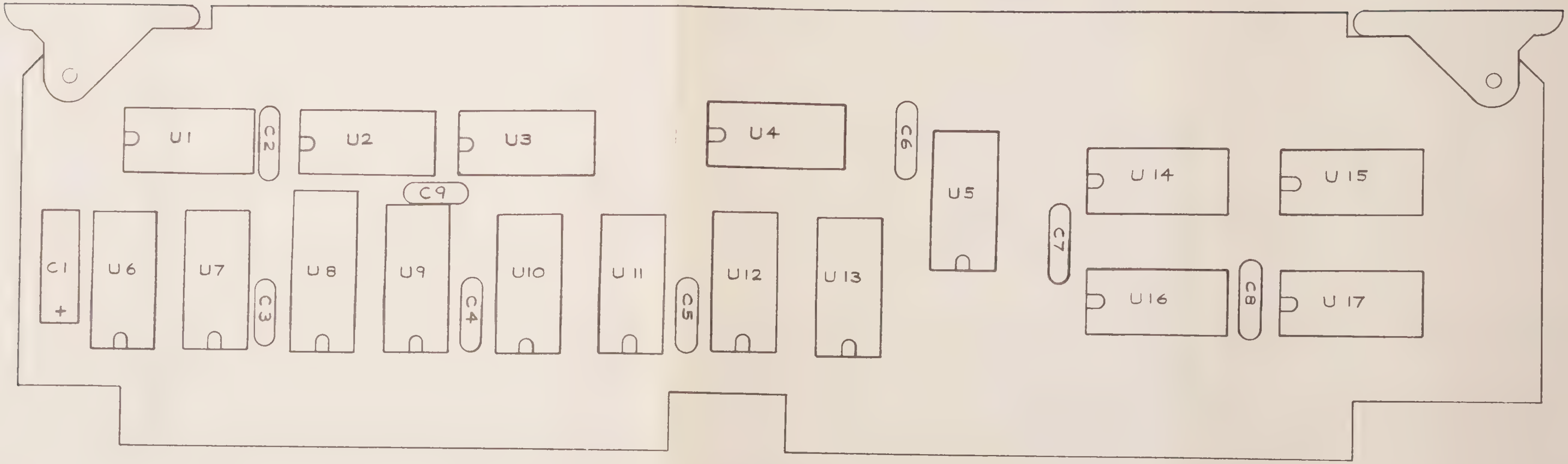
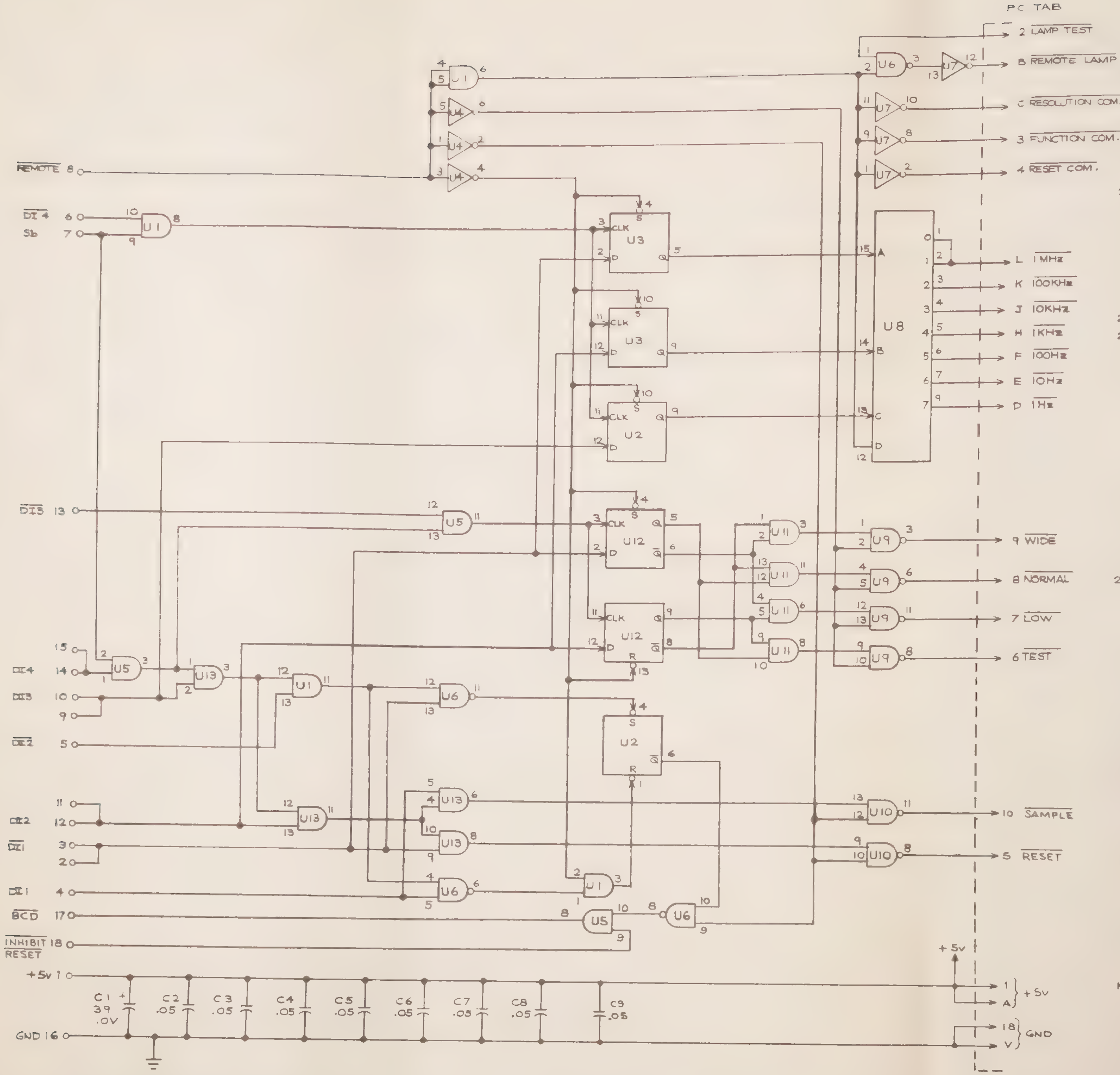
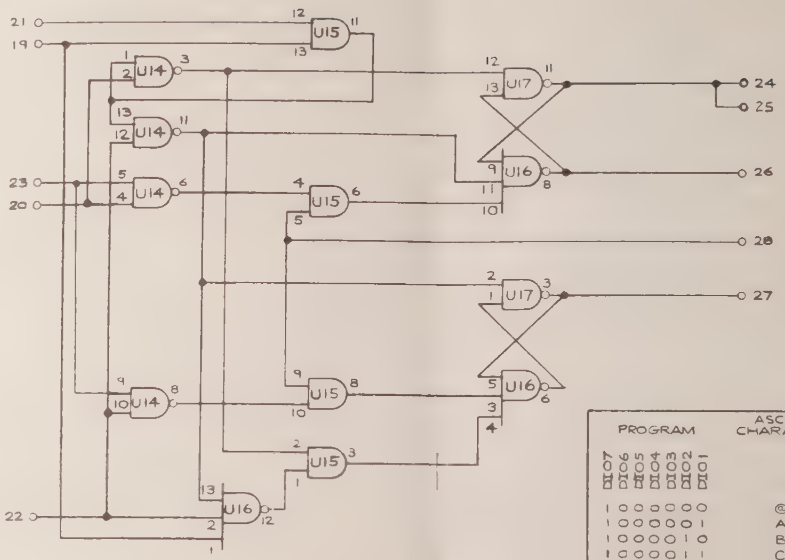

U1
C2
U2
U3
U4
C6
U5
U14
U15
C9
C1
+
U6
U7
U8
U9
U10
U11
U12
U13
C7
C3
C4
C5
U16
C8
U17

FIGURE 7-60 OPTION 05
A5, IEEE 488 PROGRAMMING PC ASSEMBLY
#05725601 Rev B


PC TAB
2 LAMP TEST
B REMOTE LAMP
C RESOLUTION COM.
3 FUNCTION COM.
4 RESET COM.
L 1MHz
K 100KHz
J 10KHz
H 1KHz
F 100Hz
E 10Hz
D 1Hz
9 WIDE
8 NORMAL
7 LOW
6 TEST
10 SAMPLE
5 RESET
1
A
+5v
18
V
GND
REMOTE 8
DI4 6
5b 7
DI5 13
15
DI4 14
DI3 10
9
DI2 5
11
DI2 12
DI1 3
2
DI1 4
BCD 17
INHIBIT RESET 18
+5v 1
GND 16
C1 39 .0V
C2 .05
C3 .05
C4 .05
C5 .05
C6 .05
C7 .05
C8 .05
C9 .05
U1
U2
U3
U4
U5
U6
U7
U8
U9
U10
U11
U12
U13
CLK
S
D
R
Q


21
19
23
20
22
U14
U15
U16
U17
24
25
26
28
27

| I.C. POWER HOOK UP | | | |
|---|---|---|---|
| REF. | TYPE | GND | +5V |
| U1, U5, U11<br>U13, U15 | SN74LS08N | 7 | 14 |
| U2, U3 U12 | SN74LS74N | - | 14 |
| U4 | SN74LS04N | 7 | 14 |
| U6, U14, U17 | SN74LS00N | 7 | 14 |
| U7 | SN7416N | 7 | 14 |
| U8 | SN74145N | 8 | 16 |
| U9, U10 | SN7426N | 7 | 14 |
| U16 | SN74LS10N | 7 | 14 |

1 . ALL CAPACITOR VALUES ARE IN μf.

NOTE : UNLESS OTHERWISE SPECIFIED.

| | PROGRAM | | | | | | | ASCII CHARACTER | FUNCTION |
|---|---|---|---|---|---|---|---|---|---|
| | DI07 | DI06 | DI05 | DI04 | DI03 | DI02 | DI01 | | |
| | 1 | 0 | 0 | 0 | 0 | 0 | 0 | @ | 1MHz |
| | 1 | 0 | 0 | 0 | 0 | 0 | 1 | A | 1MHZ |
| | 1 | 0 | 0 | 0 | 0 | 1 | 0 | B | 100KHZ |
| | 1 | 0 | 0 | 0 | 0 | 1 | 1 | C | 10KHZ |
| | 1 | 0 | 0 | 0 | 1 | 0 | 0 | D | 1KHZ |
| | 1 | 0 | 0 | 0 | 1 | 0 | 1 | E | 100 HZ |
| | 1 | 0 | 0 | 0 | 1 | 1 | 0 | F | 10 HZ |
| * | 1 | 0 | 0 | 0 | 1 | 1 | 1 | G | 1 Hz |
| | 1 | 0 | 0 | 1 | 0 | 0 | 0 | H | WIDE |
| * | 1 | 0 | 0 | 1 | 0 | 0 | 1 | I | NORMAL |
| | 1 | 0 | 0 | 1 | 0 | 1 | 0 | J | LOW |
| | 1 | 0 | 0 | 1 | 0 | 1 | 1 | K | TEST |
| * | 1 | 0 | 0 | 1 | 1 | 0 | 0 | L | HOLD |
| | 1 | 0 | 0 | 1 | 1 | 0 | 1 | M | RECYCLE |
| | 1 | 0 | 0 | 1 | 1 | 1 | 0 | N | SAMPLE |
| | 1 | 0 | 0 | 1 | 1 | 1 | 1 | O | RESET |
| * | 1 | 0 | 1 | 0 | 0 | 0 | 0 | P | NO OFFSET |
| | 1 | 0 | 1 | 0 | 0 | 0 | 1 | Q | POSITIVE OFFSETS |
| | 1 | 0 | 1 | 0 | 0 | 1 | 0 | R | |
| | 1 | 0 | 1 | 0 | 0 | 1 | 1 | S | |
| | 1 | 0 | 1 | 0 | 1 | 0 | 0 | T | |
| | 1 | 0 | 1 | 0 | 1 | 0 | 1 | U | |
| | 1 | 0 | 1 | 0 | 1 | 1 | 0 | V | |
| | 1 | 0 | 1 | 0 | 1 | 1 | 1 | W | |
| | 1 | 0 | 1 | 1 | 0 | 0 | 0 | X | NEGATIVE OFFSETS |
| | 1 | 0 | 1 | 1 | 0 | 0 | 1 | Y | |
| | 1 | 0 | 1 | 1 | 0 | 1 | 0 | Z | |
| | 1 | 0 | 1 | 1 | 0 | 1 | 1 | [ | |
| | 1 | 0 | 1 | 1 | 1 | 0 | 0 | \ | |
| | 1 | 0 | 1 | 1 | 1 | 0 | 1 | ] | |
| | 1 | 0 | 1 | 1 | 1 | 1 | 0 | ^ | |
| | 1 | 0 | 1 | 1 | 1 | 1 | 1 | _ | |

*— WAKE UP STATE.

FIGURE 7-61 OPTION 05
A5, IEEE 488 PROGRAMMING SCHEMATIC
#7-05725601 Rev A

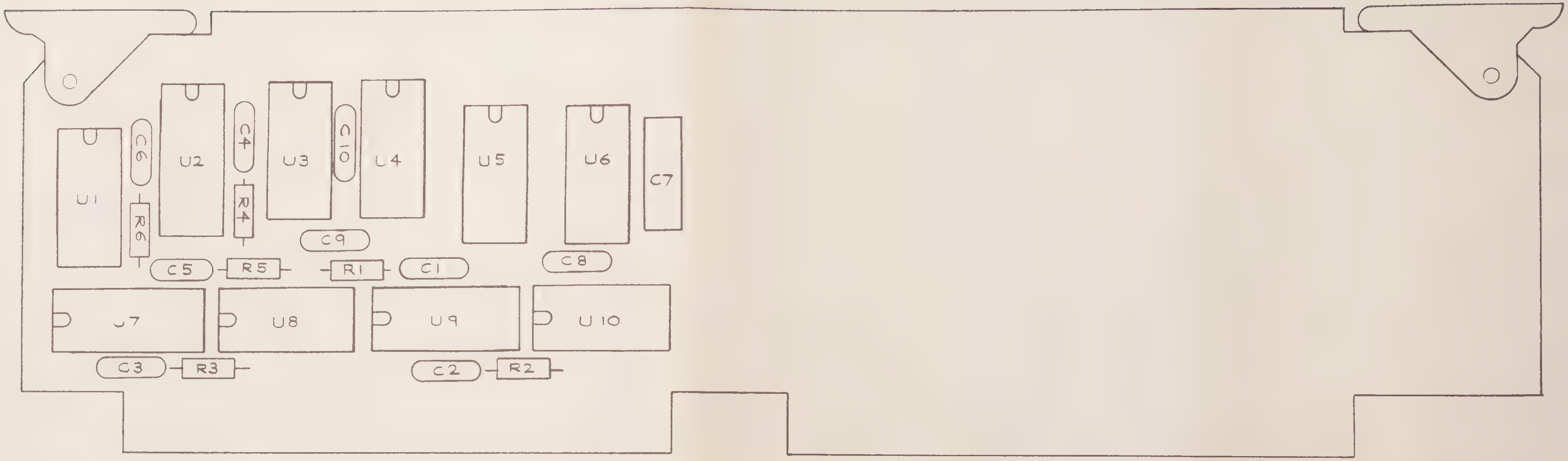
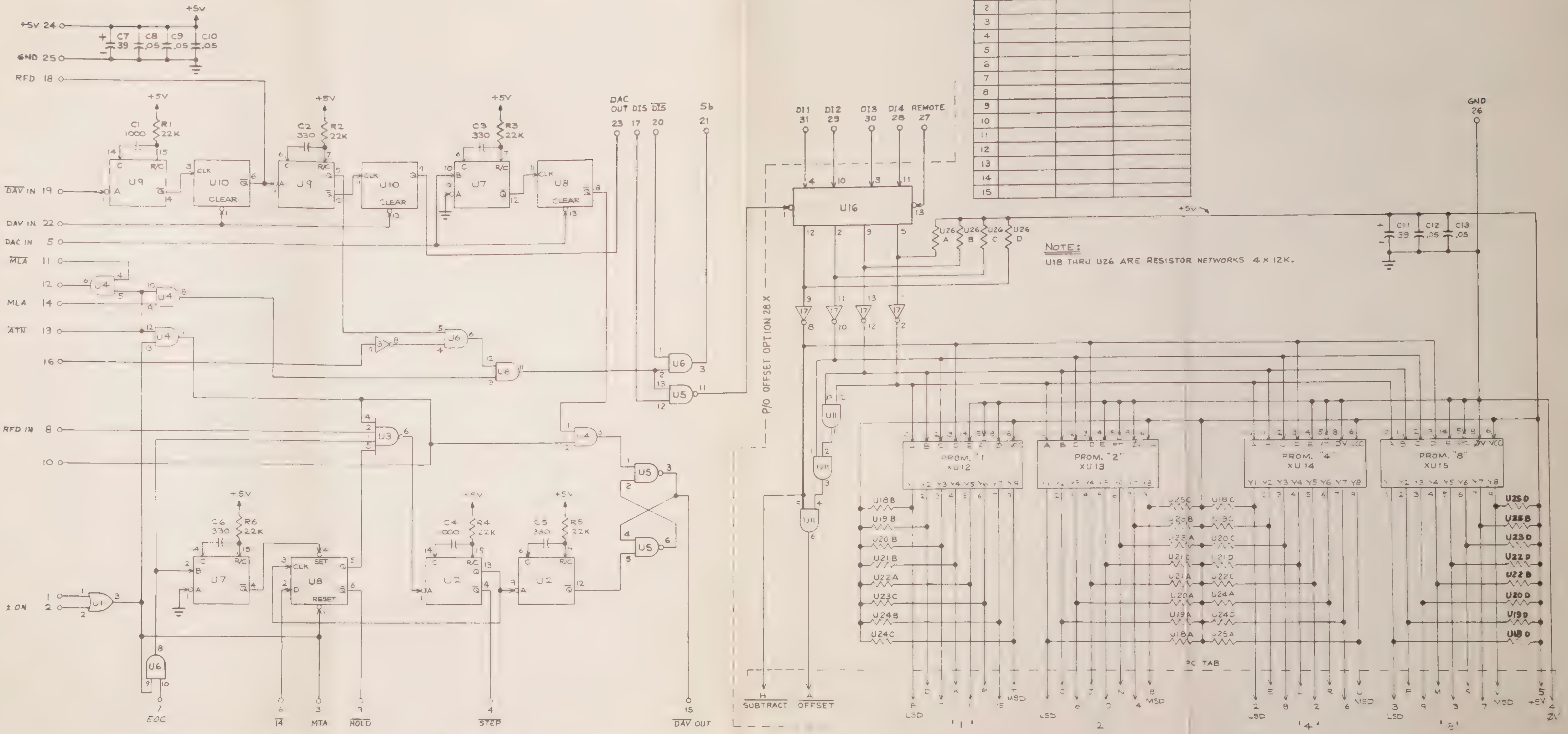

U1
C6
R6
U2
C4
R4
U3
C10
U4
U5
U6
C7
C9
C5
R5
R1
C1
C8
U7
U8
U9
U10
C3
R3
C2
R2

FIGURE 7-62 OPTION 05
A7, IEEE 488 UNIVERSAL OFFSET
PC ASSEMBLY #05725901 Rev B

| Nº | OFFSET | RESOLUTION | ASCII CHARACTER |
|---|---|---|---|
| 0 | 0 | — | P |
| 1 | | | |
| 2 | | | |
| 3 | | | |
| 4 | | | |
| 5 | | | |
| 6 | | | |
| 7 | | | |
| 8 | | | |
| 9 | | | |
| 10 | | | |
| 11 | | | |
| 12 | | | |
| 13 | | | |
| 14 | | | |
| 15 | | | |


+5V 24
GND 25
+5V
C7 39
C8 .05
C9 .05
C10 .05
RFD 18
C1 1000
R1 22K
C2 330
R2 22K
C3 330
R3 22K
U9
U10
CLEAR
U7
U8
DAV IN 19
DAV IN 22
DAC IN 5
MLA 11
12
MLA 14
ATN 13
16
RFD IN 8
10
U4
U6
U3
U5
U1
U2
C6 330
R6 22K
C4 1000
R4 22K
C5 330
R5 22K
SET
RESET
ON 1 2
7 EOC
6 14
3 MTA
9 HOLD
4 STEP
15 DAV OUT
DAC OUT 23
DIS 17
DIS 20
Sb 21
DI1 31
DI2 29
DI3 30
DI4 28
REMOTE 27
U16
U17
U11
P/O OFFSET OPTION 28 X
H SUBTRACT
A OFFSET
U26 A
U26 B
U26 C
U26 D
+5V
GND 26
C11 39
C12 .05
C13 .05
PROM. "1" XU12
PROM. "2" XU13
PROM. "4" XU14
PROM. "8" XU15
U18B
U19B
U20B
U21B
U22A
U23C
U24B
U24C
U25C
U25B
U23A
U21C
U21A
U20A
U19A
U18A
U18C
U19C
U20C
U21D
U22C
U24A
U24D
U25A
U25D
U23D
U22D
U20D
U18D
PC TAB
LSD
MSD
'1'
2
'4'
'8'
+5V
5
4
ØV

NOTE:
U18 THRU U26 ARE RESISTOR NETWORKS 4 X 12K.

| IC POWER HOOK UP | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| IC | U1 | U2,U7,U9 | U3 | U4,U6,U11 | U5 | U8,U10 | XU12 | XU13 | XU14 | XU15 | U16 | U17 |
| TYPE | SN74LS32N | SN74LS123N | SN74LS20N | SN74LS08N | SN74LS00N | SN74LS74N | | | | | SN74LS197N | SN74LS04N |
| GND | 7 | 8 | 7 | 7 | 7 | 7 | 8 | 8 | 8 | 8 | 7 | 7 |
| +5V | 14 | 16 | 14 | 4 | 14 | 14 | 16 | 6 | 16 | 6 | 14 | 4 |

3. ALL PROM'S ARE SN74188AN.
2. ALL RESISTOR VALUES ARE IN OHMS, 5%, 1/4W.
1. ALL CAPACITOR VALUES ARE IN µf.
NOTE:
UNLESS OTHERWISE SPECIFIED

FIGURE 7-63 OPTION 05
A7, IEEE 488 UNIVERSAL OFFSET
SCHEMATIC #7-05725901 Rev D

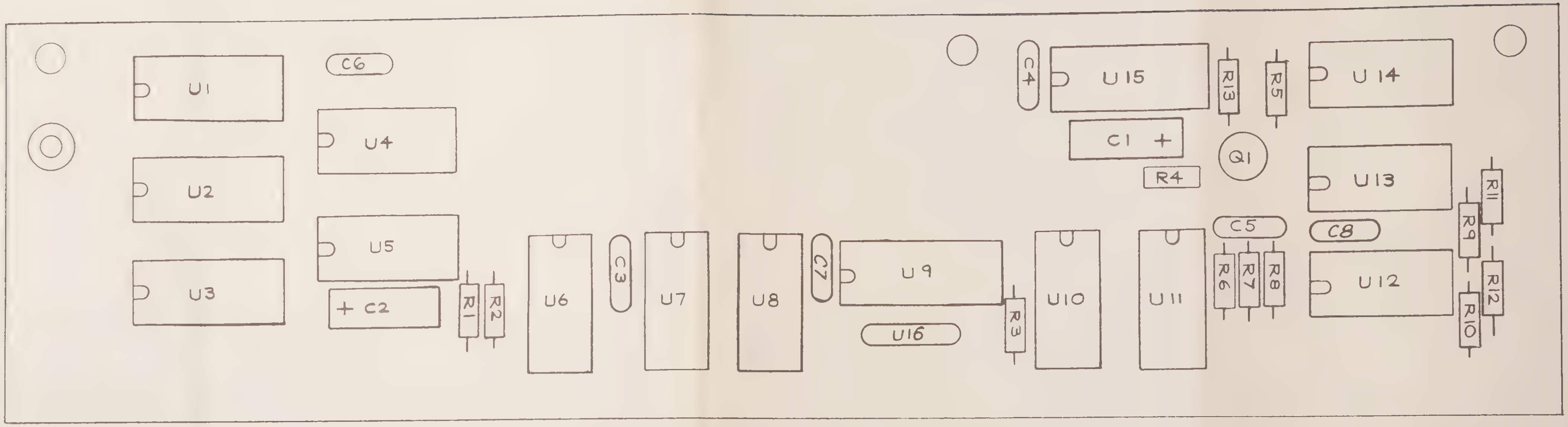
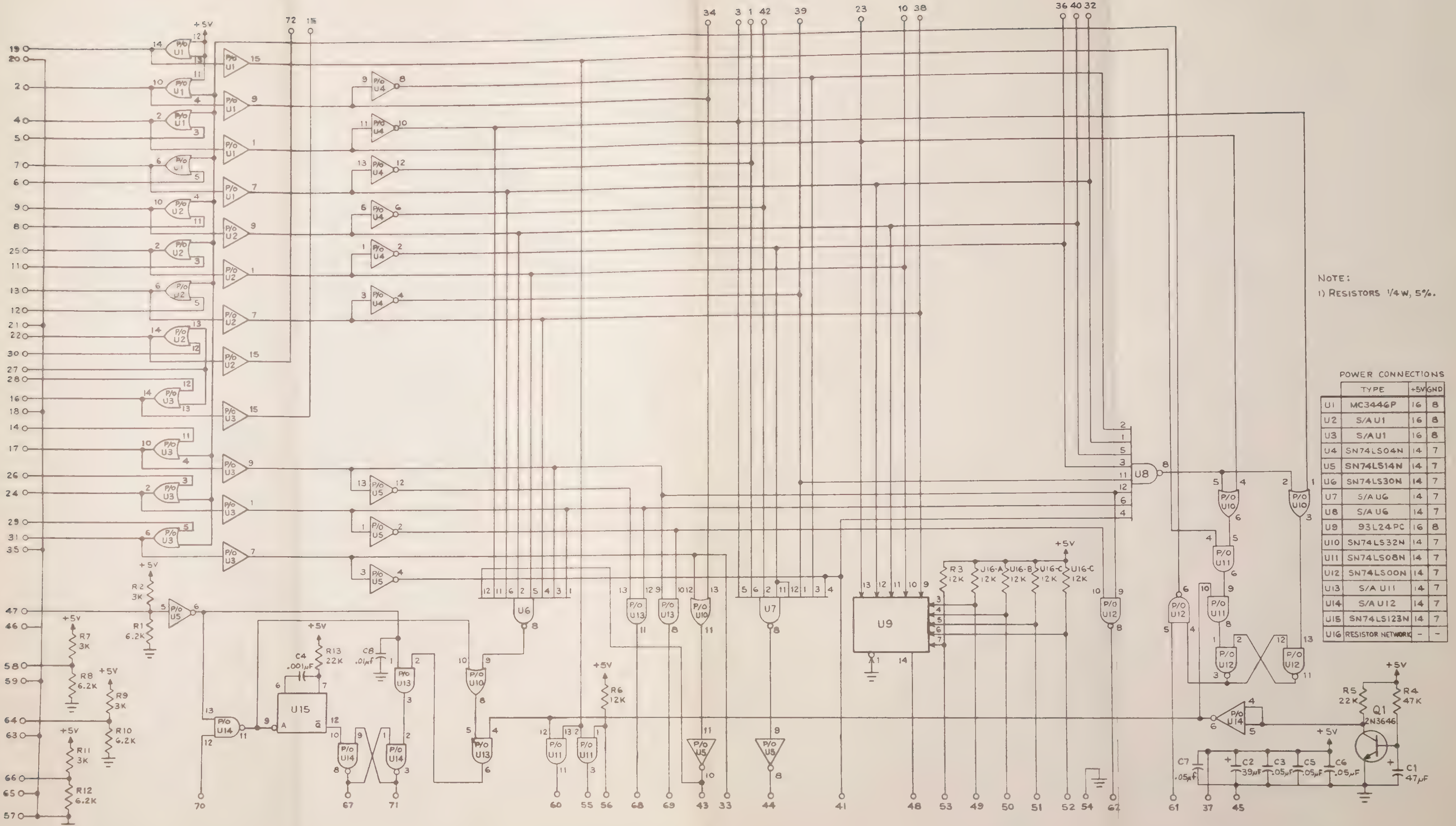

U1
C6
U4
U2
U5
U3
+ C2
R1
R2
U6
C3
U7
U8
C7
U9
U16
R3
U10
U11
C4
U15
C1 +
R4
R13
R5
Q1
U14
U13
C5
C8
R6
R7
R8
R9
R11
U12
R10
R12

FIGURE 7-64 OPTION 05
A20, IEEE 488 I/O PC ASSEMBLY
#05725401 Rev C


P/O U1
P/O U2
P/O U3
P/O U4
P/O U5
U6
U7
U8
U9
P/O U10
P/O U11
P/O U12
P/O U13
P/O U14
U15
Q1 2N3646
R1 6.2K
R2 3K
R3 12K
R4 47K
R5 22K
R6 12K
R7 3K
R8 6.2K
R9 3K
R10 6.2K
R11 3K
R12 6.2K
R13 22K
U16-A 12K
U16-B 12K
U16-C 12K
C1 47μF
C2 39μF
C3 .05μF
C4 .001μF
C5 .05μF
C6 .05μF
C7 .05μF
C8 .01μF
+5V

NOTE:
1) RESISTORS 1/4W, 5%.

POWER CONNECTIONS

| | TYPE | +5V | GND |
|---|---|---|---|
| U1 | MC3446P | 16 | 8 |
| U2 | S/A U1 | 16 | 8 |
| U3 | S/A U1 | 16 | 8 |
| U4 | SN74LS04N | 14 | 7 |
| U5 | SN74LS14N | 14 | 7 |
| U6 | SN74LS30N | 14 | 7 |
| U7 | S/A U6 | 14 | 7 |
| U8 | S/A U6 | 14 | 7 |
| U9 | 93L24PC | 16 | 8 |
| U10 | SN74LS32N | 14 | 7 |
| U11 | SN74LS08N | 14 | 7 |
| U12 | SN74LS00N | 14 | 7 |
| U13 | S/A U11 | 14 | 7 |
| U14 | S/A U12 | 14 | 7 |
| U15 | SN74LS123N | 14 | 7 |
| U16 | RESISTOR NETWORK | - | - |

**FIGURE 7-65 OPTION 05**
**A20, IEEE 488 I/O SCHEMATIC**
**#7-05725401 Rev B**

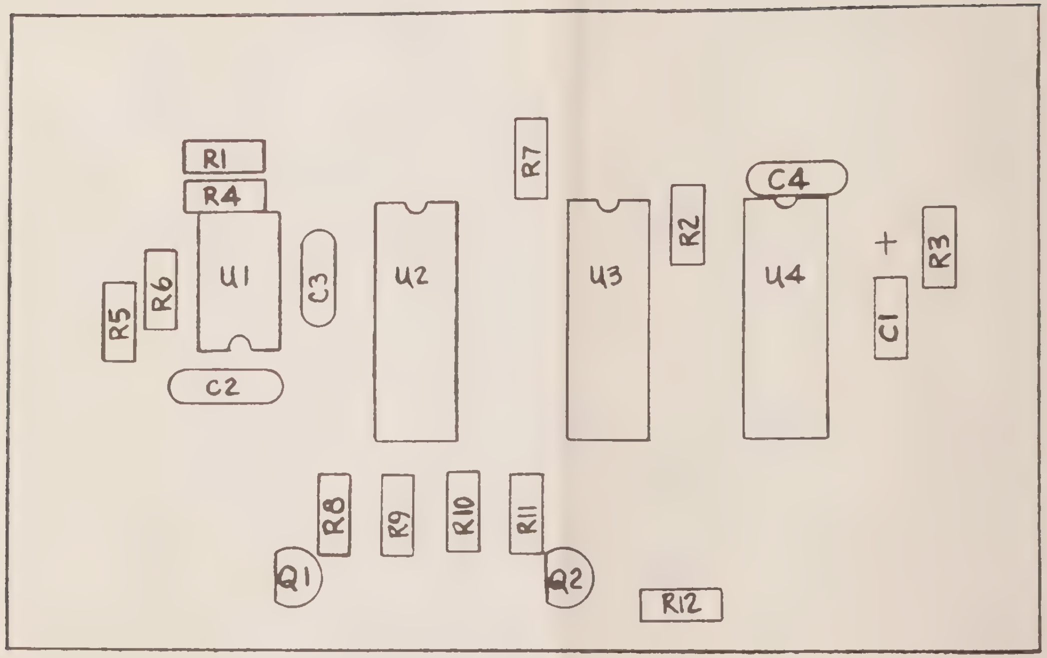
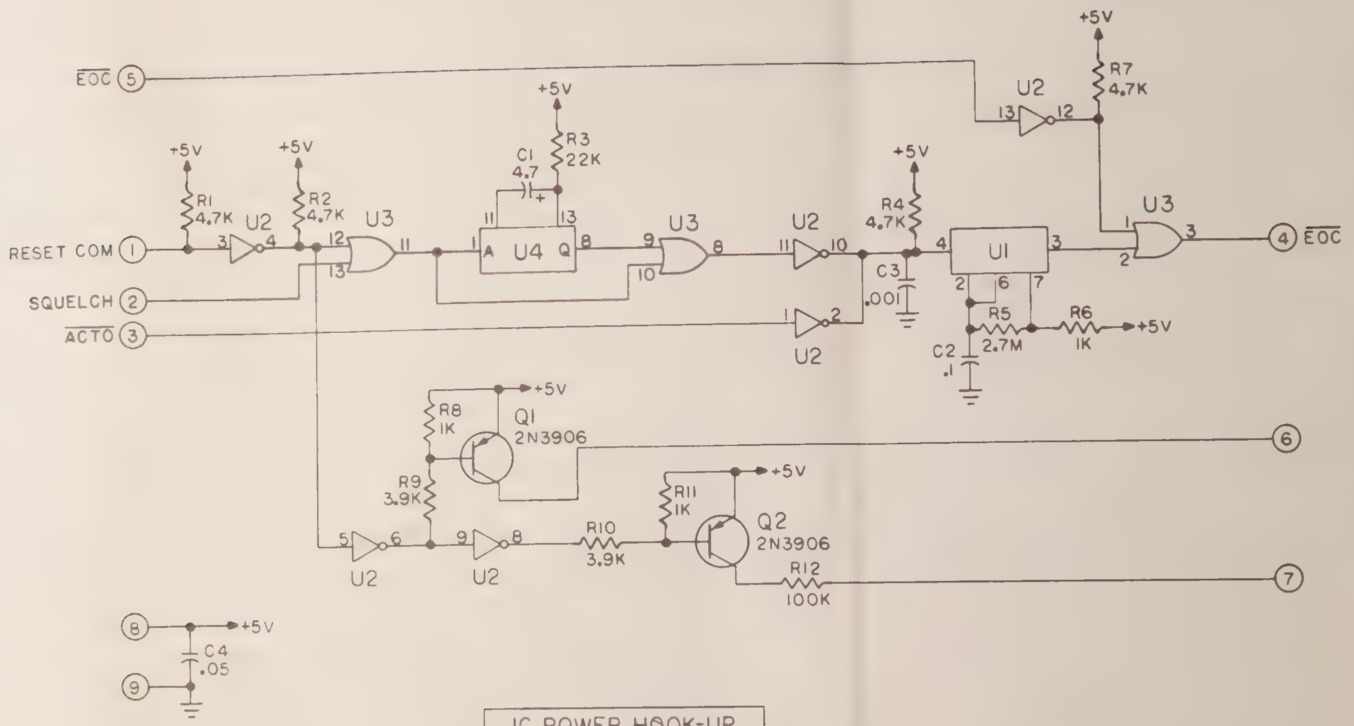

R1
R4
R7
C4
R5
R6
U1
C3
U2
U3
R2
U4
+
R3
C1
C2
R8
R9
R10
R11
Q1
Q2
R12

FIGURE 7-66 OPTION 05
A21, SAMPLE RATE & CONTROL
PC ASSEMBLY #05788601 Rev C



$\overline{EOC}$ ⑤
RESET COM ①
SQUELCH ②
$\overline{ACTO}$ ③
④ $\overline{EOC}$
⑥
⑦
⑧
⑨
+5V
R1 4.7K
R2 4.7K
R3 22K
R4 4.7K
R5 2.7M
R6 1K
R7 4.7K
R8 1K
R9 3.9K
R10 3.9K
R11 1K
R12 100K
C1 4.7
C2 .1
C3 .001
C4 .05
U1
U2
U3
U4
A
Q
Q1 2N3906
Q2 2N3906

IC POWER HOOK-UP

| REF | TYPE | +5V | GND |
|---|---|---|---|
| U1 | NE555V | 8 | 1 |
| U2 | SN7416N | 14 | 7 |
| U3 | SN7432N | 14 | 7 |
| U4 | SN74122N | 14 | 7 |

NOTE

1) ALL RESISTOR VALUES ARE IN OHMS, ¼W, 5%.
2) ALL CAPACITOR VALUES ARE IN $\mu f$.

**FIGURE 7-67 OPTION 05**
**A21, SAMPLE RATE & CONTROL**
**SCHEMATIC #7-05788601 Rev B**

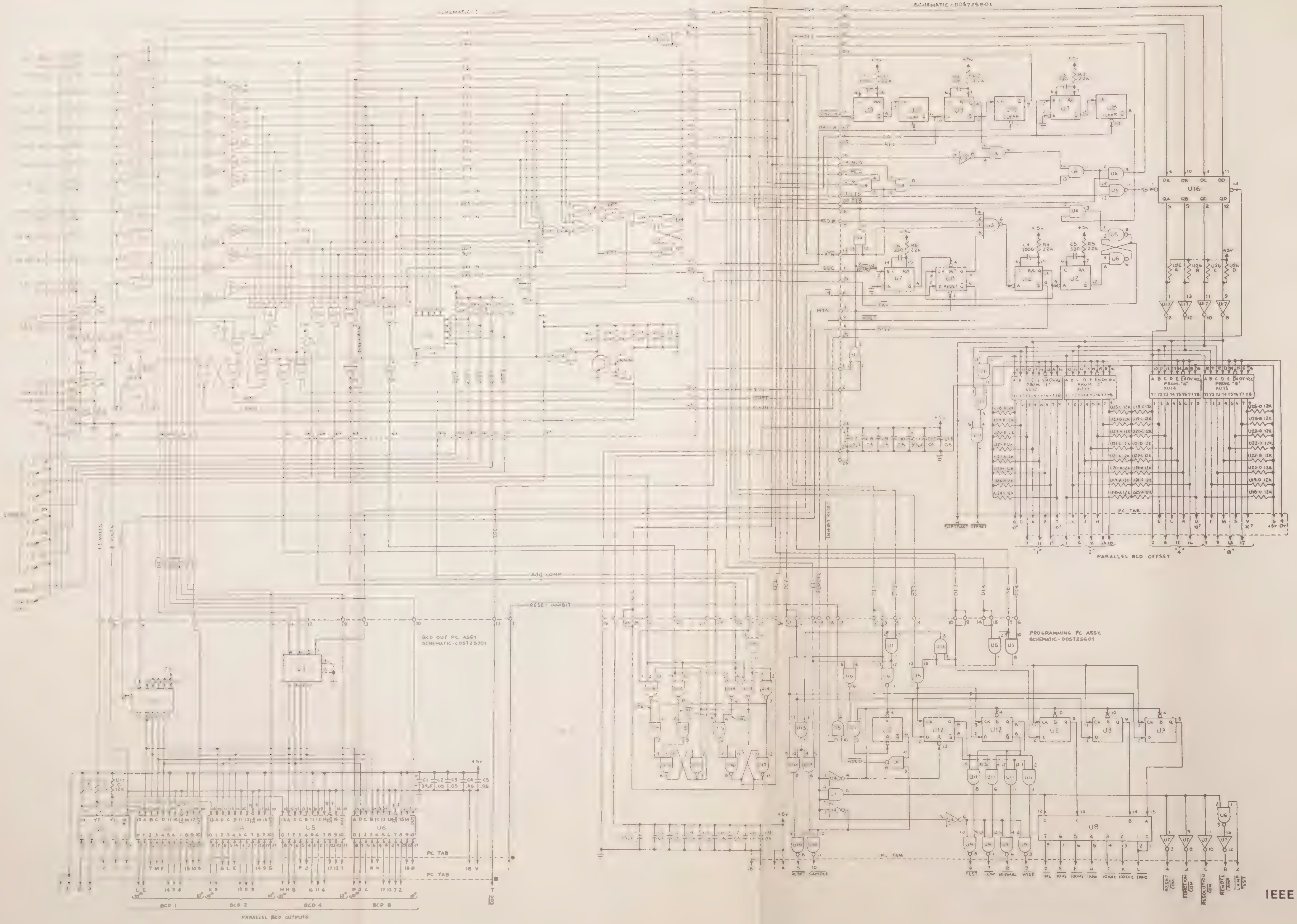
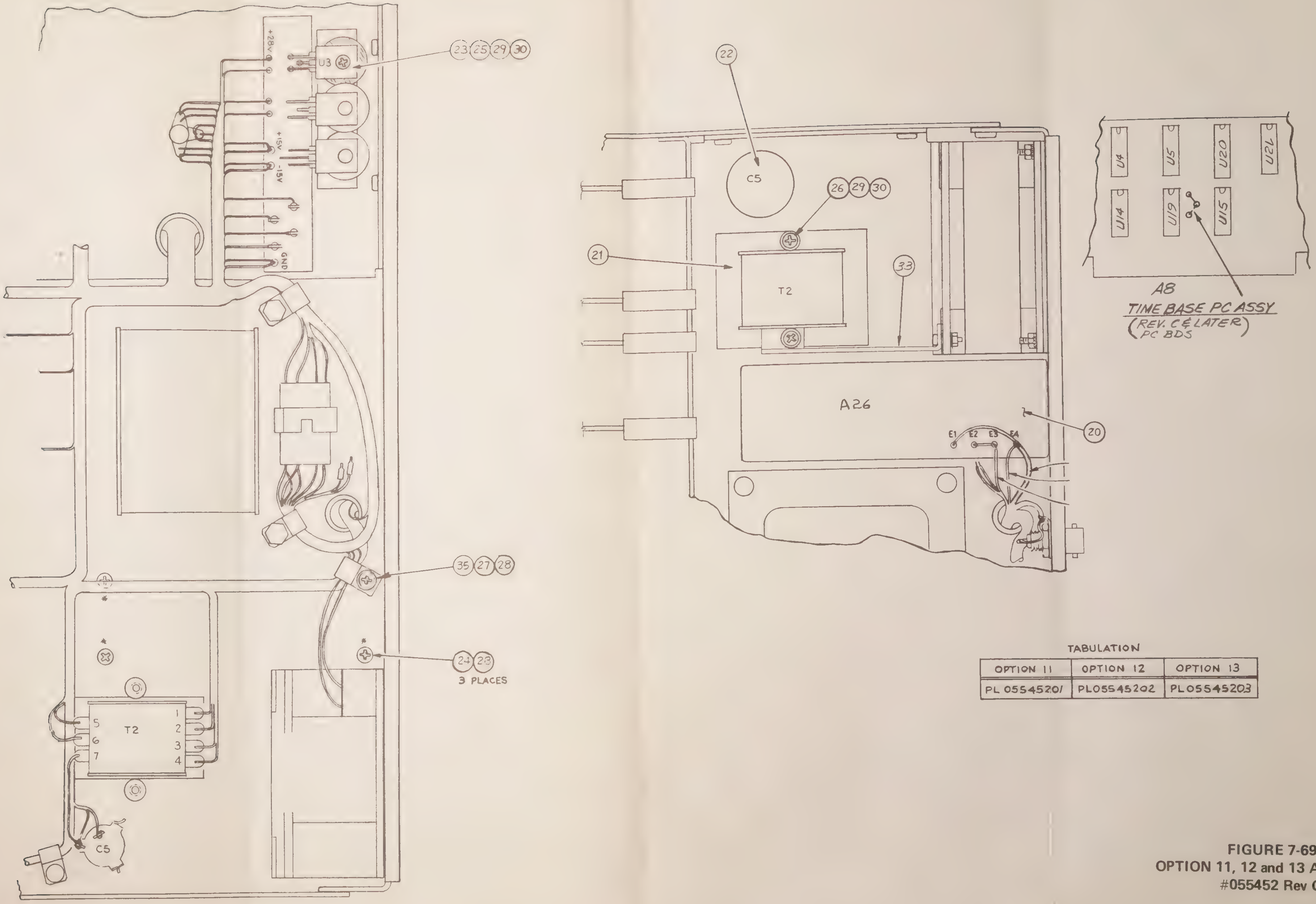

SCHEMATIC-005725801
U16
PROM "1"
PROM "2"
PROM "4"
PROM "8"
PARALLEL BCD OFFSET
SUBTRACT OFFSET
PC TAB
RESET INHIBIT
Add COMP
BCD OUT PC ASSY SCHEMATIC-005725701
PROGRAMMING PC ASSY. SCHEMATIC-005725601
U8
U12
HOLD
BCD 1
BCD 2
BCD 4
BCD 8
PARALLEL BCD OUTPUTS
RESET
SAMPLE
TEST
LOW
NORMAL
WIDE
+5v

FIGURE 7-68 OPTION 05
IEEE 488 INTERCONNECT ASSEMBLY
#057620 Rev D


+28V
U3
+15V
-15V
GND
23 25 29 30
35 27 28
24 28
3 PLACES
T2
1
2
3
4
5
6
7
C5
22
C5
26 29 30
21
T2
33
A26
E1
E2
E3
E4
20
U4
U5
U20
U21
U14
U19
U15
A8
TIME BASE PC ASSY
(REV. C & LATER PC BDS)

TABULATION

| OPTION 11 | OPTION 12 | OPTION 13 |
|---|---|---|
| PL 05545201 | PL05545202 | PL05545203 |

FIGURE 7-69
OPTION 11, 12 and 13 ASSEMBLY
#055452 Rev C

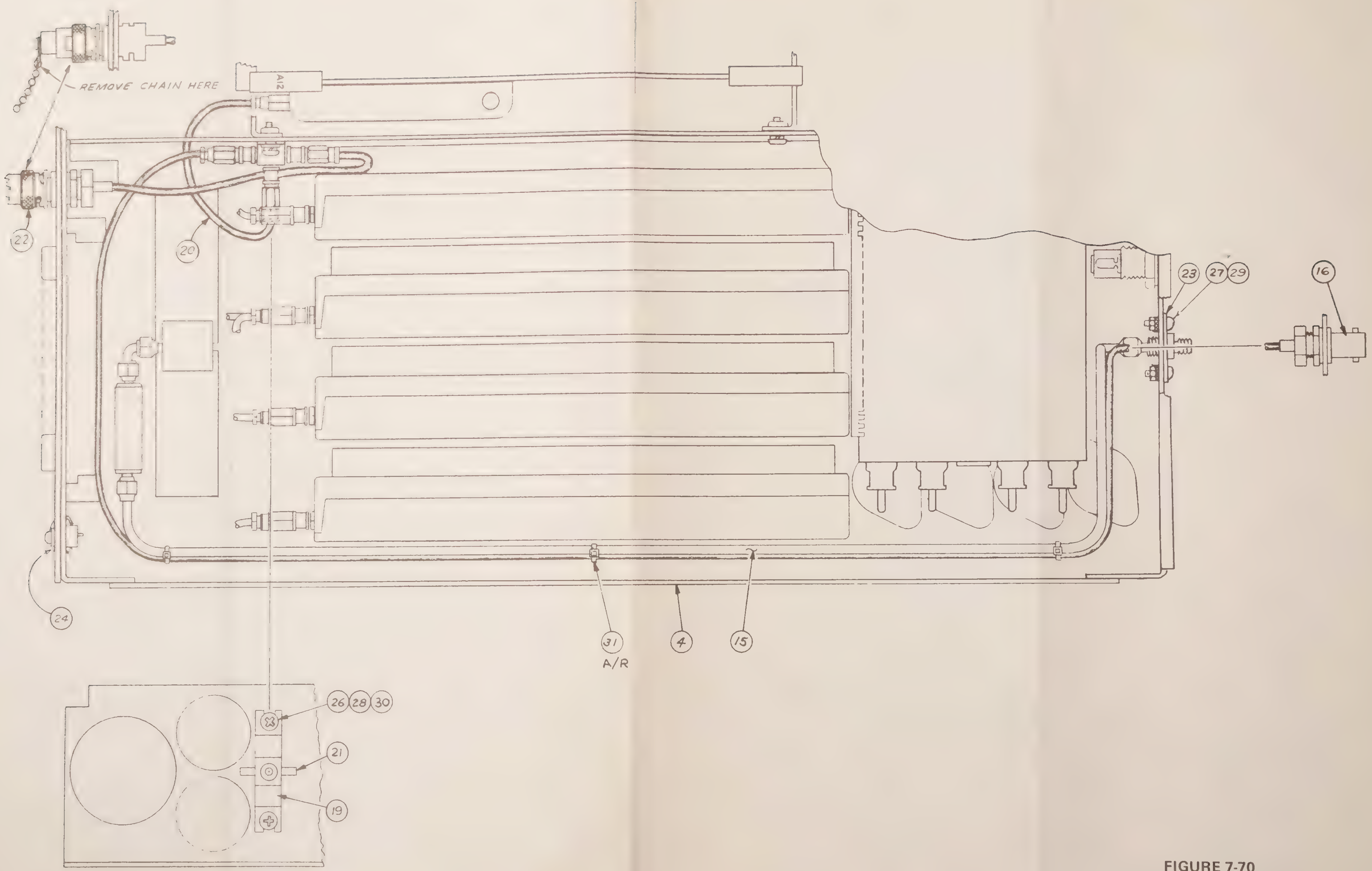
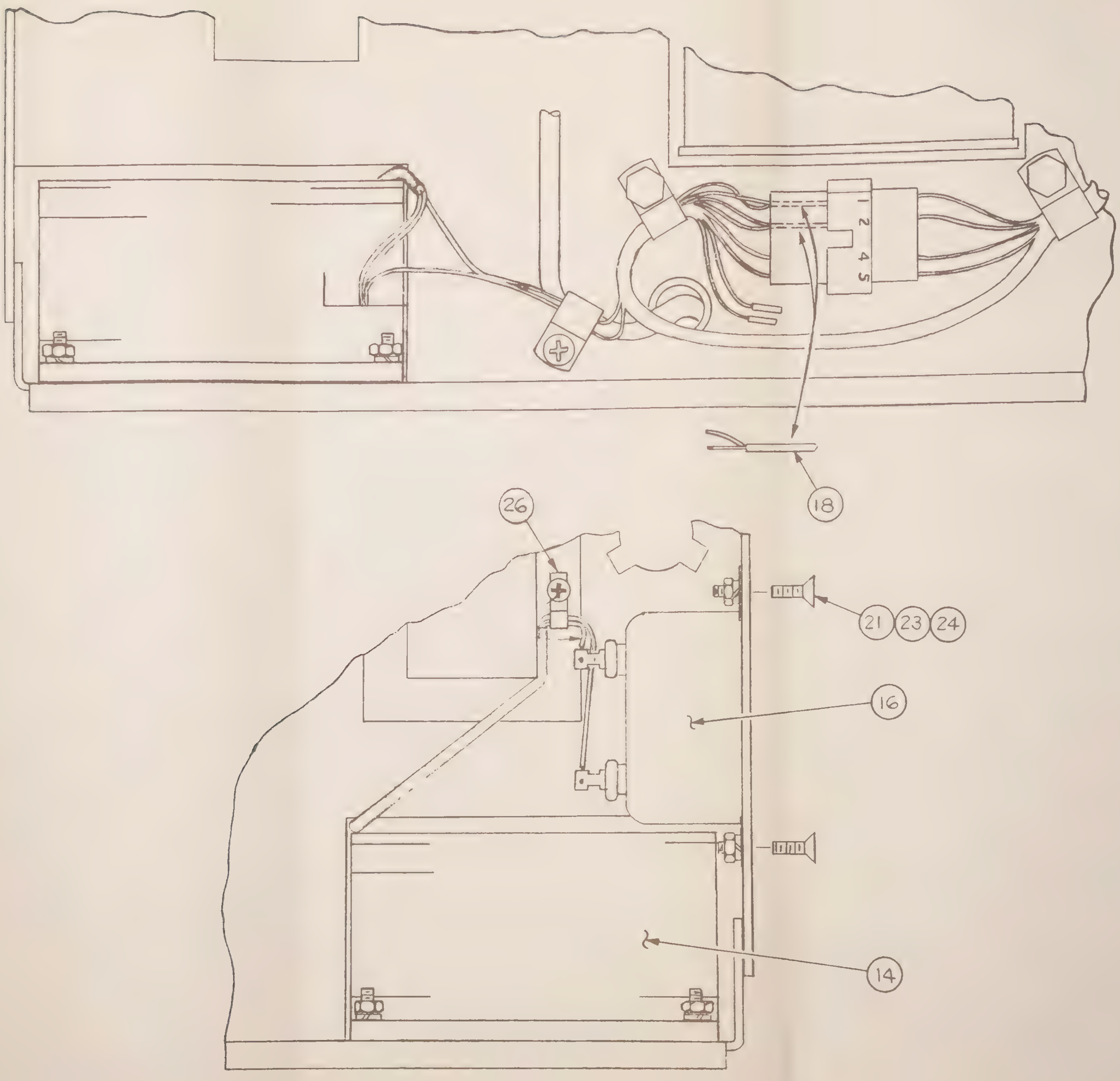
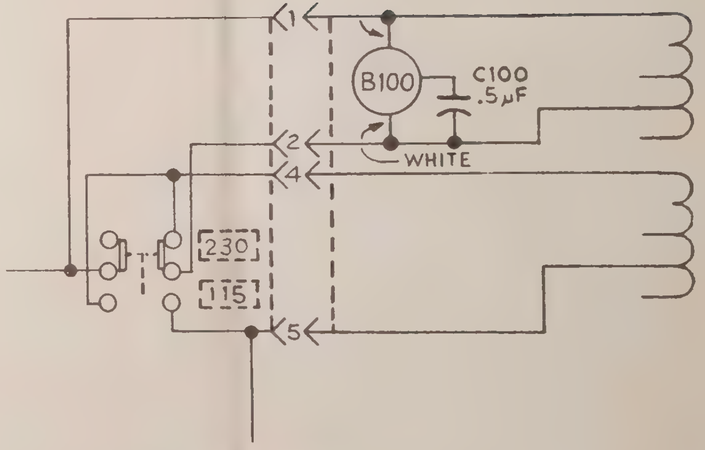

REMOVE CHAIN HERE
A12
22
20
24
23
27
29
16
31
A/R
4
15
26
28
30
21
19

FIGURE 7-70
OPTION 20 REAR INPUTS
#057379 Rev A


1
2
4
5
18
26
21
23
24
16
14


1
2
4
5
B100
C100
.5µF
WHITE
230
115

SUPPLEMENTAL SCHEMATIC

FIGURE 7-71 OPTION 27
50 - 60/400 Hz OPERATION
#055515 Rev A

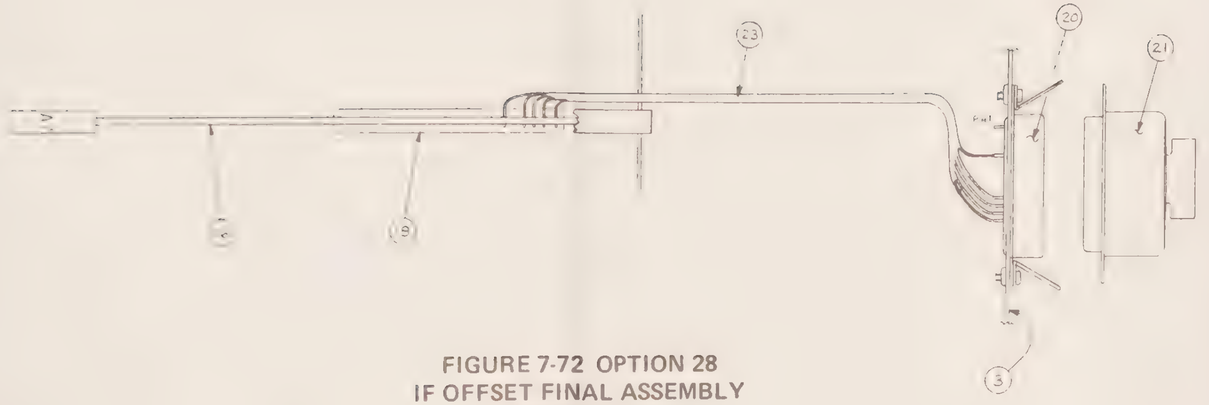

23
20
21
A7
19
3

FIGURE 7-72 OPTION 28
IF OFFSET FINAL ASSEMBLY
#057674 Rev A

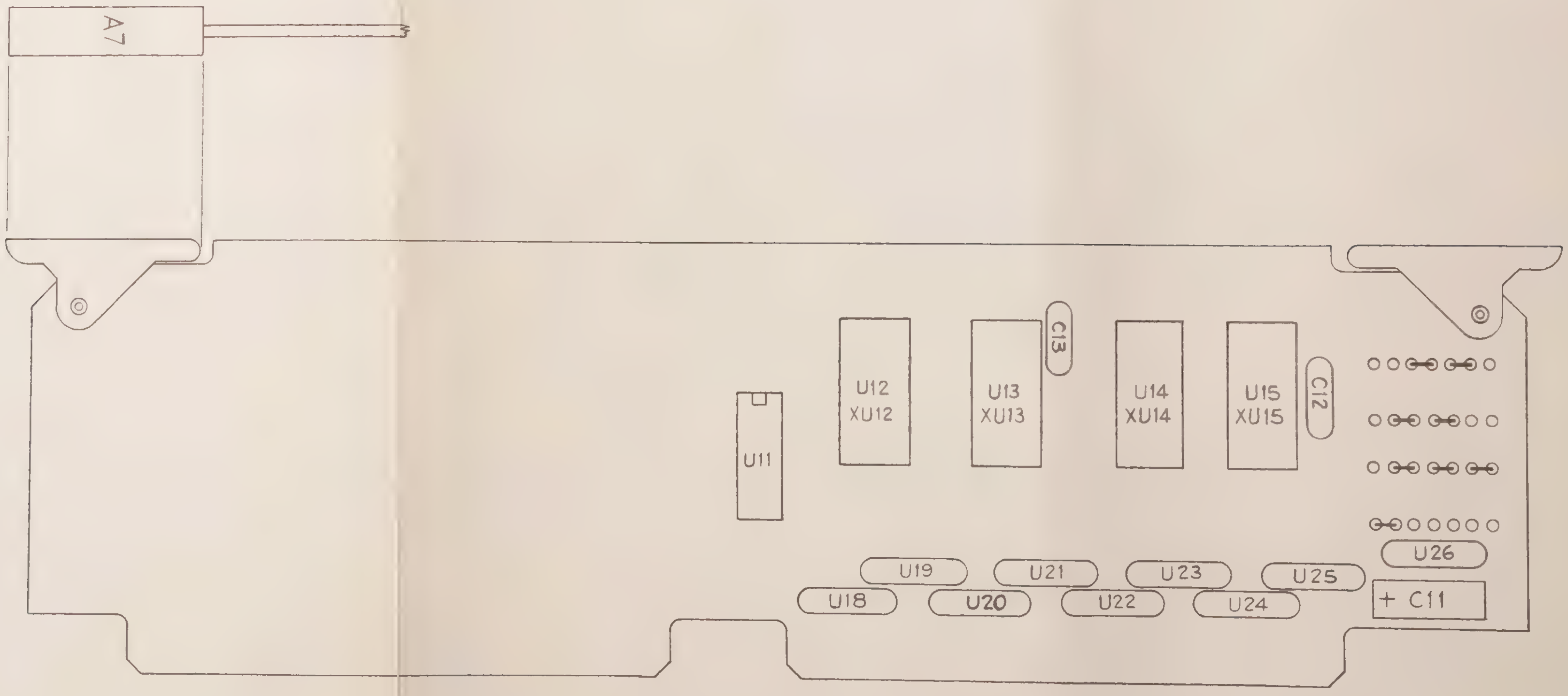
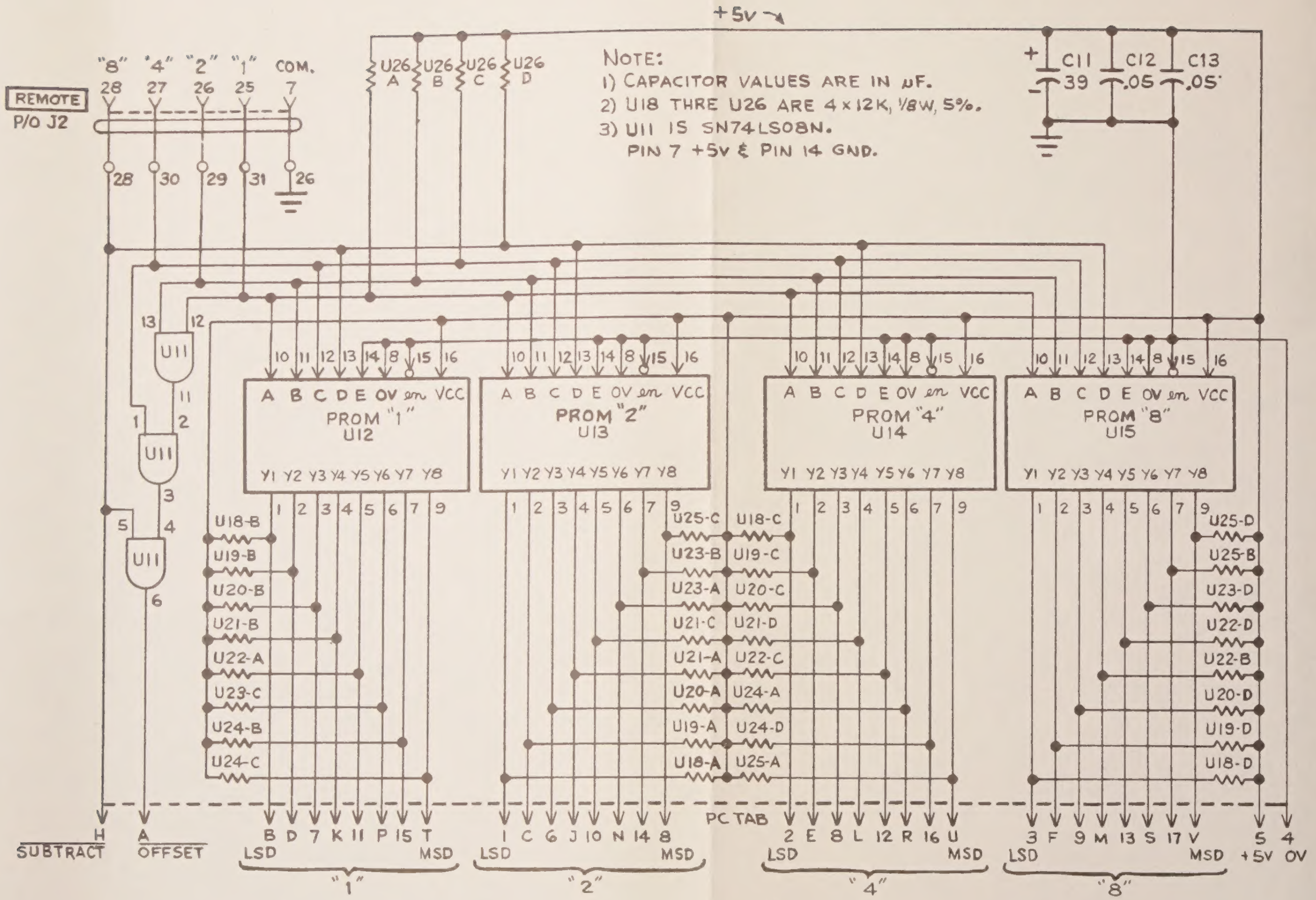

A7
C13
U12
XU12
U13
XU13
U14
XU14
U15
XU15
C12
U11
U19
U21
U23
U25
U26
U18
U20
U22
U24
+ C11

FIGURE 7-73 OPTION 28
A7, OFFSET PC ASSEMBLY
#057259 Rev A



NOTE:
1) CAPACITOR VALUES ARE IN μF.
2) U18 THRU U26 ARE 4 x 12K, 1/8W, 5%.
3) U11 IS SN74LS08N.
PIN 7 +5V & PIN 14 GND.

+5V
REMOTE
P/O J2
"8" "4" "2" "1" COM.
28 27 26 25 7
28 30 29 31 26
U26 A
U26 B
U26 C
U26 D
C11 39
C12 .05
C13 .05
U11
A B C D E OV en VCC
PROM "1" U12
PROM "2" U13
PROM "4" U14
PROM "8" U15
Y1 Y2 Y3 Y4 Y5 Y6 Y7 Y8
10 11 12 13 14 8 15 16
1 2 3 4 5 6 7 9
U18-B U19-B U20-B U21-B U22-A U23-C U24-B U24-C
U25-C U23-B U23-A U21-C U21-A U20-A U19-A U18-A
U18-C U19-C U20-C U21-D U22-C U24-A U24-D U25-A
U25-D U25-B U23-D U22-D U22-B U20-D U19-D U18-D
PC TAB
H SUBTRACT
A OFFSET
B D 7 K 11 P 15 T
1 C 6 J 10 N 14 8
2 E 8 L 12 R 16 U
3 F 9 M 13 S 17 V
5 +5V
4 0V
LSD MSD
"1" "2" "4" "8"

| N° | OFFSET | RESOLUTION |
|---|---|---|
| 0 | | |
| 1 | | |
| 2 | | |
| 3 | | |
| 4 | | |
| 5 | | |
| 6 | | |
| 7 | | |
| 8 | | |
| 9 | | |
| 10 | | |
| 11 | | |
| 12 | | |
| 13 | | |
| 14 | | |
| 15 | 0 | — |

FIGURE 7-74 OPTION 28
A7, OFFSET SCHEMATIC
#7-057259 Rev A

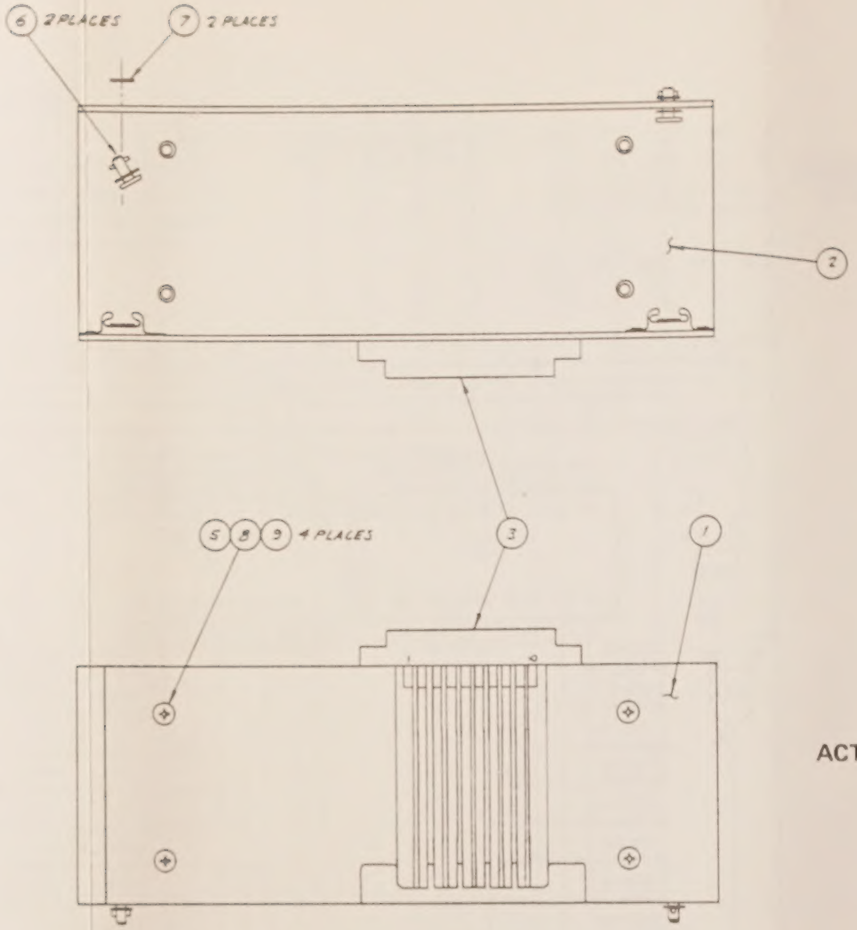

6 2 PLACES
7 2 PLACES
2
5 8 9 4 PLACES
3
1

FIGURE 7-75
ACTO EXTENDER ASSEMBLY
#05502801 Rev A

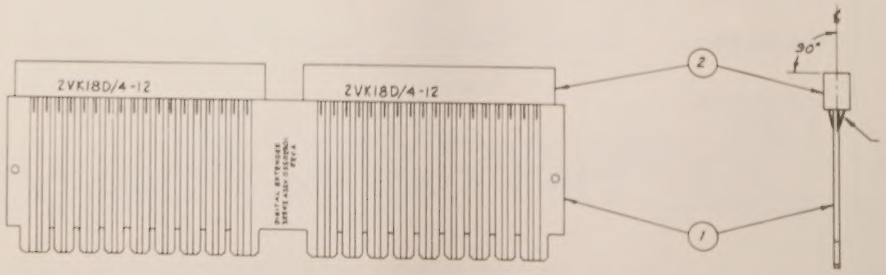

2VK18D/4-12
2VK18D/4-12
90°
2
1

FIGURE 7-76
DIGITAL EXTENDER ASSEMBLY
#05502901 Rev A

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